1991

LOW POWER DISCRETES

DATA BOOK

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Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

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TABLE OF CONTENTS

Section 1. GENERAL INFORMATION

Device Ordering Information 1-1
Hi-Rel Process Capabilities 1-2

Section 2. CROSS REFERENCE 2-1

Section 3. SELECTOR GUIDE

Selector Guide Introduction
JFET Selector Guide 3-1
DMOS Selector Guide 3-6
MOSFET Selector Guide 3-8
JFET Amplifiers 3-11
JFET Geometry Typical Characteristics 3-12
Low Power MOS 3-15
Low Power MOS Geometry Typical Characteristics 3-16

Section 4. JFETs

Introduction to JFETs
2N4117A Series 4-1
2N4338 Series 4-3
2N4391 Series 4-6
2N4416 Series 4-8
2N5114 Series 4-10
2N5114 Series – JANTX, JANTXV 4-12
2N5196 Series 4-14
2N5432 Series 4-17
2N5484 Series 4-19
2N5564 Series 4-21
2N5911 Series 4-23
DPAD1 Series 4-25
J105 Series 4-27
J108 Series 4-29
J111 Series 4-31
J174 Series 4-33
J201 Series 4-36
J210 Series 4-38
J304 Series 4-40
J308 Series 4-42
JPAD5 Series 4-44
PAD1 Series 4-45
PN4117A Series 4-46
PN4391 Series 4-48
SST108 Series 4-50
SST111 Series 4-52
SST174 Series 4-54
SST201 Series 4-57
SST304 Series 4-59
SST308 Series 4-61
SST404 Series 4-63
SST440 Series 4-65
SST4391 Series 4-67
SST4416 4-69
SSTDPAD5 Series 4-71
SSTPAD5 Series 4-72
U290 Series 4-73

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Section 4. JFETs (Cont'd)

U309 Series 4-75
U401 Series 4-77
U421 Series 4-79
U430 Series 4-81
U440 Series 4-83
VCR2N, VCR4N, VCR7N 4-85

JFET Die

NCB Series Die 4-89
NCBD1 Die 4-92
NH Series Die 4-94
NIP Series Die 4-96
NNR1 Die 4-98
NNT1 Die 4-100
NNZ1 Die 4-102
NPA Series Die 4-104
NQP1 Die 4-107
NT Series Die 4-109
NVA Series Die 4-111
NZB Series Die 4-113
NZBD Series Die 4-115
NZF Series Die 4-117
NZFD1 Die 4-119
PSCIA Series Die 4-121

JFET Performance Characteristics

Typical Characteristics: NCB 4-127
Typical Characteristics: NH 4-130
Typical Characteristics: NIP 4-134
Typical Characteristics: NNR 4-137
Typical Characteristics: NNT 4-140
Typical Characteristics: NNZ 4-143
Typical Characteristics: NPA 4-146
Typical Characteristics: NQP 4-149
Typical Characteristics: NT 4-152
Typical Characteristics: NVA 4-155
Typical Characteristics: NZB 4-158
Typical Characteristics: NZF 4-162
Typical Characteristics: PSCIA 4-166

Section 5. DMOS

Introduction to DMOS

SD210DE Series 5-1
SD211DE Series 5-3
SD2100 5-5
SD5000 Series 5-7
SD5400 Series 5-9
SST211 Series 5-11

DMOS Die

DMCA1 Die 5-15
DMCB Series Die 5-17
DMCD1 Die 5-19

DMOS Performance Characteristics

Typical Characteristics: DMCA/B 5-23
Typical Characteristics: DMCD 5-27

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Section 6. LOW POWER MOS

Introduction to Low Power MOS

2N6659 6-1
2N6660 6-3
2N6660 JANTX, JANTXV 6-5
2N6661 6-7
2N6661 JANTX, JANTXV 6-9
2N7000 6-11
2N7002 6-13
3N163 Series 6-15
ND2012L, ND2020L 6-17
ND2406L, ND2410L 6-20
TD1001Y 6-23
TD1004Y 6-25
TD2001Y 6-27
TD3001Y 6-29
TD3002Y 6-32
TN0201L, TN0401L 6-35
TN0601L 6-37
TN1206L 6-39
TN2010L, TN2410L 6-41
TN2460 Series 6-43
TN3512L, TN4012L 6-45
TP0610 Series 6-47
TP1220L, TP2020L 6-50
TP2010L, TP2410L 6-52
TQ1001J 6-54
TQ1004J 6-56
VN46AFD 6-58
VN66AFD 6-60
VN88AFD 6-62
VN0300 Series 6-64
VN0605T 6-66
VN0606M, VN0808M 6-68
VN0610L, VN10KE, VN10KM 6-70
VN0610LL, VN10LM 6-72
VN1206 Series 6-74
VN1210 Series 6-76
VN2010L 6-78
VN2222 Series 6-80
VN2222L 6-82
VN2406 Series 6-84
VN2410 Series 6-86
VN4012L, VN3515L 6-88
VN50300 Series 6-90
VP0300 Series 6-92
VP0610 Series 6-94
VP0808 Series 6-97
VP1008 Series 6-99
VP2020L 6-101
VP2410L 6-103
VQ1000 Series 6-105
VQ1001 Series 6-107
VQ1004 Series 6-109
VQ2001 Series 6-111
VQ2004 Series 6-113
VQ3001 Series 6-115
VQ7254J 6-117

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Section 6. LOW POWER MOS (Cont'd)

Low Power MOS Die

MRA1 Die 6-121
VDDQ Series Die 6-123
VDDV Series Die 6-125
VNDB1 Die 6-127
VNDN1 Die 6-129
VNDO1 Die 6-131
VNDP1 Die 6-133
VNDQ Series Die 6-135
VNDS1 Die 6-141
VNDV1 Die 6-143
VPDQ1 Die 6-145
VPDS1 Die 6-147
VPDV Series Die 6-149

Low Power MOS Performance Characteristics

Typical Characteristics: MRA 6-155
Typical Characteristics: VDDQ20 6-157
Typical Characteristics: VDDV24 6-160
Typical Characteristics: VNDB24 6-163
Typical Characteristics: VNDN24 6-166
Typical Characteristics: VNDO50 6-169
Typical Characteristics: VNDP06 6-172
Typical Characteristics: VNDQ03 6-175
Typical Characteristics: VNDQ06 6-178
Typical Characteristics: VNDQ09 6-182
Typical Characteristics: VNDQ12 6-185
Typical Characteristics: VNDQ20 6-188
Typical Characteristics: VNDS06 6-191
Typical Characteristics: VNDV40 6-194
Typical Characteristics: VPDQ20 6-198
Typical Characteristics: VPDS06 6-202
Typical Characteristics: VPDV10 6-206
Typical Characteristics: VPDV24 6-210

Section 7. PACKAGE OUTLINES 7-1

Section 8. APPLICATIONS

LPD-1: An Introduction to FETs 8-1
LPD-2: FET Biasing 8-9
LPD-3: The FET Constant-Current Source 8-20
LPD-4: P-Channel MOSFETs, The Best Choice for High-Side Switching 8-23
LPD-5: Depletion-Mode MOSFETs Expand Circuit Opportunities 8-26
LPD-6: Spice Parameters for Select JFETs 8-32

Section 9. PUBLICATIONS INDEX 9-1

Section 10. SALES OFFICES 10-1

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ALPHA-NUMERIC INDEX

2N4117A 4-1
2N4118A 4-1
2N4119A 4-1
2N4338 4-3
2N4339 4-3
2N4340 4-3
2N4341 4-3
2N4391 4-6
2N4392 4-6
2N4393 4-6
2N4416 4-8
2N4416A 4-8
2N5114 4-10
2N5115 4-10
2N5116 4-10
2N5114 JANTX, JANTXV 4-12
2N5115 JANTX, JANTXV 4-12
2N5116 JANTX, JANTXV 4-12
2N5196 4-14
2N5197 4-14
2N5198 4-14
2N5199 4-14
2N5432 4-17
2N5433 4-17
2N5434 4-17
2N5484 4-19
2N5485 4-19
2N5486 4-19
2N5564 4-21
2N5565 4-21
2N5566 4-21
2N5911 4-23
2N5912 4-23
2N6659 6-1
2N6660 6-3
2N6660 JANTX, JANTXV 6-5
2N6661 6-7
2N6661 JANTX, JANTXV 6-9
2N7000 6-11
2N7002 6-13
3N163 6-15
3N164 6-15
DMCA1CHP 5-15
DMCB1CHP 5-17
DMCB2CHP 5-17
DMCD1CHP 5-19
DPAD1 4-25
DPAD5 4-25
DPAD50 4-25
J105 4-27
J106 4-27
J107 4-27
J108 4-29
J109 4-29
J110 4-29
J111 4-31
J112 4-31
J113 4-31
J174 4-33
J175 4-33
J176 4-33
J177 4-33
J201 4-36
J202 4-36
J210 4-38
J211 4-38
J212 4-38
J304 4-40
J305 4-40
J308 4-42
J309 4-42
J310 4-42
JPAD5 4-44
JPAD50 4-44
MRA1CHP 6-119
NCB1CHP 4-89
NCB2CHP 4-89
NCB3CHP 4-89
NCB4CHP 4-89
NCBD1CHP 4-92
ND2012L 6-17
ND2020L 6-17
ND2406L 6-20
ND2410L 6-20
NH1CHP 4-94
NH2CHP 4-94
NH3CHP 4-94
NIP1CHP 4-96
NIP2CHP 4-96
NIP3CHP 4-96
NNR1CHP 4-98
NNT1CHP 4-100
NNZ1CHP 4-102
NPA1CHP 4-104
NPA2CHP 4-104
NPA3CHP 4-104
NPA4CHP 4-104
NQP1CHP 4-107
NT1CHP 4-109
NT2CHP 4-109
NT3CHP 4-109
NVA1CHP 4-111
NVA2CHP 4-111
NVA3CHP 4-111
NZB1CHP 4-113
NZB2CHP 4-113
NZB3CHP 4-113
NZBD1CHP 4-115
NZBD2CHP 4-115
NZF1CHP 4-117
NZF2CHP 4-117
NZF3CHP 4-117
NZFD1CHP 4-119
PAD1 4-45
PAD5 4-45
PAD50 4-45
PN4117A 4-46
PN4118A 4-46
PN4119A 4-46
PN4391 4-48
PN4392 4-48
PN4393 4-48
PSCIA1CHP 4-121
PSCIA2CHP 4-121
PSCIA3CHIP 4-121
PSCIA4CHP 4-121
TD1001Y 6-23
TD1004Y 6-25
TD2001Y 6-27
TD3001Y 6-29
TD3002Y 6-32
TN0201L 6-35
TN0401L 6-35
TN0601L 6-37
TN1206L 6-39

TN2010L 6-41
TN2410L 6-41
TN2460L 6-43
TN2460T 6-43
TN3512L 6-45
TN4012L 6-45
TP0610L 6-47
TP0610T 6-47
TP1220L 6-50
TP2010L 6-52
TP2020L 6-50
TP2410L 6-52
TQ1001J 6-54
TQ1004J 6-56
SD210DE 5-1
SD211DE 5-3
SD214DE 5-1
SD215DE 5-3
SD2100 5-5
SD5000I 5-7
SD5000N 5-7
SD5001N 5-7
SD5400CY 5-9
SD5401CY 5-9
SST108 4-50
SST109 4-50
SST110 4-50
SST111 4-52
SST112 4-52
SST113 4-52
SST174 4-54
SST175 4-54
SST176 4-54
SST177 4-54
SST201 4-57
SST202 4-57
SST211 5-11
SST215 5-11
SST304 4-59
SST305 4-59
SST308 4-61
SST309 4-61
SST310 4-61
SST404 4-63
SST406 4-63
SST440 4-65
SST441 4-65
SST4391 4-67
SST4392 4-67
SST4393 4-67
SST4416 4-69
SSTDPAD5 4-71
SSTDPAD100 4-71
SSTPAD5 4-72
SSTPAD100 4-72
U290 4-73
U291 4-73
U309 4-75
U310 4-75
U401 4-77
U404 4-77
U406 4-77
U421 4-79
U423 4-79
U430 4-81
U431 4-81
U440 4-83
U441 4-83
VCR2N 4-85
VCR4N 4-85
VCR7N 4-85
VDDQ1CHP 6-123
VDDQ2CHP 6-123
VDDV1CHP 6-125
VDDV2CHP 6-125
VN10KE 6-70
VN10KM 6-70
VN10LM 6-72
VN66AFD 6-60
VN88AFD 6-62
VN46AFD 6-58
VN0300L 6-64
VN0300M 6-64
VN0605T 6-66
VN0606M 6-68
VN0610L 6-70
VN0610LL 6-72
VN0808M 6-68
VN1206L 6-74
VN1206M 6-74
VN1210L 6-76
VN1210M 6-76
VN2010L 6-78
VN2222L 6-82
VN2222LL 6-80
VN2222LM 6-80
VN2406D 6-84
VN2406L 6-84
VN2406M 6-84
VN2410L 6-86
VN2410M 6-86
VN3515L 6-88
VN4012L 6-88
VN50300L 6-90
VN50300T 6-90
VNDB1CHP 6-127
VNDN1CHP 6-129
VNDO1CHP 6-131
VNDP1CHP 6-133
VNDQ1CHP 6-135
VNDQ2CHP 6-135
VNDQ3CHP 6-135
VNDQ4CHP 6-135
VNDQ5CHP 6-135
VNDS1CHP 6-141
VNDV1CHP 6-143
VP0300B 6-92
VP0300L 6-92
VP0300M 6-92
VP0610L 6-94
VP0610T 6-94
VP0808B 6-97
VP0808L 6-97
VP0808M 6-97
VP1008B 6-99
VP1008L 6-99
VP1008M 6-99
VP2020L 6-101
VP2410L 6-103
VPDQ1CHP 6-145
VPDS1CHP 6-147
VPDV1CHP 6-149
VPDV2CHP 6-149
VQ1000J 6-105
VQ1000P 6-105
VQ1001J 6-107
VQ1001P 6-107
VQ1004 6-109
VQ1006 6-109
VQ2001J 6-111
VQ2001P 6-111
VQ2004 6-113
VQ2006 6-113
VQ3001J 6-115
VQ3001P 6-115
VQ7254J 6-117

General Information 1

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LOW POWER DISCRETES DEVICE ORDERING INFORMATION

NOMENCLATURE

Technology/Design Prefix-Device Family

CR	-Si Standard N-Channel Current Regulator
DPAD	-Si Standard Dual JFET Diode
J	-Si Standard TO-92 Cased FET
JPAD	-Si Standard JFET Diode
ND	-Si Standard Low Power Depletion-Mode MOS
PAD	-Si Standard JFET Diode
PN	-Si Standard TO-92 Cased FET
SD	-Si Standard DMOS FET
SST	-Surface Mount Device
TN	-Si Standard Low Threshold N-Channel LPMOS
TP	-Si Standard Low Threshold P-Channel LPMOS
U	-Si Standard FET
V	-Si Standard or Special Low Power MOS
VCR	-Si Standard N-Channel Voltage Controlled Resistors
2N	-JEDEC-Registered Device
3N	-JEDEC-Registered Device

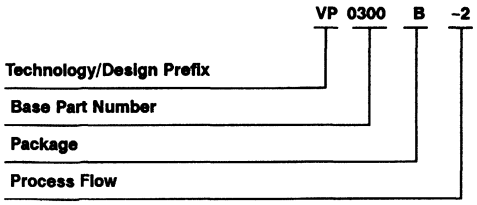
Process Option

-1 Contact Factory - 750B Visual, MIL-STD-750 Processing (JANTXV)

-2 Contact Factory - 750B Visual, MIL-STD-750 Processing (JANTX)

Package

-18 Std TO-92 and TO-237 with Center Lead Formed Toward Flat in TO-18 Pin Circle
-TR1 Tape and Reel Available on TO-92 and TO-237 FETs
-TA Tape and Ammo Pack Available on TO-92 and TO-237 FETs
-T1, T2 Tape and Reel Available on SOT-23, SOT-143 and SOIC Products



Package

Hermetic

B	-TO-39
E	-TO-52
G	-TO-18
P	-Sidebraze DIP

Plastic

D	-TO-220
J	-Plastic DIP
L	-TO-92
M	-TO-237
T	-SOT-23, SOT-143
Y	-SO-8, SO-14

Process Flow

Level-1	MIL-S-19500, US Build
Level-2	MIL-S-19500, Offshore Build
Level-3	HTRB 96 Hour Minimum Burn-In at 150°C

HI-REL PROCESS CAPABILITIES

Siliconix has been dedicated to serving the Military/Hi-Rel market for over twenty years. We do so by providing QPL (Qualified Parts List) devices, Standard Hi-Rel Process Flows, Hi-Rel Specials, and Lockheed Monitored Line devices.

Low Power Discrete products for Military/Hi-Rel applications offer performance benefits that cannot be matched with any other existing technology. LPD devices are inherently radiation-hardened, as high as 6×10^5 RAD (Si). They perform reliably at cryogenic temperatures, proving they can operate as a "focal plane preamp" at a liquid helium temperature of 35°K.

QPL Devices

The Low Power Discrete product line features 11 QPL devices. These products are qualified under Military Specification MIL-S-19500, the General Specification for Semiconductor Devices.

Standard Hi-Rel Processes

Most of Siliconix's hermetic-packaged Low Power Discrete products are offered with -1 and -2 process flows. Use of these standard processes can eliminate the need for a costly source control drawing. The -1 process flow provides many of the 100% screening steps for a JANTXV-level device and the -2 flow provides many of the 100% screening steps for a JANTX-level device, both as called out in the MIL-S-19500.

Hi-Rel "Specials"

Where QPL, -1 and -2 process flows do not meet our customers' needs, Siliconix can provide processing based on a customer source control drawing or detail specification. We have built a reputation in the industry for our skill in manufacturing such Hi-Rel Specials. All MIL-S-19500/MIL-STD-750 requirements through JANTXV-level processing can be provided. Baseline control is offered.

Lockheed Monitored Line

A resident team of quality and reliability engineers provides on-line process monitoring for Lockheed monitored parts. With approval from the U.S. Air Force, this service can be used by any aerospace company or government agency.

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LOW POWER DISCRETE QUALIFIED PARTS LIST (QPL)

Products Qualified as Standard Devices under Military Specification

MIL-S-19500: Semiconductor Devices, General Specification For

Government Designation	Siliconix Designation Type Number (Cage/Code)	Detail Specification (Slash Sheet)
2N4856 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	MIL-S-19500/385
2N4857 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	
2N4858 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	
2N4859 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	
2N4860 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	
2N4861 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	
2N5114 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	MIL-S-19500/476
2N5115 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	
2N5116 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	
2N6660 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	
2N6661 (JAN) JANTX JANTXV	CDBN 17856 (FSCM)	MIL-S-19500/547A

- JANTXV: JANTX plus 100% internal visual inspection
- JANTX: JAN plus 100% processing to MIL-S-19500 including Group A, B, C testing
- JAN: Controlled lot with sample environmental and life testing

PROCESS OPTION FLOWS FOR DISCRETE DEVICES

Test and Condition			U.S. Build Only If Specified	JANTXV Build & Test In Qualified 19500 Facility	JANTX Build Offshore Test In Qualified 19500 Facility	
	Methods Per MIL-S-19500 For					
Description	JFETs	LOPMOS DMOS	Space Rated Extended Hi-Rel	-1 Build & Test In Qualified 19500 Facility	-2 Offshore Build & Test	Industrial Standard
Traceability to W/L			X	N/A	N/A	N/A
SEM	2077	2077	X	N/A	N/A	N/A
Internal Visual	2072	2069	Inhouse spec Cond. A	Inhouse spec Cond. B	Inhouse spec Cond. B	Inhouse spec IND.
Die shear**	2017	2017 N/A for MOSPOWER	X	N/A	N/A	N/A
Bond strength** cert/data	2037	2037	X	N/A	N/A	N/A
Stab bake	1032	1032	X	X	X	N/A
Temp cycle	1051	1051	X	X	X	N/A
Centrifuge (if reg.)	2006	2006	X	X	X	N/A
PIND	2052	2052	X	N/A	N/A	N/A
Fine leak (see note)	1071	1071	Cond. G or H	Cond. G or H	Cond. G or H	AQL = 1% hermetic
Gross leak (see note)	1071	1071	Cond. C or K	Cond. C or K	Cond. C or K	AQL = 1% hermetic
1st electrical	per spec	per spec	Read/Record	Go/No-Go MOS	Go/No-Go MOS	N/A
Burn-in	N/A	1042 Cond. B	48 hrs per dwg.	48 hrs per dwg.	48 hrs per dwg.	N/A
Interim electrical post burn-in	per spec	per spec	Read/Record per spec	Read/Record per spec	Read/Record per spec	N/A
Burn-in	1039 Cond A	1042 Cond A	160 min MOS* 240 min JFET	160 hrs	160 hrs	N/A

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PROCESS OPTION FLOWS FOR DISCRETE DEVICES (Cont'd)

Test and Condition			U.S. Build Only If Specified	JANTXV Build & Test In Qualified 19500 Facility	JANTX Build Offshore Test In Qualified 19500 Facility	
	Methods Per MIL-S-19500 For					
Description	JFETs	LOPMOS DMOS	Space Rated Extended Hi-Rel	-1 Build & Test In Qualified 19500 Facility	-2 Offshore Build & Test	Industrial Standard
Intermin electrical post burn-in	Static per spec	Static per spec	Read/Record 25c PDA = 10%	Read/Record 25c PDA = 10%	Read/Record 25c PDA = 10%	N/A
Final electrical	Static 25c	Static 25c	25c, -55c, +125c	25c	25c	25c
X-Ray	2076	2076	X	N/A	N/A	N/A
External visual	2012	2012	X	X	X	AQL = 0.65%
QCI A 19500 MIL spec	per spec	per spec	X	X Note	X Note	AQL = 0.065%
QCI B 19500 MIL spec	per spec	per spec	X	X Note	X Note	N/A
QCI C 19500 MIL spec	per spec	per spec	X	X Note	X Note	N/A
Deltas option	per spec	per spec	Option	per spec	per spec	N/A
Solder Dip option	per spec	per spec	Option	per spec	per spec	Option
Note: Fine/gross leak test may be done at either steps after centrifuge or after final electrical ** = Test performed on line during assembly procedure (monitor)			Notice: On U.S. builds unless otherwise specified by 19500 or dwg. parts may be assembled off shore	Note: -1 & -2 devices QCI B & C will be performed by dwg. and/or P.O. only. All S/S devices will be tested accordingly		

1

PROCESS OPTION FLOWS FOR DISCRETE CHIP/WAFER

Standard Die/Chip, and Chip Samples with Element Evaluation		
Die ship element evaluation Method 5008 Class B Subgroup 1 and 3 performed in-line screen.	Die ship. No canned samples.	Die Wafer Form
Wafer probe static 25°C (min) per device spec visual Method 2069 Cond B, MIL-STD-750.	Wafer probe static 25°C (min) per device spec visual Method 2069 Cond B, MIL-STD-750.	Wafer probe static 25°C (min) per device spec.
Canned samples: Per MIL-STD-883, Class B device. Subgroup 1 (ss-10/0) internal visual Method 2069 Cond B inhouse spec. Subgroup 2 (ss-10/1) final electrical static @ 25°C, elevated temperature per device spec. Subgroup 3 (5 die min) (s/s = 10/0 or 20/1 wires) NDT Method 2023 wire bond eval (bond pull). Method 2011 (cert & data). *SEM available	Die Prep Process	

Cross Reference 2

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CROSS REFERENCE

Siliconix Direct Replacement Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications.

Siliconix Similar Replacement Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed, as these parts may have different pin configurations. Before selecting a device as a substitute, compare the specifications. For devices not shown in this guide, or for additional information, the user should contact the nearest Siliconix sales office.

INDUSTRY PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
AM0610LL	VN0610LL	
AM10LM	VN10LM	
AM2222LL	VN2222LL	
AM2222LM	VN2222LM	
BF256LA		2N5485
BF256LB		2N5485
BF256LC		2N5486
BFR31		SST202
BFT10	SST202	
BSD10	SD2100	
BSD12	SD2100	
BSD212	SD210DE	
BSD213	SD211DE	
BSD214	SD214DE	
BSD215	SD215DE	
BSR66		VN0606M
BSR67		VN0606M
BSR76		VN2410M
BSS100		VN1206L
BSS101		VN2406L
BSS110		TP0610L
BSS124		VN4012L
BSS83		SST211
BSS84		TP0610T
BST70		VN0606M
BST72A		VN0606M
BSV78		2N4856JAN
BSV79		2N4857JAN
BSV80		2N4856JAN
BS107P	VN2010L	
CRR1950		CR200
CRR2900		CR300
CRR4300		CR430
DN5566	2N5566	
DN5567	2N5566	
DPAD2		DPAD5
DPAD10	DPAD5	
DPAD20	DPAD5	
DPAD100	DPAD50	
ECG464		3N164
ECG466	2N4091	
ECG467	J111	
E100	J203-18	
E101	J201-18	
E102	J202-18	
E105	J105-18	
E106	J106-18	
E107	J107-18	
E108	J108-18	
E109	J109-18	
E110	J110-18	
E111	J111-18	
E112	J112-18	
E113	J113-18	
E174	J174-18	
E175	J175-18	
E176	J176-18	
E177	J177-18	
E201	J201-18	
E202	J202-18	
E210	J210-18	
E211	J211-18	
E212	J212-18	
E300		J212-18
E304	J304-18	
E305	J305-18	
E308	J308-18	
E309	J309-18	
E310	J310-18	
E420		U440
E421		U441
E430		U430
E431		U431
E500	J500	
E501	J501	
E502	J502	
E503	J503	
E504	J504	
E505	J505	
E508	J508	
E507	J507	
FE0854A		J210
FE0854B		J210
FE0854C		J202
FN4117	2N4117A	
FN4117A	2N4117A	
FN4118	2N4118A	
FN4118A	2N4118A	
FN4119	2N4119A	
FN4119A	2N4119A	
FN4392	2N4392	
FN4393	2N4393	

CROSS REFERENCE

Siliconix incorporated

INDUSTRY PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
FT704	3N163	
IMF5911	2N5911	
IMF5912	2N5912	
IMF8485		U404
IVN6300ANF	VN0808M	
J110A		J110
J111A		J111
J203		J202
J204		J201
J230		J202
J231		J202
J232		J202
J270		J177
J271		J176
J300		J211
J300-18		J212-18
J300A		J210
J300B		J210
J300C		J211
J300D		J212
J552		J504
J553		J503
J554		J505
J555		J507
J556		J509
J557		J511
J9100		J504
JPAD10		JPAD5
JPAD20		JPAD5
JPAD100		JPAD50
JPAD200		JPAD50
JPAD500		JPAD50
KE4091		PN4391
KE4091		PN4392
KE4091		PN4393
KE4220		J202
KE4222		J203
KE4391		PN4391
KE4392		PN4392
KE4393		PN4393
K114		J211
K114-18		J211-18
K210-18	J210-18	
K211-18	J211-18	
K300-18	J210-18	
K304-18	J304-18	
K305-18	J305-18	
K308-18	J308-18	
K309-18	J309-18	
K310-18	J310-18	
M163	3N163	
M164	3N164	
M440		U440
M441		U441
M5911		2N5911
M5912		2N5912
MEF101		J203
MEM511		3N163
MFE825		3N163
MFE910		VN10KE
MFE2010	2N5434	
MFE2011	2N5433	
MFE2012	2N5432	
MFE3069	2N4341	
MFE3459	2N4339	
MFE3460	2N4338	

INDUSTRY PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
MFE9200		VN2406L
MK10		J212
MMBF170		2N7002
MMBF4391	SST4391	
MMBF4392	SST4392	
MMBF4393	SST4393	
MMBF4416	SST4416	
MMBFJ111	SST111	
MMBFJ112	SST112	
MMBFJ113	SST113	
MMBFJ174	SST174	
MMBFJ175	SST175	
MMBFJ176	SST176	
MMBFJ177	SST177	
MMBFJ309	SST309	
MMBFJ310	SST310	
MPF10LM		VN10LM
MPF102		J304
MPF103		J202
MPF104		J202
MPF105		J202
MPF106	2N5485	
MPF107	2N5486	
MPF108		J304
MPF109		J304
MPF110	2N3819	
MPF111		J304
MPF112		J304
MPF203	J310	
MPF820	J212	
MPF910		VN10LM
MPF970	J174	
MPF971	J176	
MPF4391	PN4391-18	
MPF4392	PN4392-18	
MPF4393	PN4393-18	
MPF6660		2N6660
MPF6661		2N6661
MFP9200		VN2406L
NF500	2N4416	
NF501	2N4416	
NF506	2N4416	
NF510	2N4393	
NF511	2N4393	
NF520	2N4339	
NF521	2N4339	
NF522	2N4339	
NF523	2N4340	
NF530	2N4341	
NF531	2N4339	
NF532	2N4341	
NF533	2N4339	
NF550		2N5566
NF580	2N5432	
NF581	2N5432	
NF582	2N5433	
NF583	2N5434	
NF584	2N5433	
NF585	2N4859	
NF3819		J212-18
NF4445		2N5432
NF4446		2N5433
NF4447		2N5432
NF4448		2N5433
NF5102		J202
NF5457	J202	

Siliconix incorporated

CROSS REFERENCE

INDUSTRY PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
NF5458	J202	
NF5484	2N5484	
NF5485	2N5485	
NF5486	2N5486	
NOS100B		ND2410L
NOS101B		ND2410L
NOS102B		ND2410L
NPC108	J304	
NPC108A	J304	
P1086		J174
P1087E		J176
PAD2	PAD1	
PAD10	PAD5	
PAD20	PAD5	
PAD100	PAD50	
PMBF4391	SST4391	
PMBF4392	SST4392	
PMBF4393	SST4393	
PN4091		J111
PN4092		J112
PN4093		J113
PN4117	PN4117A	
PN4118	PN4118A	
PN4119	PN4119A	
PN4120	PN4118A	
PN4120A	PN4118A	
PN4303		J304
PN4416		J304
PN4856		2N4856JAN
PN4857		2N4857JAN
PN4858		2N4858JAN
PN4859		2N4859JAN
PN4860		2N4860JAN
PN4861		2N4861JAN
PN5114		2N5114
PN5115		2N5115
PN5116		2N5116
PN5432		2N5432
PN5433		2N5433
PN5434		2N5434
PN7000	2N7000	
SD210DE	SD210DE	
SD211DE	SD211DE	
SD214DE	SD214DE	
SD215DE	SD215DE	
SD5000J	SD5000N	
SD5001I	SD5000I	
SD5002I	SD5000I	
SD5001J	SD5001N	
SD5002J	SD5002N	
SD5002N	SD5000N	
SD5200I		SD5000I
SD5200N		SD5000N
SK3746/326		J305
SK3834/132		J211
SST203		SST202
SST204		SST201
SST4091		SST111
SST4092		SST112
SST4093		SST113
SST4856		SST4391
SST4857		SST4392
SST4858		SST4393
SST5484		SST305
SST5485		SST304
SST5486		SST304
SST5912		SST441
SSTDPAD10	SSTPAD5	
SSTDPAD20	SSTPAD5	
SSTDPAD50	SSTPAD5	
SSTPAD10	SSTPAD5	
SSTPAD20	SSTPAD5	
SSTPAD200	SSTPAD100	
SSTPAD500	SSTPAD100	
SU2098	2N5197	
SU2098B	2N5196	
TD5902	U421	
TD5903		U421
TD5904	U423	
TD5905	U421	
TD5906		U421
TD5907	U421	
TD5908		U421
TD5909	U423	
TN0102N2		VN0300L
TN0102N3		VN0300L
TN0520N2		VN2406L
TN0520N3		VN2410L
TN0524N3		VN2410L
TN4117A	2N4117A	
TN4118A	2N4118A	
TP0610E	TP0610L	
TP0610L	TP0610L	
TP0610T	TP0610T	
U183	2N4416	
U184	2N4416	
U198	2N4340	
U199		2N4341
U200		2N4393
U201		2N4392
U202		2N4391
U231	2N5197	
U232	2N5196	
U233	2N5199	
U234	2N5199	
U235	2N5199	
U240	2N5432	
U241	2N5433	
U242	2N5432	
U243	2N5433	
U248	U42402	
U249	U421	
U250		U421
U251	U423	
U257	2N5912	
U280		2N5197
U281		2N5197
U282		2N5196
U283		2N5196
U284		2N5199
U285		2N5199
U295		U290
U296		U291
U300		2N5114
U301		2N5115
U304	2N5114	
U305	2N5115	
U306	2N5116	
U311		U310
U320		2N5432
U321		2N5434
U322		2N5432

CROSS REFERENCE

Siliconix incorporated

INDUSTRY PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
U410		2N5197
U411		2N5198
U412		2N5199
U424	U421	
U425		U421
U426	U423	
U427		U421
U428	U423	
U1897		J111
U1898		J112
U1899		J112
U1994		J304
U1994E		J304-18
U2047E		2N4416
U2134		2N5199
U3000	2N4341	
U3001	2N4339	
U3002	2N4338	
U3010	2N4341	
U3011	2N4340	
U3012	2N4338	
VN0104N5		VN66AFD
VN0104N6		VQ1004J
VN0104N7		VQ1004P
VN0106N5		VN66AFD
VN0106N6		VQ1004J
VN0106N7		VQ1004P
VN0120N2		VN2406L
VN0120N3		VN2410L
VN0120N5	VN2406D	
VN0220N2		VN2406L
VN0220N3		VN2406L
VN0220N5		VN2406L
VN0350N3		VN3515L
VN0535N2		VN4012L
VN0535N3		VN3515L
VN0540N2		VN4012L
VN0540N3		VN4012L
VN0603L		2N7000
VN0603T		2N7002
VN0606L		VN0606M
VN10KMA	VN10KM	
VN10KN3		VN10LM
VN40AF		VN46AFD
VN40AFD	VN46AFD	
VN46AF		VN46AFD
VN66AF		VN66AFD
VN88AF		VN88AFD
VN89AB		2N6661
VN98AK	2N6661	
VN1206D	VN2406D	
VN1304N2		VN1206L
VN1304N3		VN1206L
VN1304N6		VQ1004J
VN1304N7		VQ1004P
VN1306N2		VN1206L
VN1306N3		VN1206L
VN1306N6		VQ1004J
VN1306N7		VQ1004P
VN1310N2		VN1206L
VN1310N3		VN1206L
VN1316N2		VN4012L
VN1316N3		BS107
VN1320N2		VN4012L
VN1320N3		BS107
VN1706D	VN2406D	
VN1706L	VN2406L	
VN1706M	VN2406M	
VN1710L	VN2410L	
VN1710M	VN2410M	
VN1720M	VN2410M	
VN2020L	VN2410L	
VN2222KM	VN10KM	
VN4010B		VN4012L
VN4010L		VN4012L
VP0104N3		TP0610L
VP0104N6		VQ2004J
VP0104N9		TP0610L
VP0106N3		TP0610L
VP0106N9		TP0610L
VP0116N2		VP2020L
VP0116N3		VP2020L
VP0120N2		VP2020L
VP0120N3		VP2020L
VP0204N2	VP0808B	
VQ7254P		VQ3001P
ZVN01A2A	VN0300L	
ZVN01A2L	VN0300L	
ZVN0102A	VN0300L	
ZVN0102B	VN0300L	
ZVN0102L	VN0300L	
ZVN0106L	VN66AFD	
ZVN0109B	2N6661	
ZVN0109L		VN88AFD
ZVN0110A	VN1206L	
ZVN0110B	VN1206L	
ZVN0110L	VN1206L	
ZVN0120A	VN2410L	
ZVN530A	VN3515L	
ZVN535A	VN3515L	
ZVN540A	VN4012L	
ZVN1304A	VN2222L	
ZVN1306A	VN0610L	
ZVN1308A	VN1210L	
ZVN1308B	VN1210L	
ZVN1309A	VN2410L	
ZVN1310A	VN2406L	
ZVN1314A	VN2410L	
ZVN1316A	VN2410L	
ZVN1320A	VN2410L	
ZVN1404A	VN0610L	
ZVN1406A	VN0610L	
ZVN1408A	VN2410L	
ZVN1409A	VN2410L	
ZVN1414A	VN2410L	
ZVN1416A	VN2410L	
ZVN3302A	VN0300L	
ZVN3302B		VN0300L
ZVN3304A	VN1206L	
ZVN3304B		VN1206L
ZVN3306B		VN1206L
ZVN3310A		VN1206L
ZVP0120A		BSS92
ZVP1306A		TP0610L
ZVP1306B		TP0610L
ZVP1308A		BSS92
ZVP1320A		BSS92
ZVP1408B	VP0808B	
ZVP1409B	VP1008B	
ZVP1410B	VP1008B	
ZVP3306A		TP0610L
1N5303		CR160

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CROSS REFERENCE

INDUSTRY PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
1N5304		CR180
1N5305		CR200
1N5306		CR220
1N5307		CR240
1N5308		CR270
1N5309		CR300
1N5310		CR330
1N5311		CR360
1N5312		CR390
1N5313		CR430
1N5314		CR470
2N2386		J177
2N2386A		J177
2N2497		J177
2N2498		J177
2N2499		J177
2N2500		J177
2N2606		J176
2N2607		J176
2N2841		J177
2N2842		J177
2N2843		J177
2N2844		J177
2N3066	2N4340	
2N3067	2N4338	
2N3068	2N4338	
2N3069	2N4341	
2N3070	2N4339	
2N3071	2N4338	
2N3084	2N4340	
2N3085	2N4340	
2N3086	2N4340	
2N3087	2N4340	
2N3088	2N4338	
2N3088A	2N4338	
2N3089	2N4338	
2N3089A	2N4338	
2N3112		J177
2N3328		J176
2N3329		J176
2N3330		J176
2N3331		J176
2N3332		J176
2N3365	2N4340	
2N3366	2N4338	
2N3367	2N4338	
2N3368	2N4341	
2N3369	2N4339	
2N3370	2N4340	
2N3376		J201
2N3378		J177
2N3380		J176
2N3382		J176
2N3384		J175
2N3386	2N5116	
2N3436	2N4341	
2N3437	2N4340	
2N3438	2N4338	
2N3452	2N4340	
2N3453	2N4338	
2N3454		J201
2N3455	2N4340	
2N3456	2N4338	
2N3457	2N4338	
2N3458	2N4341	
2N3820		J177

INDUSTRY PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
2N3921		U401
2N3922		U401
2N3954		2N5196
2N3954A		2N5196
2N3955		2N5197
2N3955A		2N5196
2N3956		2N5199
2N3957		2N5199
2N3958		2N5199
2N4084		U401
2N4085		U404
2N4091		2N4391
2N4091A	2N4391	
2N4092		2N4392
2N4092A	2N4392	
2N4093		2N4393
2N4093A	2N4393	
2N4094		2N4391
2N4095		2N4392
2N4117	2N4117A	
2N4118	2N4118A	
2N4119	2N4119A	
2N4120	3N163	
2N4220		2N4340
2N4220A		2N4340
2N4221		2N4341
2N4221A		2N4341
2N4222		2N4341
2N4222A		2N4341
2N4223		2N4416
2N4224		2N4416
2N4267	3N163	
2N4417		SST4416
2N4445	2N5432	
2N4446	2N5433	
2N4447	2N5432	
2N4448	2N5432	
2N4856		2N4391
2N4856A		2N4391
2N4857		2N4392
2N4857A		2N4392
2N4858		2N4393
2N4858A		2N4393
2N4859		2N4391
2N4859A		2N4391
2N4860		2N4392
2N4860A		2N4392
2N4861		2N4393
2N4861A		2N4393
2N4867		2N4338
2N4867A		2N4338
2N4868		2N4340
2N4868A		2N4340
2N4869		2N4341
2N4869A		2N4341
2N4977	2N5432	
2N4978	2N5433	
2N4979	2N5434	
2N5018		2N5114
2N5019		2N5116
2N5045		2N5196
2N5046		2N5196
2N5047		2N5197
2N5361		2N4341
2N5362		2N4341
2N5398		J212

CROSS REFERENCE

Siliconix incorporated

INDUSTRY PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
2N5452		2N5196
2N5453		2N5198
2N5454		2N5199
2N5456		2N4340
2N5457		J202
2N5458		J202
2N5459		J202
2N5515		2N5196
2N5516		2N5197
2N5517		2N5198
2N5518		2N5199
2N5519		2N5199
2N5520		2N5196
2N5521		2N5197
2N5522		2N5198
2N5523		2N5199
2N5524		2N5199
2N5543		2N5197
2N5544		2N5197
2N5545		2N5199
2N5546		2N5198
2N5547		2N5199
2N5549		2N4392
2N5556	2N4339	
2N5561	U401	
2N5562		U401
2N5563	U404	
2N5564	2N5564	
2N5565	2N5565	
2N5566	2N5566	
2N5592	2N4341	
2N5593	2N4341	
2N5594	2N4341	
2N5638		J111
2N5639		J112
2N5640		J113
2N5647	2N4117A	
2N5648	2N4117A	
2N5649	2N4117A	
2N5653	J112	
2N5654		J111
2N5902		U404
2N5903		U421
2N5904		U421
2N5905		U423
2N5906		U421
2N5907		U421
2N5908		U421
2N5909		U423
2N5952	J305-18	
2N5953	J305-18	
2N6451	2N4393	
2N6452	2N4393	
2N6453	2N4393	
2N6454	2N4393	
2N6483	U401	
2N6484		U401
2N6485	U404	
2N6659/750	2N6659-2	
2N6660/750	2N6660-2	
2N6661/750	2N6661-2	
2N6905		U401
2N6905A		U401
2N6906		U401
2N6906A		U401
2N6907		U404
2N6907A		U404
2N7008	2N7000	
2N7009		VN50300L
2N7019	VP0610T	
2N7020		ND2020L
2N7022		VN4012L
2N7023		VP2020L
2N7024		ND2410L
2N7025		TP0610L
2N7026	TP0610T	
2N7027		TP0610L
2N7030		VP2410L
2N7104	SD210DE	
2N7105	SD211DE	
2N7106	SD210DE	
2N7107	SD211DE	
2N7108	SD214DE	
2N7109	SD215DE	
2N7116	SD5000I	
2N7117	SD5000I	
2N7118	SD5000I	
2SK13		2N4340
2SK15		2N4340
2SK19BL		J309
2SK19GR		J304
2SK19Y		2N5485
2SK23A-8		2N5485
2SK23A-9		2N4416A
2SK25		2N5486
2SK30		J210
2SK30AGR		2N4341
2SK30AO		2N4339
2SK30AR		2N4338
2SK30ATM		J211
2SK30AY		2N4340
2SK33		J304
2SK35		J210
2SK37		2N5484
2SK39		PN4119A
2SK39A		PN4119A
2SK40		2N4339
2SK40B		2N4339
2SK40C		2N4340
2SK41		2N5486
2SK41C		2N5484
2SK41D		2N5484
2SK41E		2N5484
2SK41F		2N5485
2SK42		2N5484
2SK43S		J113
2SK43S-D		J113
2SK47		2N5484
2SK49		2N5484
2SK49E		2N5484
2SK49F		2N5484
2SK49H		2N5484
2SK54		2N5484
2SK54B		2N5484
2SK54C		2N5484
2SK55		2N5485
2SK55D		2N5485
2SK55E		2N5485
2SK56		2N5484
2SK57		2N5484
2SK58		U441
2SK61		2N5484

Siliconix incorporated

CROSS REFERENCE

INDUSTRY PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
2SK85		J201
2SK86		J202
2SK87		SST201
2SK87A		SST201
2SK88		2N4341
2SK88A		2N4341
2SK93		2N5484
2SK93		PN4119A
2SK94		SST202
2SK97		SST406
2SK103		SST201
2SK107		J304
2SK108		PN4392
2SK109		U404
2SK113		2N4393
2SK117		2N4341
2SK118		2N4340
2SK119		2N4340
2SK120		2N5484
2SK121		J210
2SK123		SST201
2SK125		J310
2SK148		2N5485
2SK149		J309
2SK150		U404
2SK154		2N5485
2SK155		J309
2SK156A		PN4118A
2SK156B		PN4119A
2SK156C		PN4119 A
2SK157		SST202
2SK158		2N4340
2SK160		SST202
2SK161		2N5485
2SK163		J113
2SK165		J309
2SK168D		2N5485
2SK168E		J304
2SK168F		2N5486
2SK185		2N5566
2SK192ABL		2N5486
2SK192AGR		2N5484
2SK192AY		2N5484
2SK193EF		2N5484
2SK193FF		2N5484
2SK193KF		2N5484
2SK193LF		2N5484
2SK193MF		2N5485
2SK193PF		2N5484
2SK193UF		J201
2SK195E		2N5484
2SK195F		2N5484
2SK195H		2N5484
2SK195J		2N5485
2SK197C		SST202
2SK197D		SST4416
2SK197E		SST4416
2SK199		2N5485
2SK208		SST202
2SK209		SST4416
2SK210BL		SST309
2SK210GR		SST4416
2SK210Y		SST4416
2SK211		SST4416
2SK212C		2N5484
2SK212D		2N5484
2SK212E		2N5484
2SK212F		2N5484
2SK217C		SST202
2SK217D		SST4416
2SK217E		SST4416
2SK238K14		SST202
2SK238K15		SST202
2SK238K16		SST4416
2SK238K17		SST4416
2SK242C		SST202
2SK242D		SST202
2SK242E		SST4416
2SK242F		SST4416
2SK266		PN4119A
2SK270		U404
2SK292		2N5484
2SK314		2N4416A
2SK315E		2N5484
2SK315F		2N5485
2SK315G		J211
2SK330GR		J202
2SK330Y		J202
2SK331		SST201
2SK334		SST201
2SK370		J109
2SK374		2N4341
2SK376		PN4119A
2SK377		SST201
2SK381		J113
2SK389		SST405
2SK404		2N5485
2SK425		SST4416
2SK426		SST4416
2SK507		J308
2SK508		SST308

This Cross Reference material is accurate to the best knowledge and belief of Siliconix, incorporated. Since individual circuit design and layout can influence device performance, the purchaser must be responsible for the ultimate selection and determination of interchangeability.

Selector Guide 3

SELECTOR GUIDE

INTRODUCTION

Siliconix' line of small-signal transistors includes JFETs, MOSFETs, and DMOS FETs. Since the company's founding in 1962, Siliconix has been a leading supplier of small-signal FETs for military and industrial applications. We have focused on high-performance areas where FETs add value to a system due to important features such as extremely low noise, sub-picoamp leakages, nanosecond switching times, and high slew rates.

JFETs: We offer the world's broadest selection of JFETs, including all of the most popular functions and performance specifications. Our new focused selection, which is shown in this catalog, now allows us to offer you more efficient service, including faster quote turnaround and on-time delivery.

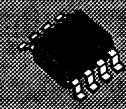
DMOS FETs: To enhance the performance levels of our FET line, Siliconix offers FETs made with our proprietary silicon-gate DMOS technology. Featuring sub-nanosecond switching speeds and near gigahertz amplifier capabilities, DMOS FETs bridge the performance gap between conventional FETs and devices made with gallium arsenide.

MOSFETs: Advances in our fabrication process for small-signal MOSFETs have allowed us to streamline our product offerings by eliminating low-performance products and cost-effectively providing "prime" performance in all the popular MOSFET geometries. In addition, we have recently added two new product options: fifteen new MOSFETs that feature low threshold voltages and low on-resistance, and a new family of electrically isolated MOSFET pairs housed in SO-8 surface-mount packages. The low-threshold devices are TTL and CMOS compatible; they are well suited for low-current, cost-sensitive applications, and they make excellent drivers for larger MOSFETs and small motors. Like our popular Si9950DY half-bridges, the new SO-8 packaged devices provide two of our reliable discrete MOSFETs in a compact package, creating a space-saving solution for low-power motor control circuits.

Siliconix incorporated

JFET SELECTOR GUIDE

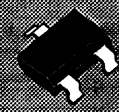
SO-8



Description	Channel	Max. Off-Set (mV)	Part Number
Dual Low-Noise JFET	N	15	SST404
Dual Low-Noise JFET	N	40	SST406
Dual High-Gain JFET	N	10	SST440
Dual High-Gain JFET	N	20	SST441

Description	Max. Reverse Current (pA)	Part Number
Low-Leakage Diode	-5	SSTDPAD5
Low-Leakage Diode	-100	SSTDPAD100

SOT-23



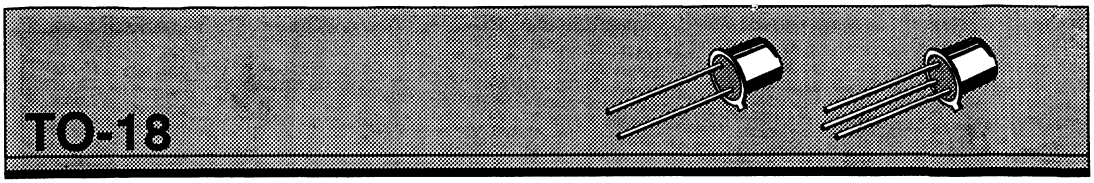
Description	Channel	Max. $r_{DS(ON)}$ (Ω)	Part Number
Analog Switch	N	8	SST108
Analog Switch	N	12	SST109
Analog Switch	N	18	SST110
Analog Switch	N	30	SST111
Analog Switch	N	50	SST112
Analog Switch	N	100	SST113
Analog Switch	P	85	SST174
Analog Switch	P	125	SST175
Analog Switch	P	250	SST176
Analog Switch	P	300	SST177
Analog Switch	N	30	SST4391
Analog Switch	N	60	SST4392
Analog Switch	N	100	SST4393

Description	Channel	I_{DSS} Min. (mA)	Part Number
High-Frequency Amplifier	N	5	SST304
High-Frequency Amplifier	N	1	SST305
High-Frequency Amplifier	N	12	SST308
High-Frequency Amplifier	N	12	SST309
High-Frequency Amplifier	N	24	SST310
Low-Noise Amplifier	N	0.2	SST201
Low-Noise Amplifier	N	0.9	SST202
Low-Noise Amplifier	N	5	SST4416

Description	Max. Reverse Current (pA)	Part Number
Low-Leakage Diode	-5	SSTPAD5
Low-Leakage Diode	-100	SSTPAD100

3

TO-18



Description	Channel	Min. I_{DSS} (mA)	Part Number
Low-Noise Amplifier	N	0.2	2N4338
Low-Noise Amplifier	N	0.5	2N4339
Low-Noise Amplifier	N	1.2	2N4340
Low-Noise Amplifier	N	3	2N4341

Description	Channel	Max. $r_{DS(ON)}$ (Ω)	Part Number
Analog Switch	N	30	2N4091 J
Analog Switch	N	50	2N4092 J
Analog Switch	N	80	2N4093 J
Analog Switch	N	30	2N4391
Analog Switch	N	60	2N4392
Analog Switch	N	100	2N4393
Analog Switch	N	25	2N4856 J
Analog Switch	N	40	2N4857 J
Analog Switch	N	60	2N4858 J
Analog Switch	N	25	2N4859 J
Analog Switch	N	40	2N4860 J
Analog Switch	N	60	2N4861 J
Analog Switch	P	75	2N5114 J
Analog Switch	P	100	2N5115 J
Analog Switch	P	150	2N5116 J

J = JAN, JANTX, JANTXV

Description	Max. Reverse Current (pA)	Part Number
Low-Leakage Diode	-1	PAD1 (TO-72)
Low-Leakage Diode	-5	PAD5 (TO-72)
Low-Leakage Diode	-50	PAD50

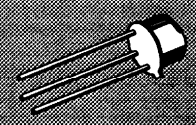
Description	Nominal Regulator Current (mA)	Part Number
Current Limiter	1.60	CR160
Current Limiter	1.80	CR180
Current Limiter	2.00	CR200
Current Limiter	2.20	CR220
Current Limiter	2.40	CR240
Current Limiter	2.70	CR270
Current Limiter	3.00	CR300
Current Limiter	3.30	CR330
Current Limiter	3.60	CR360
Current Limiter	3.90	CR390
Current Limiter	4.30	CR430
Current Limiter	4.70	CR470

Description	Channel	Min. $r_{DS(ON)}$ (Ω)	Max. $r_{DS(ON)}$ (Ω)	Part Number
Voltage-Controlled Resistor	N	20	60	VCR2N
Voltage-Controlled Resistor	N	200	600	VCR4N
Voltage-Controlled Resistor	N	4000	8000	VCR7N (TO-72)

Siliconix incorporated

JFET SELECTOR GUIDE

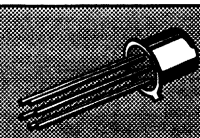
TO-52 (TO-206AC)



Description	Channel	Min. I_{DSS} (mA)	Part Number
High-Frequency Amplifier	N	12	U309
High-Frequency Amplifier	N	24	U310

Description	Channel	Min. $V_{GS(OFF)}$ (V)	Part Number
Analog Switch	N	-4	U290
Analog Switch	N	-1.5	U291
Analog Switch	N	-4	2N5432
Analog Switch	N	-3	2N5433
Analog Switch	N	-1	2N5434

TO-71



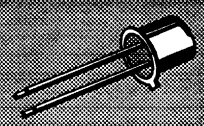
Description	I_{DSS} Min. (mA)	Max. Off-Set (mV)	Part Number
Dual Low-Noise Amplifier	0.5	5	U401
Dual Low-Noise Amplifier	0.5	15	U404
Dual Low-Noise Amplifier	0.5	40	U406
Dual High-Gain Amplifier	5	5	2N5564
Dual High-Gain Amplifier	5	10	2N5565
Dual High-Gain Amplifier	5	20	2N5566
Dual High-Frequency Amplifier	6	10	U440
Dual High-Frequency Amplifier	6	20	U441

Description	Max. Reverse Current (pA)	Part Number
Low-Leakage Diode	-5	DPAD5
Low-Leakage Diode	-50	DPAD50

Description	I_{DSS} Min. (mA)	Max. (mV) Off-Set	Part Number
Dual Amplifier	0.7	5	2N5196
Dual Amplifier	0.7	5	2N5197
Dual Amplifier	0.7	10	2N5198
Dual Amplifier	0.7	15	2N5199

3

TO-72 (TO-206AF)



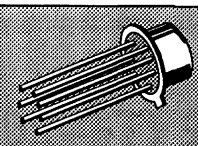
Description	Channel	I_{DSS} Min. (mA)	Part Number
Low-Leakage Amplifier	N	0.015	2N4117A
Low-Leakage Amplifier	N	0.08	2N4118A
Low-Leakage Amplifier	N	0.2	2N4119A

Description	Channel	I_{DSS} Min. (mA)	Part Number
Low-Noise Amplifier	N	5	2N4416
Low-Noise Amplifier	N	5	2N4416A

JFET SELECTOR GUIDE

Siliconix incorporated

TO-78

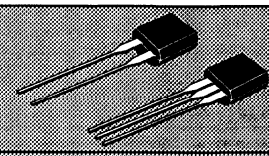


Description	Max. Offset (mV)	Part Number
Dual Low-Leakage JFET	10	U421
Dual Low-Leakage JFET	25	U423

Description	Max. Reverse Current (pA)	Part Number
Low Leakage Diode	-1	DPAD1

Description	Max. Offset (mV)	Part Number
Dual High-Frequency Amplifier	10	2N5911
Dual High-Frequency Amplifier	15	2N5912
Dual High-Frequency, Low-Noise Amplifier	-	U430
Dual High-Frequency, Low-Noise Amplifier	-	U431

TO-92 (TO-226AA)



Description	Nominal Regulator Current (mA)	Part Number
Current Limiter	0.24	J500
Current Limiter	0.33	J501
Current Limiter	0.43	J502
Current Limiter	0.56	J503
Current Limiter	0.75	J504
Current Limiter	1	J505
Current Limiter	1.4	J506
Current Limiter	1.8	J507
Current Limiter	2.4	J508
Current Limiter	3	J509
Current Limiter	3.6	J510
Current Limiter	4.7	J511

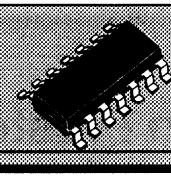
Description	Channel	Max. $V_{GS(OFF)}$ (V)	Part Number
Analog Switch	N	-10	J105
Analog Switch	N	-6	J106
Analog Switch	N	-4.5	J107
Analog Switch	N	-10	J108
Analog Switch	N	-6	J109
Analog Switch	N	-4	J110
Analog Switch	N	-10	J111
Analog Switch	N	-5	J112
Analog Switch	N	-3	J113
Analog Switch	P	10	J174
Analog Switch	P	6	J175
Analog Switch	P	4	J176
Analog Switch	P	2.25	J177

Description	Channel	Min. I_{DSS} (mA)	Part Number
Low-Noise Amplifier	N	0.2	J201
Low-Noise Amplifier	N	0.9	J202
Low-Leakage Amplifier	N	0.03	PN4117A
Low-Leakage Amplifier	N	0.08	PN4118A
Low-Leakage Amplifier	N	0.2	PN4119A
Analog Switch	N	-4	PN4391
Analog Switch	N	-2	PN4392
Analog Switch	N	5	PN4393
High-Frequency Amplifier	N	1	2N5484
High-Frequency Amplifier	N	4	2N5485
High-Frequency Amplifier	N	8	2N5486
High-Frequency Amplifier	N	2	J210
High-Frequency Amplifier	N	7	J211
High-Frequency Amplifier	N	15	J212
High-Frequency Amplifier	N	5	J304
High-Frequency Amplifier	N	1	J305
High-Frequency Amplifier	N	12	J308
High-Frequency Amplifier	N	12	J309
High-Frequency Amplifier	N	24	J310

Description	Max. Reverse Current (pA)	Part Number
Low-Leakage Diode	-5	JPAD5
Low-Leakage Diode	-50	JPAD50

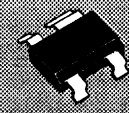
DMOS FET SELECTOR GUIDE

SO-14



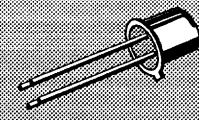
Part Number	Max. $r_{DS(ON)}$ (Ω)	Max. C_{rss} (pF)	Max. t_{ON} (ns)
SD5400CY	70	0.5	2
SD5401CY	70	0.5	2

SOT-143



Part Number	Max. $r_{DS(ON)}$ (Ω)	Max. C_{rss} (pF)	Max. t_{ON} (ns)
SST211	75	0.5	2
SST215	75	0.5	2

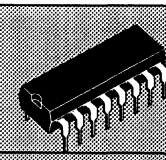
TO-72 (TO-206AF)



Part Number	Max. $r_{DS(ON)}$ (Ω)	Max. C_{rss} (pF)	Max. t_{ON} (ns)
SD210DE	70	0.5	2
SD211DE	70	0.5	2

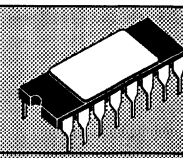
Part Number	Max. $r_{DS(ON)}$ (Ω)	Max. C_{rss} (pF)	Max. t_{ON} (ns)
SD214DE	70	0.5	2
SD215DE	70	0.5	2
SD2100	50	2	2

16-Pin Plastic DIP



Part Number	Max. $r_{DS(ON)}$ (Ω)	Max. C_{rss} (pF)	Max. t_{ON} (ns)
SD5000N	70	0.5	2
SD5001N	70	0.5	2

16-Pin Sidebraze DIP

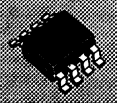


Part Number	Max. $r_{DS(ON)}$ (Ω)	Max. C_{rss} (pF)	Max. t_{ON} (ns)
SD5000I	70	0.5	2

Siliconix incorporated

MOSFET SELECTOR GUIDE

SO-8



Channel	Min. $V_{(BR)DSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
P	-30	2.0	-4.5	TD2001Y
N	30	1.5	2.0	TD1001Y

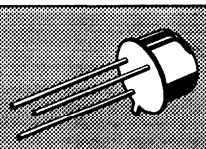
Channel	Min. $V_{(BR)DSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
N	60	2	2.0	TD1004Y
N/P	60	5/10	2.5/2.5	TD3002Y

SOT-23

Channel	Min. $V_{(BR)DSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
P	-60	10	-2.4	TP0610T
P	-60	10	-3.5	VP0610T
N	60	7.5	2.5	2N7002
N	60	5	3	VN0605T

Channel	Min. $V_{(BR)DSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
N	240	60	1.8	TN2460T
N	500	300	4.5	VN50300T

TO-39 (TO-205AD)

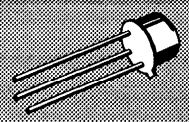


Channel	Min. $V_{(BR)DSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
P	-100	5	-4.5	VP1008B
P	-80	5	-4.5	VP0808B
P	-30	2.5	-4.5	VP0300B
N	35	1.8	2.0	2N6659

Channel	Min. $V_{(BR)DSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
N	60	3	2.0	2N6660 J
N	90	4	2.0	2N6661 J

J = JAN , JANTX, JANTXV

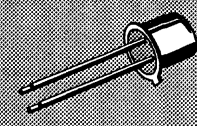
TO-52 (TO-206AC)



Channel	Min. $V_{(BR)DSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
N	60	5	2.5	VN10KE

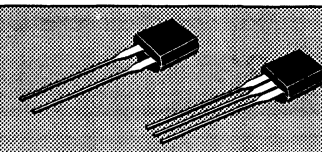
3

TO-72 (TO-206AF)



Channel	Min. $V_{(BR)GSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
P	-40	250	-5	3N163
P	-30	300	-5	3N164

TO-92 (TO-226AA)



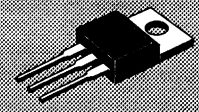
Min. $V_{(BR)GSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Channel	Part Number
-240	10	-2.4	P	TP2410L
-240	10	-2.5	P	VP2410L
-200	10	-2.4	P	TP2010L
-200	20	-2.4	P	TP2020L
-200	20	-2.5	P	VP2020L
-120	20	-2.4	P	TP1220L
-100	5	-4.5	P	VP1008L
-80	5	-4.5	P	VP0808L
-60	10	-2.4	P	TP0610L
-60	10	-3.5	P	VP0610L
-30	2.5	-4.5	P	VP0300L
20	2	2.0	N	TN0201L
30	1.2	2.5	N	VN0300L
40	2	2.0	N	TN0401L
60	5	3.0	N	2N7000
60	3	2.0	N	TN0601L
60	5	2.5	N	VN0610L
60	5	2.5	N	VN0610LL
60	7.5	2.5	N	VN2222L

Min. $V_{(BR)GSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Channel	Part Number
60	7.5	2.5	N	VN2222LL
120	6	2.0	N	TN1206L
120	6	2.0	N	VN1206L
120	10	2.0	N	VN1210L
200	12	-4.0	N	ND2012L
200	20	-2.5	N	ND2020L
200	10	1.8	N	TN2010L
200	10	1.8	N	VN2010L
240	6	-4.5	N	ND2406L
240	10	-2.5	N	ND2410L
240	10	1.8	N	TN2410L
240	6	2.0	N	VN2406L
240	10	2.0	N	VN2410L
350	12	1.8	N	TN3512L
350	15	1.8	N	VN3515L
400	12	1.8	N	TN4012L
400	12	1.8	N	VN4012L
500	300	4.5	N	VN50300L

Siliconix incorporated

MOSFET SELECTOR GUIDE

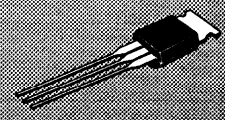
TO-220AB



Channel	Min. $V_{(BR)GSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
N	40	3	2.5	VN46AFD
N	60	3	2.5	VN66AFD

Channel	Min. $V_{(BR)GSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
N	80	4	2.5	VN88AFD
N	240	6	2.0	VN2406D

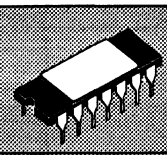
TO-237

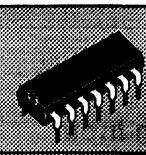


Channel	Min. $V_{(BR)GSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
P	-100	5	-4.5	VP1008M
P	-80	5	-4.5	VP0808M
P	-30	2.5	-4.5	VP0300M
N	30	1.2	2.5	VN0300M
N	60	3	2.0	VN0606M
N	60	5	2.5	VN10KM
N	60	5	2.5	VN10LM

Channel	Min. $V_{(BR)GSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
N	60	7.5	2.5	VN2222LM
N	80	4	2.0	VN0808M
N	120	6	2.0	VN1206M
N	120	10	2.0	VN1210M
N	240	6	2.0	VN2406M
N	240	10	2.0	VN2410M

14-Pin Sidebraze & Plastic DIPs

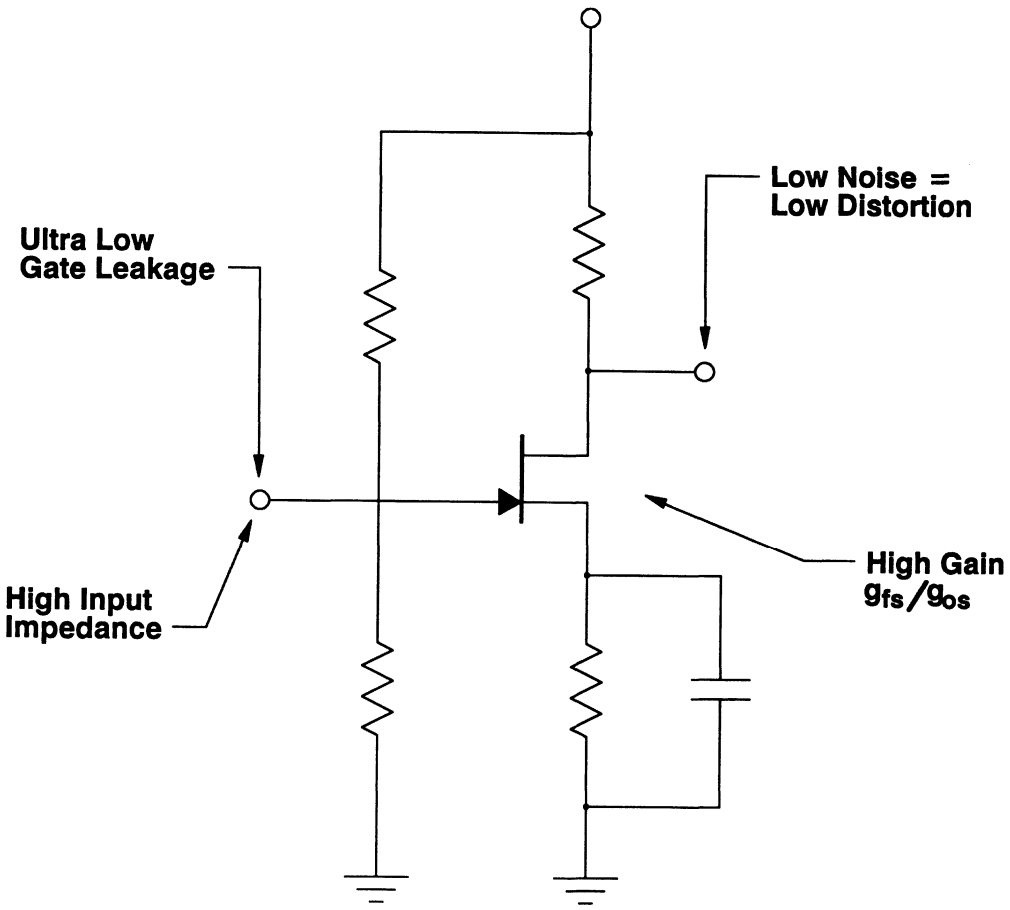




Channel	Min. $V_{(BR)GSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
N	-90	5	-4.5	VQ2006J
N	-60	5	-4.5	VQ2004J
N	-30	2	-4.5	VQ2001J
N	-30	2	-4.5	VQ2001P
N	20	3	-	VQ7254J
N	30	1.2	2.0	TQ1001J
N	30	1	2.5	VQ1001J
N	30	1	2.5	VQ1001P
N/P	30	1/2	-4.5	VQ3001J

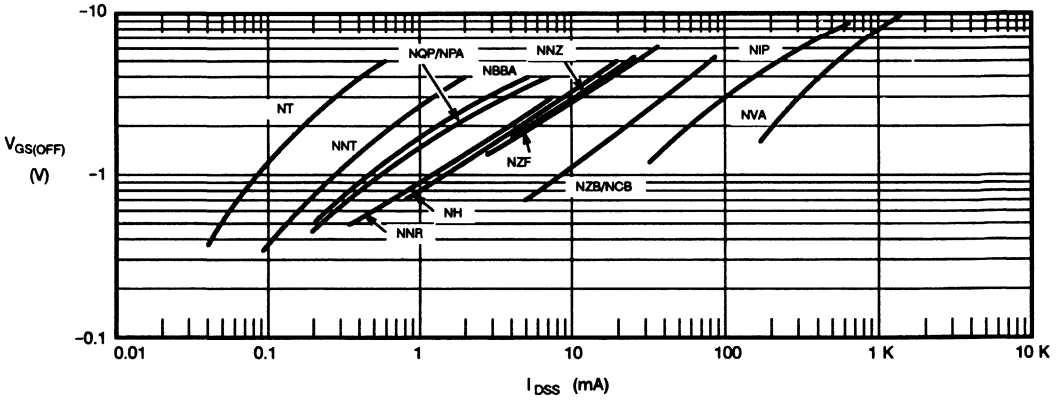
Channel	Min. $V_{(BR)GSS}$ (V)	Max. $r_{DS(ON)}$ (Ω)	Max. $V_{GS(th)}$ (V)	Part Number
N/P	30	1/2	-4.5	VQ3001P
N	60	2	2	TQ1004J
N	60	5.5	2.5	VQ1000J
N	60	5.5	2.5	VQ1000P
N	60	3.5	2.5	VQ1004J
N	60	3.5	2.5	VQ1004P
N	90	4.5	2.5	VQ1006J
N	90	4.5	2.5	VQ1006P

JFET AMPLIFIERS

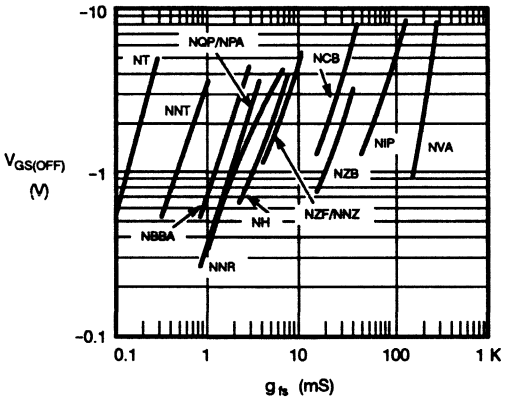


N-CHANNEL GEOMETRY TYPICALS

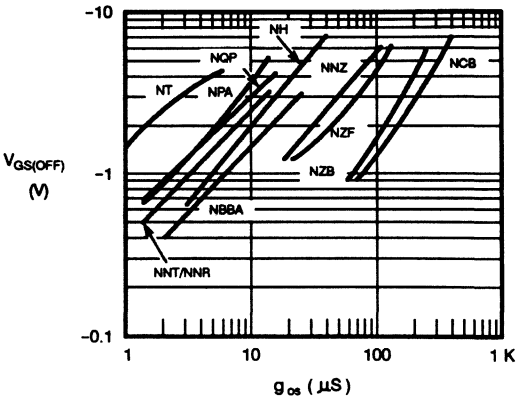
Cutoff Voltage vs. Drain Current



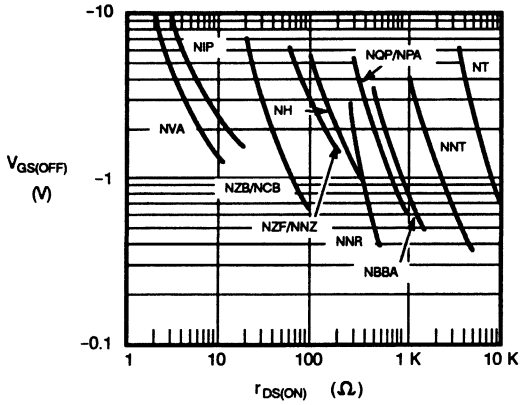
Cutoff Voltage vs. Common-Source Forward Transconductance



Cutoff Voltage vs. Common-Source Output Conductance

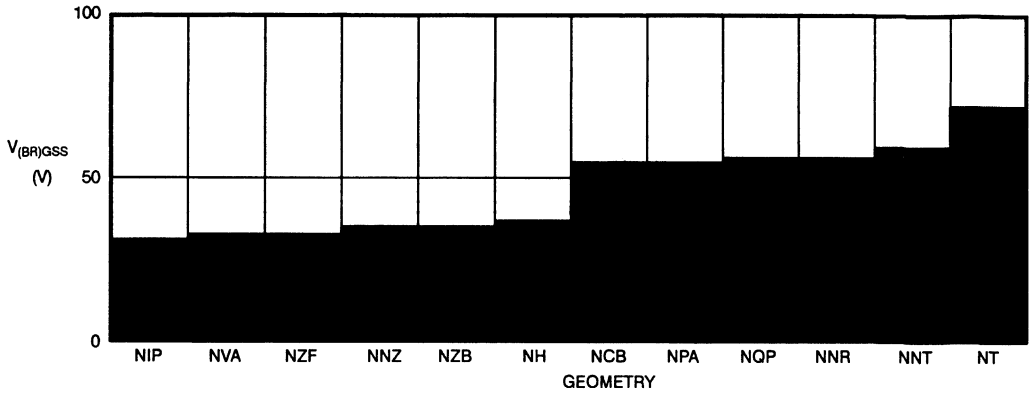


Cutoff Voltage vs. On-Resistance

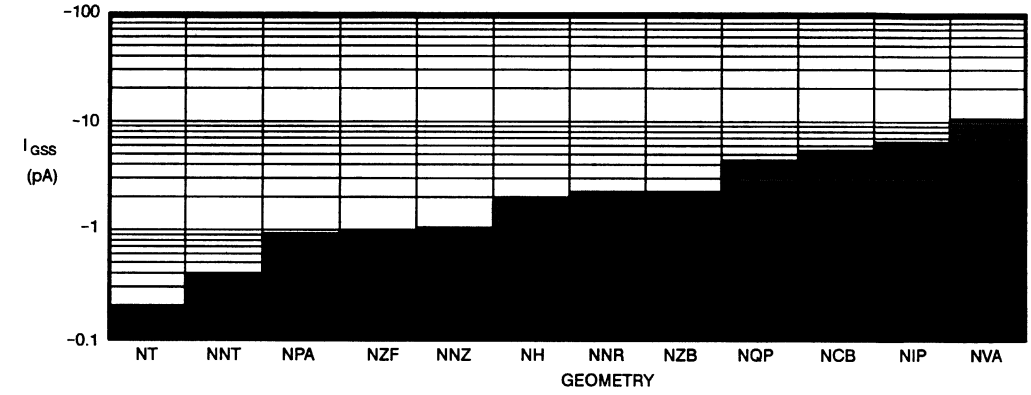


3

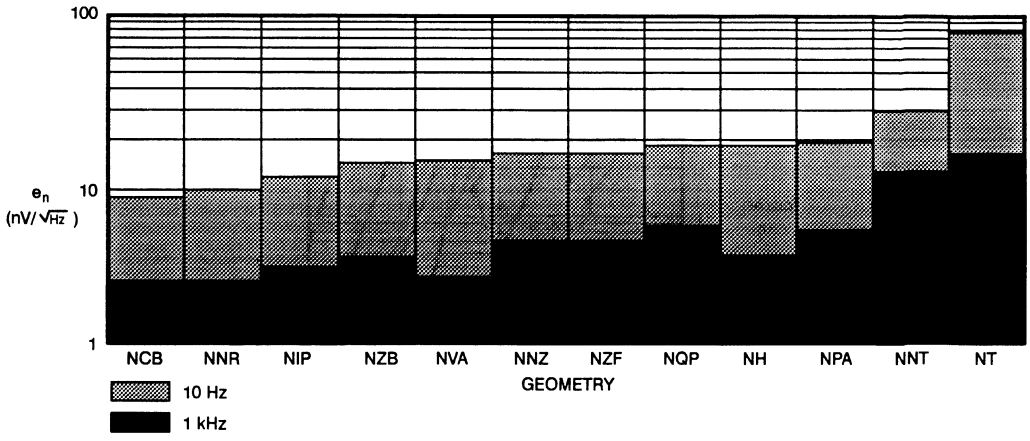
Gate-Source Breakdown Voltage vs. Geometry



Gate Leakage vs. Geometry

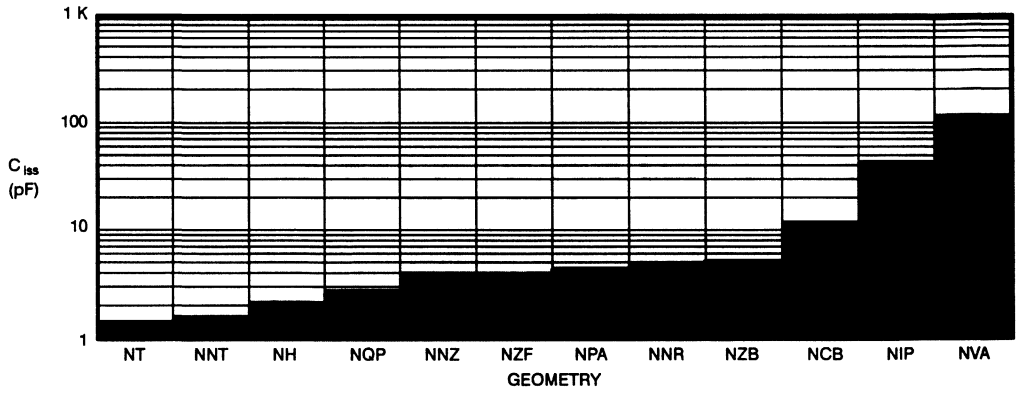


Noise Voltage vs. Geometry

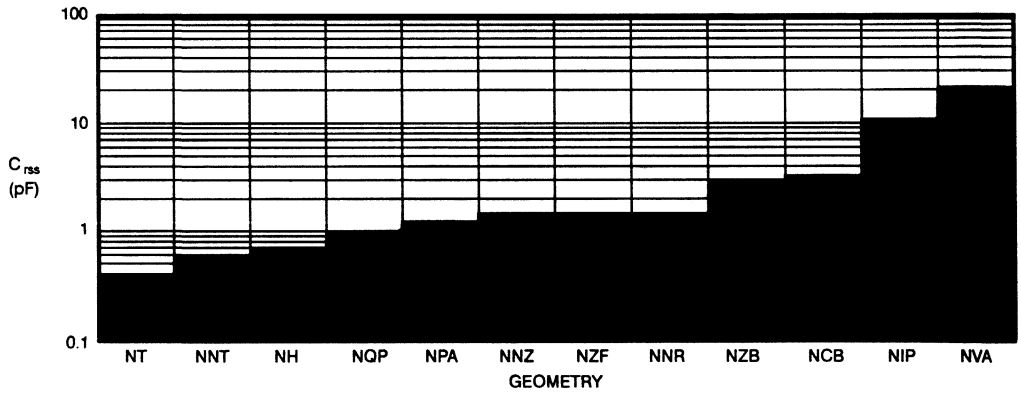


N-CHANNEL GEOMETRY TYPICALS

Input Capacitance vs. Geometry



Reverse-Transfer Capacitance vs. Geometry



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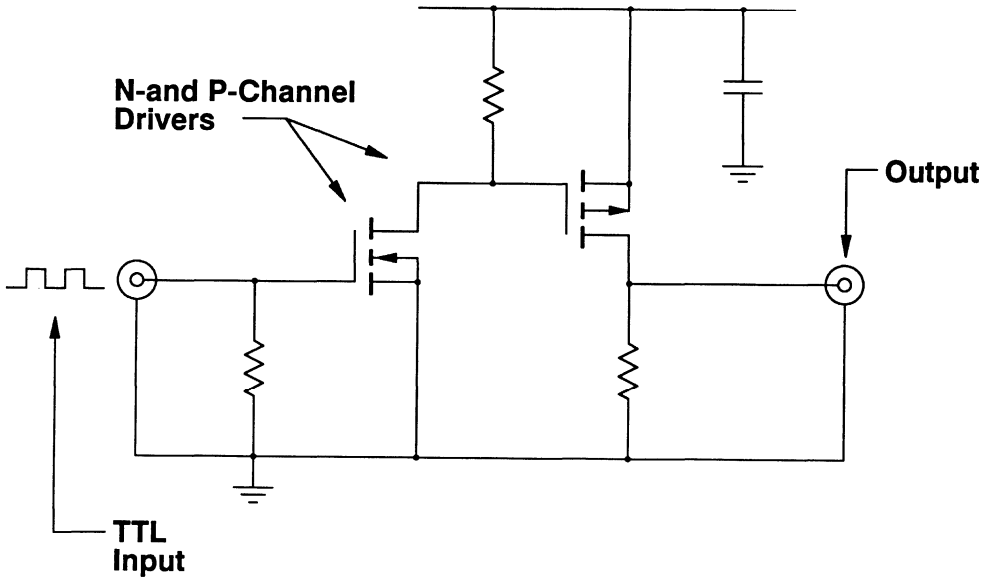
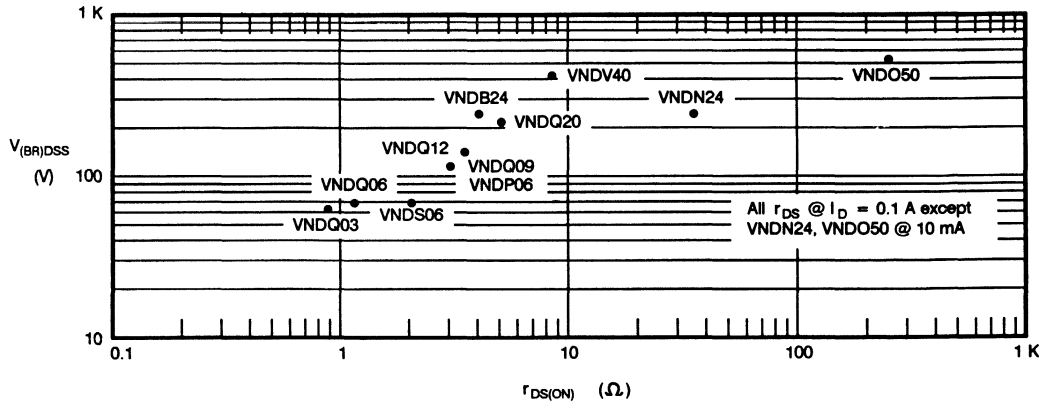
LOW POWER MOS

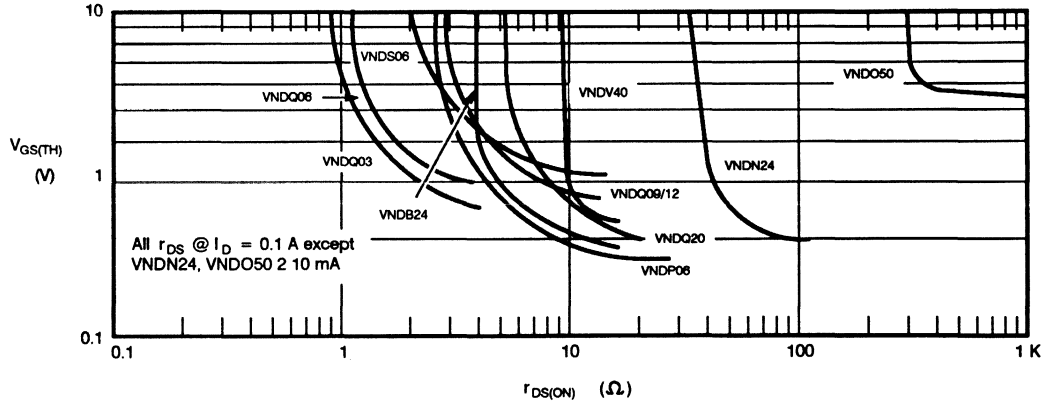


N-CHANNEL GEOMETRY TYPICALS

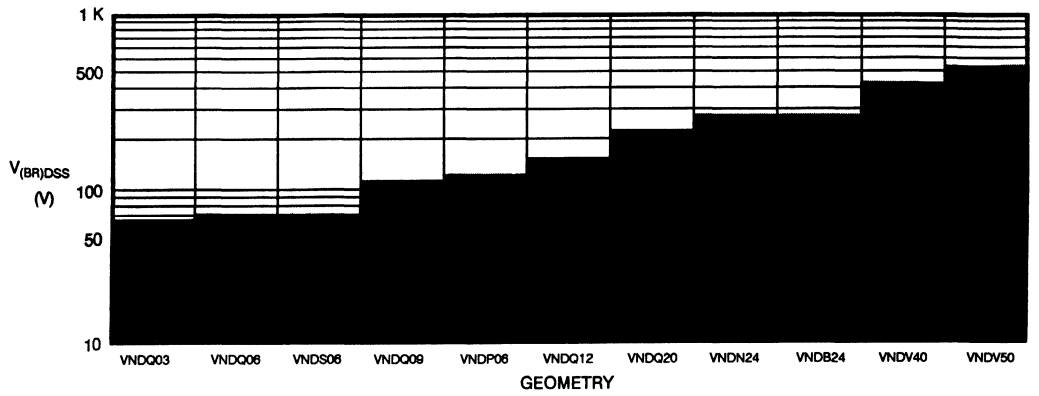
On-Resistance vs. Drain-Source Breakdown Voltage



Gate-Source Voltage vs. On-Resistance



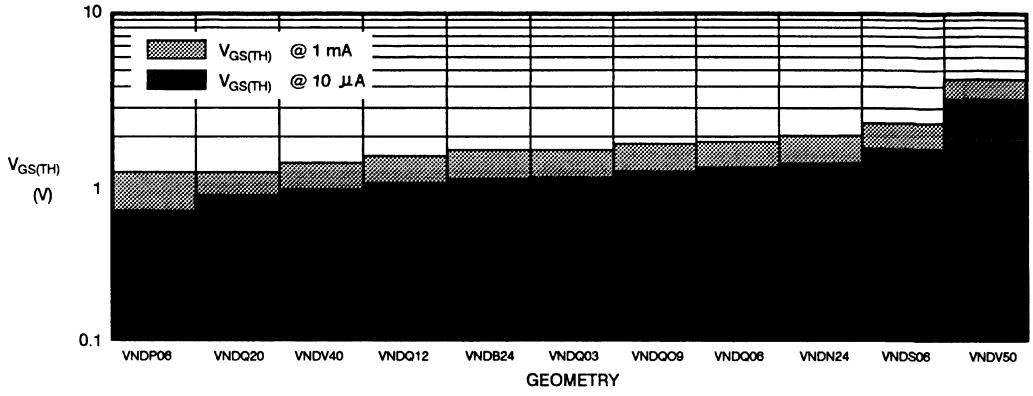
Drain-Source Breakdown Voltage vs. Geometry



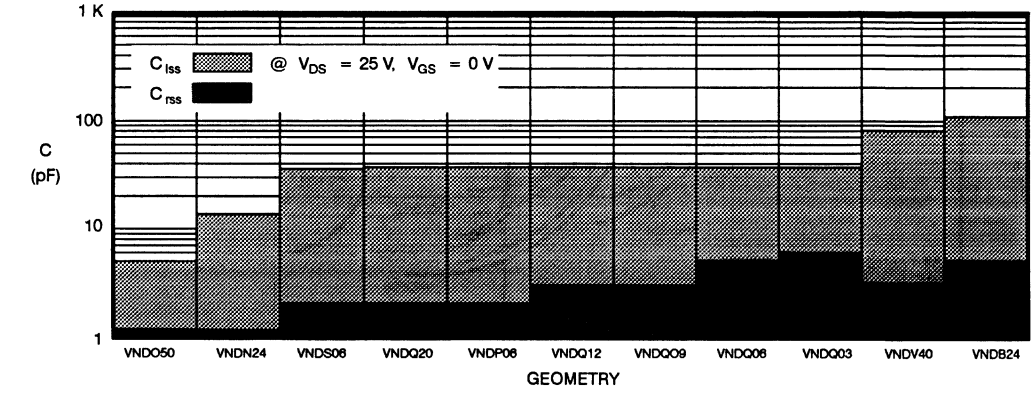
3

N-CHANNEL GEOMETRY TYPICALS

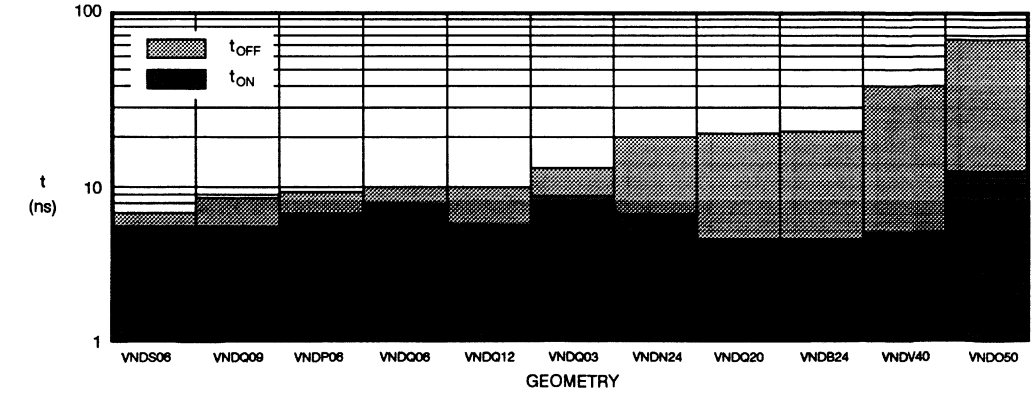
Gate-Source Threshold Voltage vs. Geometry



Capacitance vs. Geometry

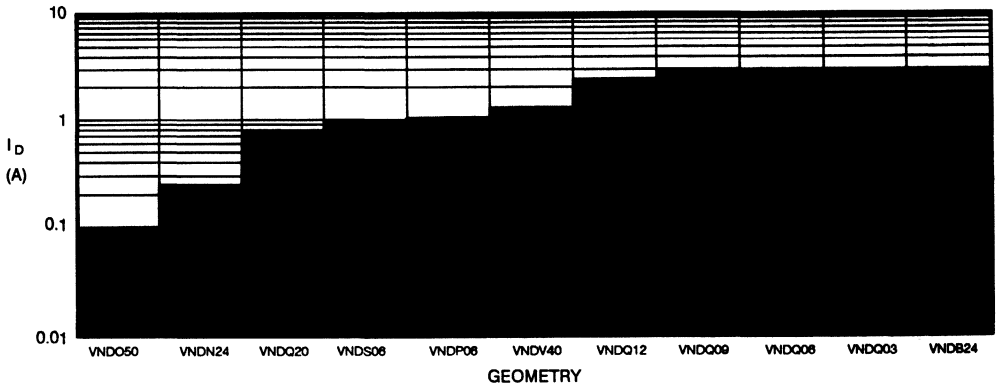


Typical Switching Time vs. Geometry



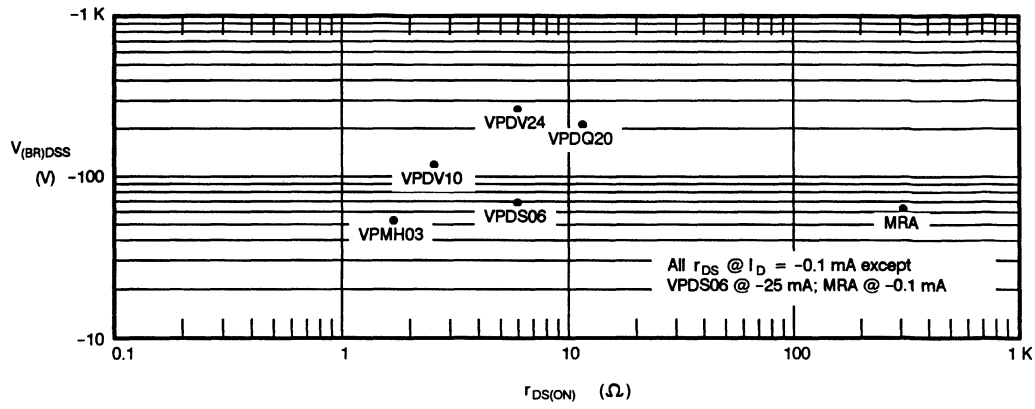
N-CHANNEL GEOMETRY TYPICALS

Maximum Drain Current vs. Geometry

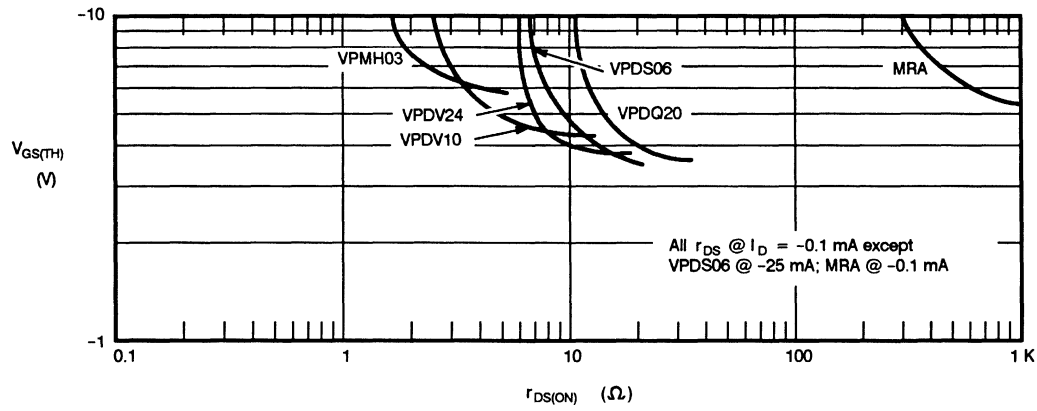


P-CHANNEL GEOMETRY TYPICALS

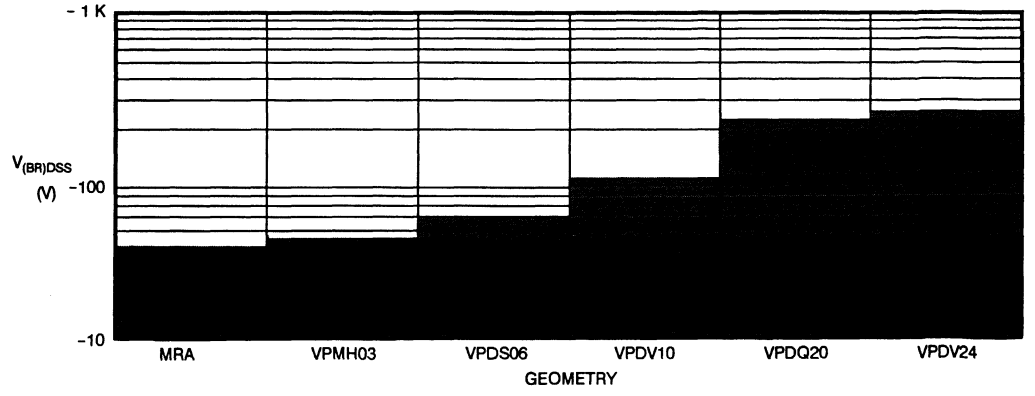
On-Resistance vs. Drain-Source Breakdown Voltage



On-Resistance vs. Gate-Source Voltage

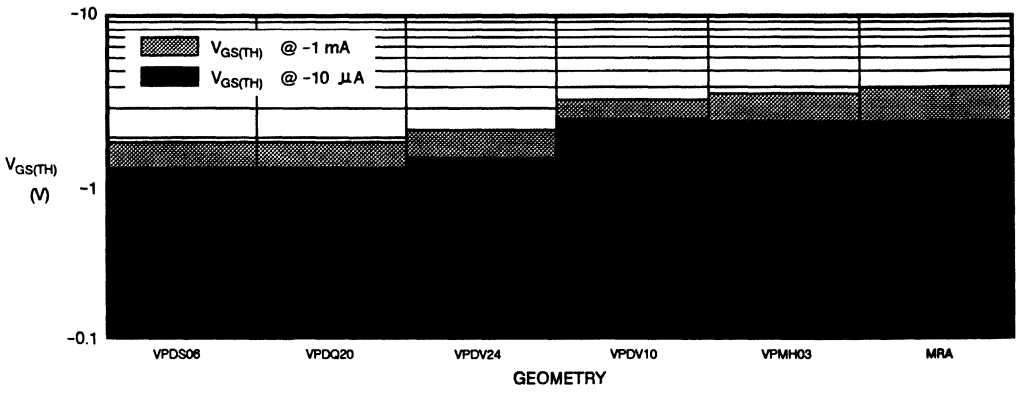


Drain-Source Breakdown Voltage vs. Geometry

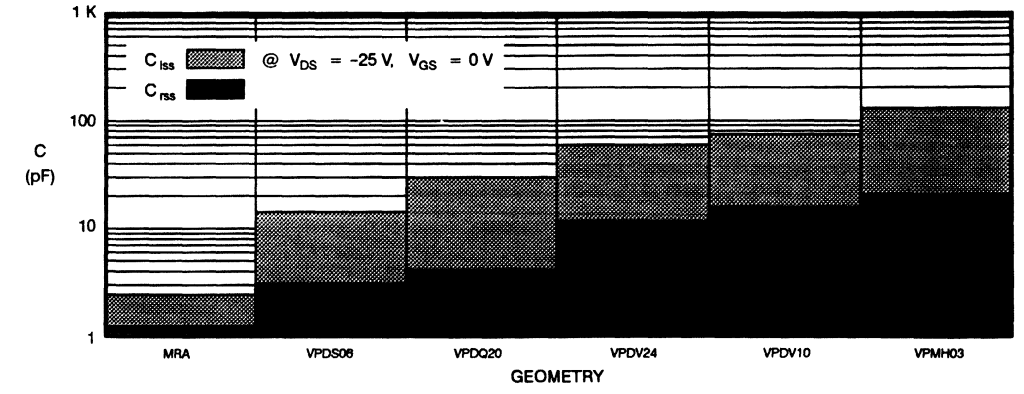


P-CHANNEL GEOMETRY TYPICALS

Gate-Source Threshold Voltage vs. Geometry

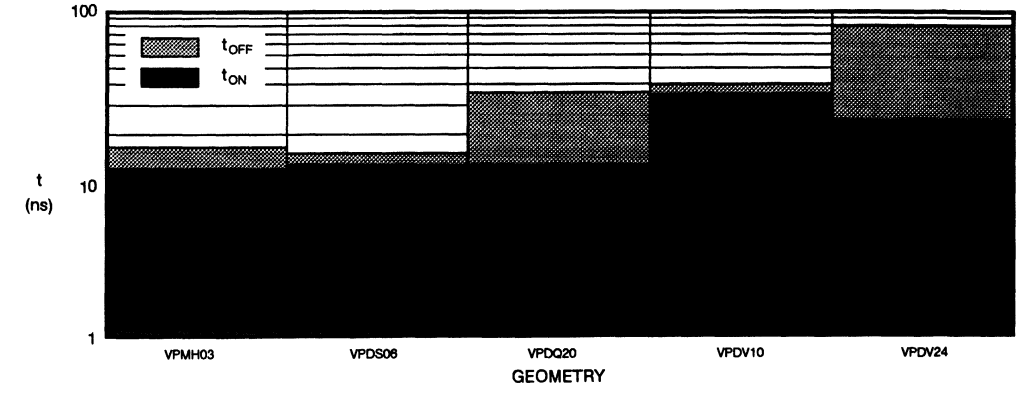


Capacitance vs. Geometry

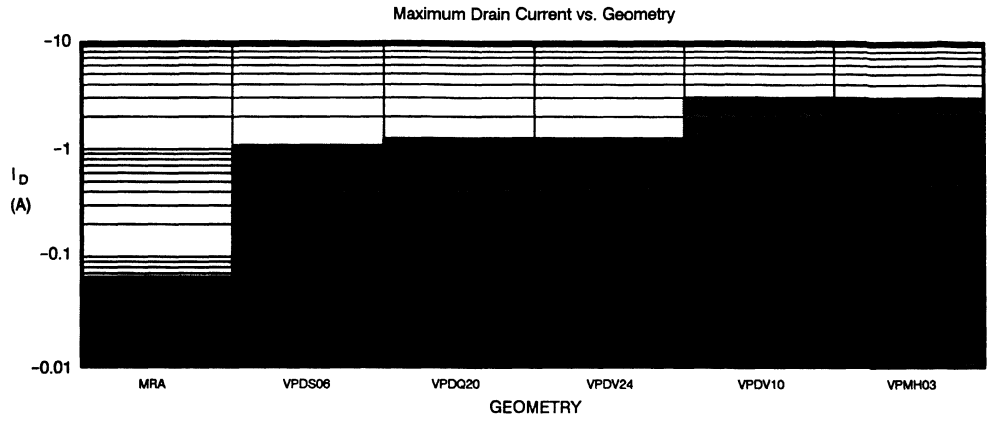


3

Typical Switching Time vs. Geometry



P-CHANNEL GEOMETRY TYPICALS



General Information
Cross Reference
Selector Guide
JFETs 4
DMOS
Low Power MOS
Package Outlines
Applications
Publications Index
Worldwide Sales Offices and Distributors

JFETS

INTRODUCTION

Siliconix has been the market and technology leader in junction field-effect transistors (JFETs) since it was founded in 1962. JFETs have maintained their popularity over the years because they offer exceptional features – low noise, low leakage, high gain, and fast switching – features that even today cannot be matched by integrated circuits or bipolar transistors.

Unlike the bipolar transistor, which requires a base-drive current, a field-effect transistor is operated by the application of a gate voltage. Thus, while the bipolar transistor exhibits low input impedance, the JFET offers just the opposite – a very high-impedance gate.

The high-impedance nature of a JFET offers superb low-leakage qualities – often specified in the low picoamp range. When this is coupled with good frequency response, JFETs ensure minimal circuit loading for such sensitive applications as sample-and-hold circuits and input devices for operational amplifiers.

An additional and fundamental advantage of the JFET is its extraordinary low noise at 1/f frequencies – so low that in comparative studies with bipolar transistors, the JFET is considered noiseless! This advantage is most obvious in applications involving high source impedances, such as those needed for low-noise electet and capacitor microphone amplifier circuits.

The application section of this book will provide some technical assistance. "An Introduction to FETs" (LPD-1) is especially useful reading for the first-time JFET designers.

Siliconix incorporated

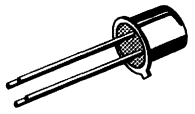
2N4117A SERIES
N-Channel JFETs

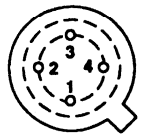
The 2N4117A Series are n-channel JFETs designed to provide ultra-high input impedance. The 2N4117A Series is specified with a 1 pA limit and typically operates at 0.2 pA. These devices, therefore, make perfect choices for use as sensitive front-end amplifiers in applications such as microphones, smoke detectors, and precision test equipment. Additionally, its hermetically sealed TO-72 package allows full military processing per MIL-S-19500. (See Section 1.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (μS)	I_{DSS} MAX (mA)
2N4117A	-1.8	-40	70	0.09
2N4118A	-3	-40	80	0.24
2N4119A	-6	-40	100	0.60

For additional design information please consult performance curves NT.

TO-72 (TO-206AF) BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 CASE

SIMILAR PRODUCTS

- TO-92, See PN4117A Series
- Duals, See U421 Series
- Chips, See NT Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	300	mW
Power Derating		2	mW/°C
Operating Junction Temperature Range	T_J	-55 to 175	°C
Storage Temperature Range	T_{stg}	-65 to 175	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	255	

4

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS							
				2N4117A		2N4118A		2N4119A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	-70	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-0.6	-1.8	-1	-3	-2	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		0.015	0.09	0.08	0.24	0.2	0.6	mA
Drain Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.2		-1		-1		-1	pA
		T_A = 150°C	-0.4		-2.5		-2.5		-2.5	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 30 µA	-0.2							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	0.2							
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz		70	210	80	250	100	330	µS
Common-Source Output Conductance	g_{os}				3		5		10	
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz	1.2		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.3		1.5		1.5		1.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	15							$nV/\sqrt{Hz}$

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.

Siliconix incorporated

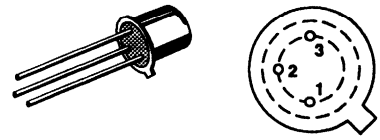
2N4338 SERIES
N-Channel JFETs

The 2N4338 Series of n-channel JFETs is designed for sensitive amplifier stages at low to mid frequencies. It features low cut-off voltages to accommodate low-level power supplies and low leakage for improved system accuracy. The 2N4338 and 2N4339 are ideal for low current, low battery operation. With their 1 dB max. noise figure at 1 kHz, system sensitivity will be excellent. Finally, the 2N4338 Series' TO-18 package is hermetically sealed and suitable for military processing. (See Section 1.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N4338	-1	-50	0.6	0.6
2N4339	-1.8	-50	0.8	1.5
2N4340	-3	-50	1.3	3.6
2N4341	-6	-50	2	9

For additional design information please consult performance curves NPA.

TO-18 BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE & CASE

SIMILAR PRODUCTS

- TO-92, See J201 Series
- SOT-23, See SST201 Series
- Chips, See NPA Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-50	V
Gate-Source Voltage	V_{GS}	-50	
Gate Current	I_G	50	mA
Power Dissipation	P_D	300	mW
Power Derating		2	mW/°C
Operating Junction Temperature Range	T_J	-55 to 175	°C
Storage Temperature Range	T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				2N4338		2N4339		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA		-0.3	-1	-0.6	-1.8	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		0.2	0.6	0.5	1.5	mA
Drain Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 150°C	-4		-100		-100	nA
Gate Operating Current[d]	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -5 V	2		50		50	
Gate-Source Forward Voltage[d]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz		0.6	1.8	0.8	2.4	mS
Common-Source Output Conductance	g_{os}				5		15	µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{DS} = 0 V, V_{GS} = 0 V f = 1 kHz			2500		1700	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	5		7		7	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	6					$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz, R_G = 1 MΩ			1		1	dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

SPECIFICATIONS[a]			LIMITS					
				2N4340		2N4341		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA		-1	-3	-2	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		1.2	3.6	3	9	mA
Drain Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 150°C	-4		-100		-100	nA
Gate Operating Current[d]	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -5 V	2		50			pA
		V_{GS} = -10 V	3				70	
Gate-Source Forward Voltage[d]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz		1.3	3	2	4	mS
Common-Source Output Conductance	g_{os}				30		60	µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 kHz			1500		800	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	5		7		7	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6					$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz, R_G = 1 MΩ			1		1	dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

4

2N4391 SERIES
N-Channel JFETs

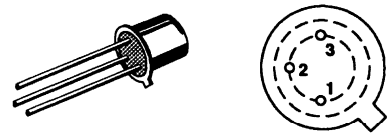
Siliconix incorporated

The 2N4391 Series features many of the superior characteristics of JFETs. Its low on-resistance and fast switching make it a good choice for demanding analog switching applications, while its high-gain, low-noise, and impressive frequency response make it the choice for specialized amplifier circuits. This series also features a hermetically sealed TO-18 can which can be processed per MIL-S-19500. (See Section 1).

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N4391	-10	30	100	20
2N4392	-5	60	100	20
2N4393	-3	100	100	20

For additional design information please consult the typical performance curves NCB.

TO-18 **BOTTOM VIEW**



1 SOURCE
2 DRAIN
3 GATE & CASE

SIMILAR PRODUCTS

- TO-92, See PN4391 Series
- SOT-23, See SST4391 Series
- Duals, See 2N5564 Series
- Chips, See NCB Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation (Case 25°C)	P_D	1800	mW
Power Derating		10	mW/°C
Operating Junction Temperature Range	T_J	-55 to 200	°C
Storage Temperature Range	T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS							
				2N4391		2N4392		2N4393		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA		-4	-10	-2	-5	-0.5	-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		50	150	25	75	5	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-5		-100		-100		-100	pA
		T_A = 150°C	-13		-200		-200		-200	nA
Gate Operating Current[d]	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 20 V, V_{GS} = -5 V	5						100	pA
		V_{DS} = 20 V, V_{GS} = -7 V	5				100			
		V_{DS} = 20 V, V_{GS} = -12 V	5		100					
		V_{DS} = 20 V, T_A = 150°C, V_{GS} = -5 V	13						200	nA
		V_{DS} = 20 V, T_A = 150°C, V_{GS} = -7 V	13				200			
		V_{DS} = 20 V, T_A = 150°C, V_{GS} = -12 V	13		200					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 3 mA	0.25						0.4	V
		V_{GS} = 0 V, I_D = 6 mA	0.3				0.4			
		V_{GS} = 0 V, I_D = 12 mA	0.35		0.4					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			30		60		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7		1		1		1	V
DYNAMIC										
Common-Source Forward Transconductance[d]	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance[d]	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			30		60		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	12		14		14		14	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz, V_{GS} = -5V	3.3						3.5	
		V_{DS} = 0 V, f = 1 MHz, V_{GS} = -7 V	3.2				3.5			
		V_{DS} = 0 V, f = 1 MHz, V_{GS} = -12 V	2.8		3.5					
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3.0							nV/√Hz
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2		15		15		15	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2		5		5		5	
Turn-Off Time	$t_{d(OFF)}$	2N4391 12mA -12V 800Ω 2N4392 6mA -7V 1600Ω 2N4393 3mA -5V 3000Ω	6		20		35		50	
	t_f		13		15		20		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

4

2N4416 SERIES
N-Channel JFETs

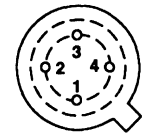
Siliconix incorporated

The 2N4416 and 2N4416A are n-channel JFETs designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise figure (4 dB max @ 400 MHz), high gain (10 dB min @ 400 MHz) and provide wide bandwidth. Its TO-72 hermetically sealed package is available with full military processing. (See Section 1.)

For additional design information please see performance curves NH.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N4416	-6	-30	4.5	15
2N4416A	-6	-35	4.5	15

TO-72 (TO-206AF) **BOTTOM VIEW**



1 SOURCE
2 DRAIN
3 GATE
4 CASE

SIMILAR PRODUCTS

- TO-92, See J304 Series
- SOT-23, See SST4416
- Chips, See NH Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		2N4416	2N4416A	
Gate-Drain Voltage	V_{GD}	-30	-35	V
Gate-Source Voltage	V_{GS}	-30	-35	
Gate Current	I_G	10		mA
Power Dissipation	P_D	300		mW
Power Derating		1.7		mW/°C
Operating Junction Temperature Range	T_J	-55 to 150		°C
Storage Temperature Range	T_{stg}	-65 to 200		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300		

SPECIFICATIONS[a]			LIMITS					
				2N4416		2N4416A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-36	-30		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-3		-6	-2.5	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	10	5	15	5	15	mA
Drain Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 150°C	-4		-100		-100	nA
Gate Operating Current[d]	I_G	V_{DG} = 10 V, I_D = 1 mA	-20					pA
Drain Cutoff Current[d]	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -6 V	2					
Drain-Source On-Resistance[d]	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	150					Ω
Gate-Source Forward Voltage[d]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance[c]	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz	6	4.5	7.5	4.5	7.5	mS
Common-Source Output Conductance[c]	g_{os}		15		50		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	2.2		4		4	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		0.8		0.8	
Common-Source Output Capacitance	C_{oss}		1		2		2	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	6					$nV/\sqrt{Hz}$
HIGH-FREQUENCY								
				100 MHZ		400 MHZ		
Common-Source Input Conductance	g_{iss}	V_{DS} = 15 V, V_{GS} = 0 V			100		1000	µS
Common-Source Input Susceptance	b_{iss}				2500		10,000	
Common-Source Output Capacitance	g_{oss}				75		100	
Common-Source Output Susceptance	b_{oss}				1000		4000	
Common-Source Forward Transconductance	g_{fs}					4000		
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_D = 5 mA		18		10		dB
Noise Figure	NF	R_G = 1 kΩ			2		4	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

2N5114 SERIES
P-Channel JFETs

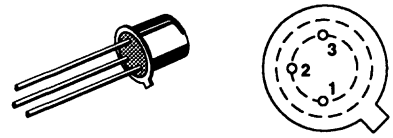
Siliconix incorporated

The 2N5114 Series are p-channel JFET analog switches designed to complement our n-channel 2N4091 Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. They are housed in TO-18 hermetic packages and available with JAN, JANTX, or JANTXV level processing. (See 2N5114 JANTX data sheet.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N5114	10	75	-500	16
2N5115	6	100	-500	30
2N5116	4	150	-500	60

For additional design information please see performance curves PSCIA.

TO-18 BOTTOM VIEW



1 SOURCE
2 GATE & CASE
3 DRAIN

SIMILAR PRODUCTS

- TO-92, See J174 Series
- SOT-23, See SST174 Series
- Chips, See PSCIA Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	-50	mA
Power Dissipation	P_D	500	mW
Power Derating		3	mW/°C
Operating Junction Temperature Range	T_J	-55 to 200	°C
Storage Temperature Range	T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]				LIMITS							
					2N5114		2N5115		2N5116		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V		45	30		30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −1 nA			5	10	3	6	1	4	
Saturation Drain Current[c]	I_{DSS}	V_{GS} = 0 V	V_{DS} = −18 V		−30	−90					mA
			V_{DS} = −15 V				−15	−60	−5	−25	
Gate Reverse Current	I_{GSS}	V_{GS} = −20 V, V_{DS} = 0 V		5		500		500		500	pA
			T_A = 150°C	0.01		1		1		1	µA
Gate Operating Current[d]	I_G	V_{DG} = −15 V, I_D = −1 mA		−5							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V	V_{GS} = 12 V	−10		−500					pA
			V_{GS} = 7 V	−10				−500			
			V_{GS} = 5 V	−10						−500	
		V_{DS} = −15 V, T_A = 150°C	V_{GS} = 12 V	−0.02		−1					µA
			V_{GS} = 7 V	−0.02				−1			
			V_{GS} = 5 V	−0.02						−1	
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = −15 mA	−1.0		−1.3					V
			I_D = −7 mA	−0.7				−0.8			
			I_D = −3 mA	−0.5						−0.6	
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = −1 mA				75		100		150	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V		−0.7		−1		−1		−1	V
DYNAMIC											
Common-Source Forward Transconductance[d]	g_{fs}	V_{DG} = −15 V, I_D = −1 mA, f = 1 kHz		4.5							mS
Common-Source Output Conductance[d]	g_{os}			20							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz				75		100		150	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz		20		25		25		25	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = 12 V	5		7					
			V_{GS} = 7 V	6				7			
			V_{GS} = 5 V	6						7	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DG} = −10 V, I_D = −1 mA, f = 1 kHz		20							$nV/\sqrt{Hz}$
SWITCHING											
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V				6		10		25	ns
	t_r	P/N V_{DD} $I_{D(ON)}$ $V_{GS(OFF)}$ R_L				10		20		35	
Turn-Off Time	$t_{d(OFF)}$	2N5114 −10V −15mA 20V 130Ω 2N5115 −6V −7mA 12V 900Ω 2N5116 −6V −3mA 8V 2000Ω				6		8		20	
	t_f					15		30		60	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 2%.
d. This parameter not registered with JEDEC.

2N5114 SERIES – JANTX, JANTXV P-Channel JFETs

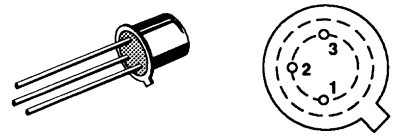
Siliconix incorporated

The 2N5114 Series are p-channel JFET analog switches designed to complement our n-channel 2N4856 Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. They are housed in TO-18 hermetic packages and available with JAN, JANTX, or JANTXV level processing.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N5114	10	75	-500	16
2N5115	6	100	-500	30
2N5116	4	150	-500	42

For additional design information please see performance curves PSCIA.

TO-18 **BOTTOM VIEW**



1 SOURCE
2 GATE & CASE
3 DRAIN

SIMILAR PRODUCTS

- TO-92, See J174 Series
- SOT-23, See SST174 Series
- Chips, See PSCIA Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	-50	mA
Power Dissipation	P_D	500	mW
Power Derating		3	mW/°C
Operating Junction Temperature Range	T_J	-55 to 200	°C
Storage Temperature Range	T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

2N5114 SERIES – JANTX, JANTXV

SPECIFICATIONS[a]				LIMITS							
					2N5114		2N5115		2N5116		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V		45	30		30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −1 nA			5	10	3	6	1	4	
Saturation Drain Current[c]	I_{DSS}	V_{GS} = 0 V	V_{DS} = −18 V		−30	−90					mA
			V_{DS} = −15 V				−15	−60	−5	−25	
Gate Reverse Current	I_{GSS}	V_{GS} = −20 V, V_{DS} = 0 V		5		500		500		500	pA
			T_A = 150°C	0.01		1		1		1	µA
Gate Operating Current[d]	I_G	V_{DG} = −15 V, I_D = −1 mA		5							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V	V_{GS} = 12 V	−10		−500					pA
			V_{GS} = 7 V	−10				−500			
			V_{GS} = 5 V	−10						−500	
		V_{DS} = −15 V, T_A = 150°C	V_{GS} = 12 V	−0.02		−1					µA
			V_{GS} = 7 V	−0.02				−1			
			V_{GS} = 5 V	−0.02						−1	
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = −15 mA	−1.0		−1.3					V
			I_D = −7 mA	−0.7				−0.8			
			I_D = −3 mA	−0.5						−0.6	
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = −1 mA				75		100		150	Ω
Gate-Source Forward Voltage[d]	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V		−0.7							V
DYNAMIC											
Common-Source Forward Transconductance[d]	g_{fs}	V_{DG} = −15 V, I_D = −1 mA, f = 1 kHz		4.5							mS
Common-Source Output Conductance[d]	g_{os}			20							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz				75		100		175	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz		20		25		25		27	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = 12 V	5		7					
			V_{GS} = 7 V	6				7			
			V_{GS} = 5 V	6						7	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DG} = −10 V, I_D = −1 mA, f = 1 kHz		20							$nV/\sqrt{Hz}$
SWITCHING											
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V				6		10		12	ns
	t_r	P/N V_{DD} $I_{D(ON)}$ $V_{GS(OFF)}$ R_L R_G				10		20		30	
Turn-Off Time	$t_{d(OFF)}$	2N5114 −10V −15mA 20V 630Ω 100Ω 2N5115 −6V −7mA 12V 900Ω 220Ω 2N5116 −6V −3mA 8V 2000Ω 390Ω				6		8		10	
	t_f					15		30		50	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 2%.
d. Not JEDEC registered.

4

2N5196 SERIES
N-Channel JFET Pairs

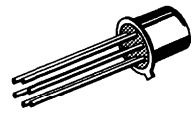
Siliconix incorporated

The 2N5196 Series of monolithic JFET pairs is designed for high-performance differential amplification for a wide range of precision test instrumentation applications. This series features tight matching specs, low gate leakage for accuracy, and wide dynamic range as I_G is guaranteed at V_{DG} = 20 V. Its TO-71 package is hermetically sealed and is available with full military processing. (See Section 1.)

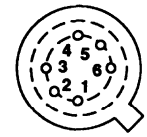
PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS1}-V_{GS2}\rvert$ MAX (mV)
2N5196	-50	1	-15	5
2N5197	-50	1	-15	5
2N5198	-50	1	-15	10
2N5199	-50	1	-15	15

For additional design information please see performance curves NQP.

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- High Gain, See 2N5911 Series
- Chips, See NQP Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Drain Voltage		V_{GD}	-50	V
Gate-Source Voltage		V_{GS}	-50	
Forward Gate Current		I_G	50	mA
Power Dissipation (T_A = 85°C)	Per Side	P_D	250	mW
	Total		500	
Power Derating (T_A = 85°C)	Per Side		2.56	mW/°C
	Total		4.3	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

SPECIFICATIONS[a]			LIMITS					
				2N5196		2N5197		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA	-2	-0.7	-4	-0.7	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	3	0.7	7	0.7	7	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-10		-25		-25	pA
		T_A = 150°C	-20		-50		-50	nA
Gate Operating Current	I_G	V_{DG} = 20 V, I_D = 200 µA	-5		-15		-15	pA
		T_A = 125°C	-0.8		-15		-15	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 20 V, I_D = 200 µA	-1.5	-0.2	-3.8	-0.2	-3.8	V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	2.5	1	4	1	4	mS
Common-Source Output Conductance	g_{os}		2		50		50	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 200 µA, f = 1 kHz	0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g_{os}		1		4		4	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	3		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		2		2	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	9		20		20	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 20 V, V_{GS} = 0 V, f = 100 Hz, R_G = 10 MΩ			0.5		0.5	dB
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 200 µA, V_{DG} = 20 V	3		5		5	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 200 µA, V_{DG} = 20 V; T = -55 to 25°C	3		5		10	µV/°C
		T = 25 to 125°C	3		5		10	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 20 V, V_{GS} = 0 V	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 20 V, I_D = 200 µA, f = 1 kHz	0.99	0.97	1	0.97	1	
Differential Output Capacitance	$\lvert g_{os1} - g_{os2} \rvert$		0.1		1		1	µS
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$	V_{DG} = 20 V, I_D = 200 µA, T_A = 125°C	0.1		5		5	nA
Common Mode Rejection Ratio[d]	CMRR	V_{DD} = 10 to 20 V, I_D = 200 µA	100					dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

4

SPECIFICATIONS[a]			LIMITS					
				2N5198		2N5199		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA	-2	-0.7	-4	-0.7	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	3	0.7	7	0.7	7	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-10		-25		-25	pA
		T_A = 150°C	-20		-50		-50	nA
Gate Operating Current	I_G	V_{DG} = 20 V, I_D = 200 µA	-5		-15		-15	pA
		T_A = 125°C	-0.8		-15		-15	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 20 V, I_D = 200 µA	-1.5	-0.2	-3.8	-0.2	-3.8	V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	2.5	1	4	1	4	mS
Common-Source Output Conductance	g_{os}		2		50		50	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 200 µA, f = 1 kHz	0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g_{os}		1		4		4	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	3		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		2		2	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	9		20		20	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 20 V, V_{GS} = 0 V, f = 100 Hz, R_G = 10 MΩ			0.5		0.5	dB
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 200 µA , V_{DG} = 20 V	7		10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 200 µA, V_{DG} = 20 V, T = -55 to 25°C	10		20		40	µV/°C
		T = 25 to 125°C	10		20		40	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 20 V, V_{GS} = 0 V	0.97	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 20 V, I_D = 200 µA, f = 1 kHz	0.97	0.95	1	0.95	1	
Differential Output Capacitance	$\lvert g_{os1} - g_{os2} \rvert$		0.2		1		1	µS
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$	V_{DG} = 20 V, I_D = 200 µA, T_A = 125°C	0.1		5		5	nA
Common Mode Rejection Ratio[d]	CMRR	V_{DD} = 10 to 20 V, I_D = 200 µA	97					dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

Siliconix incorporated

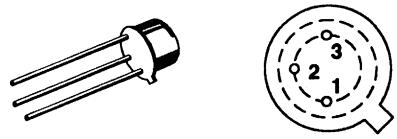
2N5432 SERIES
N-Channel JFETs

The 2N5432 Series offers the designer an alternative for true high performance analog switching applications. Good breakdown voltage characteristics coupled with low on-resistance and very fast switching make these devices suitable for a wide range of applications. For military designs, the TO-52 package is hermetically sealed and suitable for processing per MIL-S-19500. (See Section 1.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N5432	-10	5	200	5
2N5433	-9	7	200	5
2N5434	-4	10	200	5

For further design information please consult the typical performance curves NIP.

TO-52 (TO-206AC) **BOTTOM VIEW**



1 SOURCE
2 DRAIN
3 GATE & CASE

SIMILAR PRODUCTS

- SOT-23, See SST108 Series
- TO-92, See J108 Series
- Chips, See NIP Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	100	mA
Power Dissipation	P_D	300	mW
Power Derating		2.4	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-65 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS							
				2N5432		2N5433		2N5434		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-32	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 3 nA		-4	-10	-3	-9	-1	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		150		100		30		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5		-200		-200		-200	pA
		T_A = 150°C	-10		-200		-200		-200	nA
Gate Operating Current[d]	I_G	V_{DG} = 10 V, I_D = 10 mA	-10							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	10		200		200		200	
		T_A = 150°C	20		200		200		200	
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 mA			50		70		100	mV
Drain-Source On-Resistance	$r_{DS(ON)}$			2	5		7		10	Ω
Gate-Source Forward Voltage[d]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance[d]	g_{fs}	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	17							mS
Common-Source Output Conductance[d]	g_{os}		600							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V f = 1 kHz			5		7		10	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	20		30		30		30	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		11		15		15		15	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	3.5							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	2		4		4		4	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	0.5		1		1		1	
Turn-Off Time	$t_{d(OFF)}$	2N5432 10mA -12V 145Ω 2N5433 10mA -12V 143Ω 2N5434 10mA -12V 140Ω	4		6		6		6	
	t_f		18		30		30		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

Siliconix incorporated

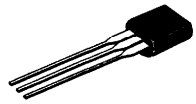
2N5484 SERIES
N-Channel JFETs

The 2N5484 Series of n-channel JFETs is designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise (4 dB max @ 400 MHz), high gain (5.5 mS typical @ 400 MHz) and provide wide bandwidth. Additionally, its low-cost TO-92 package is available with tape and reel to support automated assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N5484	-3	-25	3	5
2N5485	-4	-25	3.5	10
2N5486	-6	-25	4	20

For additional design information please see performance curves NH.

TO-92 (TO-226AA)



BOTTOM VIEW

1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST4416
- Chips, See NH Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Drain Current	I_D	30	
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-65 to 135	°C
Storage Temperature Range	T_{stg}	-65 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]				LIMITS							
					2N5484		2N5485		2N5486		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V		-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 10 nA			-0.3	-3	-0.5	-4	-2	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V			1	5	4	10	8	20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V		-0.002		-1		-1		-1	nA
			T_A = 100°C	-0.2		-200		-200		-200	
Gate Operating Current[d]	I_G	V_{DG} = 10 V, I_D = 1 mA		-20							pA
Gate-Source Forward Voltage[d]	$V_{GS(F)}$	I_G = 10 mA , V_{DS} = 0 V		0.8							V
DYNAMIC											
Common-Source Forward Transconductance[c]	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz			3	6	3.5	7	4	8	mS
Common-Source Output Conductance[c]	g_{os}					50		60		75	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz		2.2		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}			0.7		1		1		1	
Common-Source Output Capacitance	C_{oss}			1		2		2		2	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DS} = 15 V, V_{GS} = 0 V f = 100 Hz		10							$nV/\sqrt{Hz}$
HIGH-FREQUENCY											
Common-Source Transconductance	Y_{fs}	V_{DS} = 15 V, V_{GS} = 0 V	f = 100 MHz	4.5	2.5						mS
			f = 400 MHz	5.5			3		3.5		
Common-Source Output Conductance	Y_{os}		f = 100 MHz	30		75					µS
			f = 400 MHz	50				100		100	
Common-Source Input Conductance	Y_{is}		f = 100 MHz			0.1					mS
			f = 400 MHz					1		1	
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_D = 1 mA f = 100 MHz		20	16	25					dB
		V_{DS} = 15 V, I_D = 4 mA	f = 100 MHz	21			18	30	18	30	
			f = 400 MHz	13			10	20	10	20	
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V R_G = 1 MΩ, f = 1 kHz		0.3		2.5		2.5		2.5	
		V_{DS} = 15 V, I_D = 1 mA R_G = 1 MΩ, f = 100 MHz		2		3					
		V_{DS} = 15 V, I_D = 4 mA	f = 100 MHz	1				2		2	
		R_G = 1 MΩ	f = 400 MHz	2.5				4		4	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

Siliconix incorporated

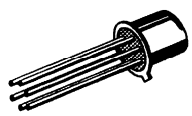
2N5564 SERIES
N-Channel JFET Pairs

The 2N5564 Series are matched pairs of JFETs mounted in a single TO-71 package. This two-chip design reduces parasitic performance at high frequency while ensuring extremely tight matching. The 2N5564 features high breakdown voltage ($V_{(BR)GSS}$ typically > 55 V), high gain (typically > 9 mS), and less than 5 mV offset between the two die. Additionally, its TO-71 package is hermetically sealed and can be processed per MIL-S-19500. (See Section 1.)

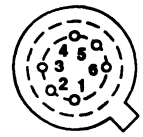
PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS1}-V_{GS2}\rvert$ MAX (mV)
2N5564	-40	7.5	-100	5
2N5565	-40	7.5	-100	10
2N5566	-40	7.5	-100	20

For additional design information please see performance curves NCB.

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, See NCBD1 Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Drain Voltage		V_{GD}	-40	V
Gate-Source Voltage		V_{GS}	-40	
Gate-Gate Voltage		V_{GG}	±80	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	325	mW
	Total		650	
Power Derating	Per Side		2.2	mW/°C
	Total		3.3	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

SPECIFICATIONS[a]			LIMITS							
				2N5564		2N5565		2N5566		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-2	-0.5	-3	-0.5	-3	-0.5	-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	20	5	30	5	30	5	30	mA
Gate Reverse Current[c]	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-5		-100		-100		-100	pA
		T_A = 150°C	-10		-200		-200		-200	nA
Gate Operating Current[d]	I_G	V_{DG} = 15 V, I_D = 2 mA	-3							pA
		T_A = 125°C	-1							nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	50		100		100		100	Ω
Gate-Source Voltage[d]	V_{GS}	V_{DS} = 15 V, I_D = 2 mA	-1.2							V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 2 mA, V_{DS} = 0 V	0.7		1		1		1	
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 2 mA, f = 1 kHz	9	7.5	12.5	7.5	12.5	7.5	12.5	mS
Common-Source Output Conductance	g_{os}		35		45		45		45	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 2 mA, f = 100 MHz	8.5	7		7		7		mS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 2 mA, f = 1 MHz	10		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		2.5		3		3		3	
Equivalent Input Noise Voltage	$\overline{e_n}$	V_{DG} = 15 V, I_D = 2 mA, f = 10 Hz	12		50		50		50	$nV/\sqrt{Hz}$
Noise Figure	NF	R_G = 10 MΩ			1		1		1	dB
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 2 mA, V_{DS} = 15 V			5		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 2 mA, V_{DS} = 15 V, T = -55 to 25°C			10		25		50	µV/°C
		T = 25 to 125°C			10		25		50	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 15 V, V_{GS} = 0 V	0.98	0.95	1	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 15 V, I_D = 2 mA, f = 1 kHz	0.98	0.95	1	0.90	1	0.90	1	
Common Mode Rejection Ratio[d]	CMRR	V_{DD} = 10 to 20 V, I_D = 2 mA	76							dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

Siliconix incorporated

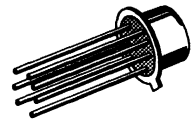
2N5911 SERIES
N-Channel JFET Pairs

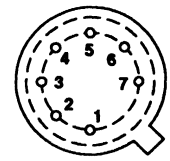
The 2N5911 Series are JFET matched pairs mounted in a single TO-78 package. This two-chip design reduces parasitic performance at high-frequency while ensuring extremely tight matching. The 2N5911 features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its TO-78 hermetically sealed package is available with military screening per MIL-S-19500. (See Section 1.)

For additional design information please see performance curves NZF.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS1}-V_{GS2}\rvert$ MAX (mV)
2N5911	-25	5	-100	10
2N5912	-25	5	-100	15

TO-78 **BOTTOM VIEW**





1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE
5 SOURCE 2
6 DRAIN 2
7 GATE 2

SIMILAR PRODUCTS

- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, See NZF Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Gate-Gate Voltage		V_{GG}	±80	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	367	mW
	Total		500	
Power Derating	Per Side		3	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				2N5911		2N5912		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-5	-1	-5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	7	40	7	40	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-100		-100	pA
		T_A = 150°C	-2		-250		-250	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-100		-100	pA
		T_A = 125°C	-0.3		-100		-100	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 5 mA	-1.5	-0.3	-4	-0.3	-4	V
Gate-Source Forward Voltage[d]	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7					
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA f = 1 kHz	6	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		70		100		100	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA f = 100 MHz	5.8	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		90		150		150	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA f = 1 kHz	3		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		1.2		1.2	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA f = 10 kHz	4		20		20	$nV/\sqrt{Hz}$
Noise Figure	NF	R_G = 100 kΩ	0.1		1		1	dB
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 5 mA , V_{DG} = 10 V	4		10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 5 mA, V_{DG} = 10 V; T= -55 to 25°C	15		20		40	µV/°C
		T= 25 to 125°C	15		20		40	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA f = 1 kHz	0.98	0.95	1	0.95	1	
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA T_A = 125°C	0.005		20		20	nA
Common Mode Rejection Ratio[d]	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	85					dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

Siliconix incorporated

DPAD1 SERIES
Dual Low-Leakage Pico-Amp Diodes

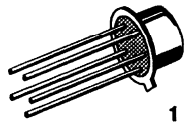
The DPAD1 Series of extremely low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. These devices feature leakage currents ranging from -1 pA (DPAD1) to -50 pA (DPAD50) to support a wide range of applications. With two diodes per package, the DPAD1 Series is well suited for use in applications such as input protection for operational amplifiers. Its hermetically sealed metal can is available with full military processing per MIL-S-19500. (See Section 1.)

PART NUMBER	I_R (pA)
DPAD1	-1
DPAD5	-5
DPAD50	-50

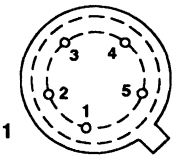
SIMILAR PRODUCTS

- TO-92, See JPAD5 Series
- SOT-23, See SSTPAD5 Series
- TO-18, See PAD1 Series

TO-78 (MODIFIED)



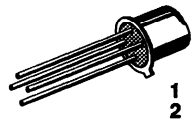
BOTTOM VIEW



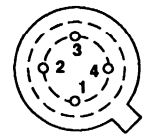
1 CATHODE 1
2 ANODE 1
***3 CASE**
4 CATHODE 2
5 ANODE 2

(DPAD1)

TO-71 (MODIFIED)



BOTTOM VIEW



1 CATHODE 1
2 ANODE 1
3 CATHODE 2
4 ANODE 2

(DPAD5, 50)

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Forward Current	I_F	50	mA
Total Device Dissipation	P_D	400	mW
Storage Temperature	T_{stg}	-65 to 135	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

*Case must be floating

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	DPAD1	-0.2		-1	pA
			DPAD5	-2		-5	
			DPAD50	-10		-50	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA	DPAD1, 5	-60	-45	-120	V
			DPAD50	-55	-35		
Forward Voltage Drop	V_F	I_F = 1 mA		0.7		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V, f = 1 MHz	DPAD1, 5	0.6		0.8	pF
			DPAD50	1		2	
Differential Capacitance	$\lvert C_{R1} - C_{R2} \rvert$	$V_{R1} = V_{R2}$ = -5 V, f = 1 MHz		0.07		0.2	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.

Siliconix incorporated

J105 SERIES
N-Channel JFETs

The J105 Series are high-performance JFET analog switches designed to offer low on-resistance and fast switching. $r_{DS(ON)}$ <3 Ω is guaranteed with the J105 which makes this device the lowest of any commercially available JFET. The J105 Series devices are housed in a low-cost TO-92 package and offer a wide range of tape and reel options. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
J105	-10	3	10	14
J106	-6	6	10	14
J107	-4.5	8	10	14

For further design information please consult the typical performance curves NVA.

TO-92 (TO-226AA) **BOTTOM VIEW**

1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-52, See U290 Series
- Chips, See NVA Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	50	mA
Power Dissipation (Case 25°C)	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]			LIMITS							
				J105		J106		J107		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-4.5	-10	-2	-6	-0.5	-4.5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		500		200		100		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.02		-3		-3		-3	nA
		T_A = 125°C	-10							
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 25 mA	-0.01							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.01		3		3		3	
		T_A = 125°C	5							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			3		6		8	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 25 mA f = 1 kHz	55							mS
Common-Source Output Conductance	g_{os}		5							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA f = 1 kHz			3		6		8	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V f = 1 MHz	120		160		160		160	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	20		35		35		35	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 25 mA f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	6							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	8							
Turn-Off Time	$t_{d(OFF)}$	J105 28mA -12V 50Ω J106 27mA -7V 50Ω J107 26mA -5V 50Ω	5							
	t_r		9							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

J108 SERIES
N-Channel JFETs

The J108 Series is designed with high-performance analog switching applications in mind. It features low on-resistance, good off-isolation, and fast switching. The TO-92 package affords low-cost and a wide range of tape and reel options. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
J108	-10	8	20	4
J109	-6	12	20	4
J110	-4	18	20	4

For further design information please consult the typical performance curves NIP.

SIMILAR PRODUCTS

- SOT-23, See SST108 Series
- TO-52, See 2N5432 Series
- Chips, See NIP Series Die

TO-92 (TO-226AA) BOTTOM VIEW

1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

J108 SERIES

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS							
				J108		J109		J110		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-32	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-3	-10	-2	-6	-0.5	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		80		40		10		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.01		-3		-3		-3	nA
		T_A = 125°C	-5							
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 10 mA	-0.01							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.02		3		3		3	
		T_A = 125°C	10							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, $V_{DS} \leq$ 0.1 V			8		12		18	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	17							mS
Common-Source Output Conductance	g_{os}		600							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V f = 1 kHz			8		12		18	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V f = 1 MHz	60		85		85		85	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	11		15		15		15	
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	3.5							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	3							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	1							
Turn-Off Time	$t_{d(OFF)}$	J108 10mA -12V 150Ω J109 10mA -7V 150Ω J110 10mA -5V 150Ω	4							
	t_r		18							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.

Siliconix incorporated

J111 SERIES
N-Channel JFETs

The J111 Series are low-cost, all-purpose analog switches designed to support a wide range of applications. They features low on-resistance, capacitance and good off-isolation. Additionally, our TO-92 package allows a variety of tape and reel combinations. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
J111	-10	30	5	4
J112	-5	50	5	4
J113	-3	100	5	4

For further design information please consult the typical performance curves NCB.

TO-92 (TO-226AA) **BOTTOM VIEW**

1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST111 Series
- TO-18, See 2N4391 Series
- Duals, See 2N5564 Series
- Chips See NCB Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-35	V
Gate-Source Voltage	V_{GS}	-35	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

J111 SERIES

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS							
				J111		J112		J113		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-3	-10	-1	-5		-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		20		5		2		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		T_A = 125°C	-3							
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.005		1		1		1	nA
		T_A = 125°C	3							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = 0.1 V			30		50		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V f = 1 kHz			30		50		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	7		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		5		5		5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 1 mA f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							
Turn-Off Time	$t_{d(OFF)}$	J111 12mA -12V 800Ω J112 6mA -7V 1600Ω J113 3mA -5V 3200Ω	6							
	t_f		15							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

J174 SERIES
P-Channel JFETs

The J174 Series are low-cost p-channel analog switches designed to provide low on-resistance and fast switching. They also work well in conjunction with Siliconix' J111 Series for complimentary switching applications. The J174 Series devices are housed in TO-92 packages and are available with various tape and reel options. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (nA)	t_{ON} TYP (ns)
J174	10	85	-1	25
J175	6	125	-1	25
J176	4	250	-1	25
J177	2.25	300	-1	25

For further design information please consult the typical performance curves PSCIA.

SIMILAR PRODUCTS

- TO-18, See 2N5114 Series
- SOT-23, See SST174 Series
- Chips, See PSCIA Series Die

TO-92 (TO-226AA) BOTTOM VIEW

1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	-50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]			LIMITS					
				J174		J175		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −10 nA		5	10	3	6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−20	−135	−7	−70	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	0.01					
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−0.01		−1		−1	
		T_A = 125°C	−5					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = −0.1 V			85		125	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = −15 V, I_D = −1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			85		125	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = −10 V, I_D = −1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r	P/N V_{DD} $V_{GS(OFF)}$ R_L	15					
Turn-Off Time	$t_{d(OFF)}$	J174 −10 V 12 V 560Ω J175 −6 V 8 V 1200Ω	10					
	t_f		20					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

SPECIFICATIONS[a]			LIMITS					
				J176		J177		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -15 V, I_D = -10 nA		1	4	0.8	2.25	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = -15 V, V_{GS} = 0 V		-2	-35	-1.5	-20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = -15 V, I_D = -1 mA	0.01					
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = -15 V, V_{GS} = 10 V	-0.01		-1		-1	
		T_A = 125°C	-5					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = -0.1 V			250		300	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V	-0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = -15 V, I_D = -1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			250		300	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = -10 V, I_D = -1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r	P/N V_{DD} $V_{GS(OFF)}$ R_L	15					
Turn-Off Time	$t_{d(OFF)}$	J176 -6 V 6 V 5600Ω J177 -6 V 3 V 10000Ω	10					
	t_f		20					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

J201 SERIES
N-Channel JFETs

Siliconix incorporated

The J201 Series of popular, low-cost JFETs offers high performance in a wide range of applications. With features such as 100 pA gate leakage, -40 V breakdown voltage, and 5 nV/√Hz noise, these devices are especially characterized for sensitive amplifier stages. The J201 has a low cut-off voltages, and is ideal for battery operated equipment and low current amplifiers. The J201 Series in the TO-92 package offers both value and compatibility with automated assembly.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J201	-1.5	-40	0.5	1
J202	-4	-40	1	4.5

For further design information please consult the typical performance curves NPA.

TO-92 (TO-226AA) BOTTOM VIEW

1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST201 Series
- TO-18, See 2N4338 Series
- Chips, See NPA Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS					
				J201		J202		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA		-0.3	-1.5	-0.8	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.2	1	0.9	4.5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 125°C	-1					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	2					
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, V_{GS} = 0 V f = 1 kHz		0.5		1		mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V f = 1 MHz	4.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	6					$nV/\sqrt{Hz}$

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.

4

J210 SERIES
N-Channel JFETs

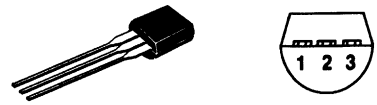
Siliconix incorporated

The J210 Series of n-channel JFETs provides good general purpose amplifiers for a wide range of test and instrumentation applications. This series features low-leakage (I_{GSS} < 100 pA), high gain (g_{fs} > 7 mS for J212), and low noise. Additionally, its low cost TO-92 package ensures value as well as compatibility with automated assembly techniques. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J210	-3	-25	4	15
J211	-4.5	-25	6	20
J212	-6	-25	7	40

For additional design information please see performance curves NZF.

TO-92 (TO-226AA) **BOTTOM VIEW**



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- Duals, See 2N5911 Series
- Chips, See NZF Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS							
				J210		J211		J212		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA		-1	-3	-2.5	-4.5	-4	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		2	15	7	20	15	40	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-100		-100		-100	pA
		T_A = 125°C	-0.5							nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-1							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	1							
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz		4	12	6	12	7	12	mS
Common-Source Output Conductance	g_{os}				150		200		200	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	4							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz	5							$nV/\sqrt{Hz}$

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.

4

J304 SERIES
N-Channel JFETs

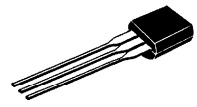
Siliconix incorporated

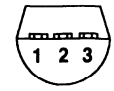
The J304 Series of n-channel JFETs is designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise, high gain and provide wide bandwidth.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J304	-6	-30	4.5	15
J305	-3	-30	3	8

For additional design information please see performance curves NH.

TO-92 (TO-226AA) **BOTTOM VIEW**





1 SOURCE
2 DRAIN
3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST5484 Series
- TO-72, See 2N4416 Series
- Chips, See NH Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS					
				J304		J305		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA		-2	-6	-0.5	-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		5	15	1	8	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 100°C	-0.2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-20					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -6 V	2					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 1 V, I_D = 1 mA	200					Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, V_{GS} = 0 V f = 1 kHz		4.5	7.5	3		mS
Common-Source Output Conductance	g_{os}				50		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	2.2					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7					
Common-Source Output Capacitance	C_{oss}		1					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 100 Hz	10					$nV/\sqrt{Hz}$

SPECIFICATIONS[a]			LIMITS (Typical)				
			J304		J305		
PARAMETER	SYMBOL	TEST CONDITIONS	100 MHz	400 MHz	100 MHz	400 MHz	UNIT
HIGH-FREQUENCY							
Common-Source Input Conductance	g_{iss}	V_{DS} = 15 V, V_{GS} = 0 V	80	800	80		µS
Common-Source Input Susceptance	b_{iss}		2	7.5	2		mS
Common-Source Output Conductance	g_{oss}		60	80	60		µS
Common-Source Output Susceptance	b_{oss}		0.8	3.6	0.8		mS
Common-Source Forward Transconductance	g_{fs}			4.2	3		
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_G = 5 mA	20	11			dB
Noise Figure	NF	R_G = 1 kΩ	1.7	3.8			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 2%.

J308 SERIES
N-Channel JFETs

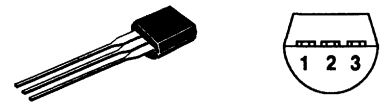
Siliconix incorporated

The J308 Series is a popular, low-cost device which offers superb amplification characteristics. It features high-gain, low noise (typically < 6 $nV\sqrt{Hz}$) and low gate leakage (typically < 2 pA). Of special interest, however, is performance at high frequency. Even at 450 MHz the J308 Series offers high power gain and low noise. Like all TO-92 packages offered by Siliconix, tape and reel options are available to support automated assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J308	-6.5	-25	8	60
J309	-4.0	-25	8	30
J310	-6.5	-25	8	60

For additional design information and a closer look at high-frequency characteristics, please consult performance curves NZB.

TO-92 (TO-226AA) BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-52, See U309 Series
- SOT-23, See SST308 Series
- Dual, See U430 Series
- Chips, See NZB Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]				LIMITS							
					J308		J309		J310		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V		-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA			-1	-6.5	-1	-4	-2	-6.5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V			12	60	12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V		-0.002		-1		-1		-1	nA
			T_A = 125°C	-0.008		-1		-1		-1	µA
Gate Operating Current	I_G	V_{DG} = 9 V, I_D = 10 mA		-15							pA
Drain Cutoff Current	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA		35							Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V		0.7		1		1		1	V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA f = 1 kHz		14	8		10		8		mS
Common-Source Output Conductance	g_{os}			110		250		250		250	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = -10 V f = 1 MHz		4		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}			1.9		2.5		2.5		2.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA f = 100 Hz		6							$nV/\sqrt{Hz}$
HIGH FREQUENCY											
Common-Gate Forward Transconductance	g_{fg}	V_{DS} = 10 V I_D = 10 mA	f = 105 MHz	15							mS
			f = 450 MHz	13							
Common-Gate Output Conductance	g_{og}		f = 105 MHz	0.16							
			f = 450 MHz	0.55							
Common-Gate Power Gain[d]	G_{pg}		f = 105 MHz	16							dB
			f = 450 MHz	11.5							
Noise Figure	NF		f = 105 MHz	1.5							
			f = 450 MHz	2.7							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. Gain (G_{pg}) measured at optimum input noise match.

4

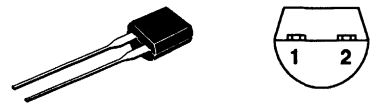
JPAD5 SERIES
Low-Leakage Pico-Amp Diodes

Siliconix incorporated

The JPAD5 Series of low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. Its TO-92 package allows designers to maximize circuit performance while maintaining the objectives of low cost and compact packaging. Tape and reel is available for use with automated assembly techniques. (See Section 7.)

PART NUMBER	I_R (pA)
JPAD5	-5
JPAD50	-50

TO-92 (Modified) **BOTTOM VIEW**



1 CATHODE
2 ANODE

SIMILAR PRODUCTS

- SOT-23, See SSTPAD5 Series
- TO-18, See PAD1 Series
- Duals, See DPAD1 Series

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Forward Current	I_F	10	mA
Total Device Dissipation	P_D	360	mW
Storage Temperature	T_{stg}	-55 to 135	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	JPAD5	-1		-5	pA
			JPAD50	-5		-50	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA		-60	-35		V
Forward Voltage Drop	V_F	I_F = 5 mA		0.8		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V, f = 1 MHz		1.5		2	pF

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.

Rev. A (02/11/91)

Siliconix incorporated

PAD1 SERIES
Low-Leakage Pico-Amp Diodes

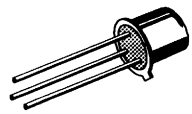
The PAD1 Series of extremely low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. These devices feature leakage currents ranging from -1 pA (PAD1) to -50 pA (PAD50) to support a wide range of applications. The PAD1 Series is well suited for use in applications such as input protection for operational amplifiers. Its hermetically sealed metal can is available with full military processing per MIL-S-19500. (See Section 1.)

PART NUMBER	I_R (pA)
PAD1	-1
PAD5	-5
PAD50	-50

SIMILAR PRODUCTS

- TO-92, See JPAD5 Series
- SOT-23, See SSTPAD5 Series
- Duals, See DPAD1 Series

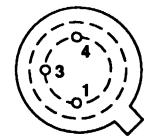
TO-72 (Modified)



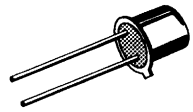
(PAD1, 5)

1 CATHODE
3 ANODE
4 CASE

BOTTOM VIEW



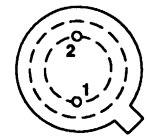
TO-18 (Modified)



(PAD50)

1 CATHODE
2 ANODE

BOTTOM VIEW



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Forward Current	I_F	50	mA
Total Device Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-55 to 125	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	PAD1	-0.3		-1	pA
			PAD5	-1		-5	
			PAD50	-5		-50	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA	PAD1, 5	-60	-45	-120	V
			PAD50	-50	-35		
Forward Voltage Drop	V_F	I_F = 5 mA		0.8		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V f = 1 MHz	PAD1, 5	0.5		0.8	pF
			PAD50	1.5		2	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.

4

PN4117A SERIES
N-Channel JFETs

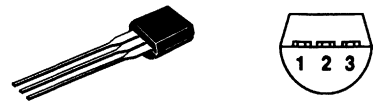
Siliconix incorporated

The PN4117A Series are n-channel JFETs designed to provide ultra-high input impedance. The PN4117A features I_{GSS} of 1 pA maximum and typically operates at 0.2 pA. These devices, therefore, make perfect choices for use as sensitive front-end amplifiers in applications such as microphones, smoke detectors, and precision test equipment. Additionally, its TO-92 plastic package provides a low-cost device compatible with today's automated assembly techniques. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (μS)	I_{DSS} MAX (mA)
PN4117A	-1.8	-40	70	0.09
PN4118A	-3	-40	80	0.24
PN4119A	-6	-40	100	0.60

For additional design information please consult performance curves NT.

TO-92 (TO-226AA) BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-72, See 2N4117A Series
- Dual, See U421 Series
- Chips, See NT Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS							
				PN4117A		PN4118A		PN4119A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-70	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-0.6	-1.8	-1	-3	-2	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		0.03	0.09	0.08	0.24	0.2	0.6	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -10 V, V_{DS} = 0 V	-0.2		-1		-1		-1	pA
		T_A = 100°C	-0.03		-2.5		-2.5		-2.5	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 30 µA	-0.2							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	0.2							
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz		70	210	80	250	100	330	µS
Common-Source Output Conductance	g_{os}				3		5		10	
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz	1.3		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.4		1.5		1.5		1.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	15							$nV/\sqrt{Hz}$

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.

4

PN4391 SERIES
N-Channel JFETs

Siliconix incorporated

The PN4391 Series is the plastic equivalent of our popular 2N4391 Series. These devices are especially well suited for analog switching applications but function efficiently as high-gain amplifiers, particularly at high-frequency. Our low-cost TO-92 packaging offers affordable performance with flexibility for designers, as these devices can be ordered with tape and reel for automated insertion. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (nA)	t_{ON} MAX (ns)
PN4391	-10	30	1	20
PN4392	-5	60	1	20
PN4393	-3	100	1	20

For additional design information please consult the typical performance curves NCB.

TO-92 (TO-226AA) **BOTTOM VIEW**

1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-18, See 2N4391 Series
- SOT-23, See SST4391 Series
- Duals, See 2N5564 Series
- Chips See NCB Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS							
				PN4391		PN4392		PN4393		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 μA, V_{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA		-4	-10	-2	-5	-0.5	-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		50	150	25	100	5	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		T_A = 100°C	-1.0		-200		-200		-200	
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 20 V, V_{GS} = -5 V	0.005						1	nA
		V_{DS} = 20 V, V_{GS} = -7 V	0.005				1			
		V_{DS} = 20 V, V_{GS} = -12 V	0.005		1					
		V_{DS} = 20 V, T_A = 100°C, V_{GS} = -5 V	1						200	
		V_{DS} = 20 V, T_A = 100°C, V_{GS} = -7 V	1				200			
		V_{DS} = 20 V, T_A = 100°C, V_{GS} = -12 V	1		200					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 3 mA	0.25						0.4	V
		V_{GS} = 0 V, I_D = 6 mA	0.30				0.4			
		V_{GS} = 0 V, I_D = 12 mA	0.35		0.4					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			30		60		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							μS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			30		60		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	12		16		16		16	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz, V_{GS} = -5V	3.5						5	
		V_{DS} = 0 V, f = 1 MHz, V_{GS} = -7 V	3.5				5			
		V_{DS} = 0 V, f = 1 MHz, V_{GS} = -12 V	3.5		5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3.0							nV/√Hz
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2		15		15		15	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2		5		5		5	
Turn-Off Time	$t_{d(OFF)}$	PN4391 12mA -12V 800Ω PN4392 6mA -7V 1600Ω PN4393 3mA -5V 3200Ω	6		20		35		50	
	t_f		13		15		20		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 μS, duty cycle ≤ 3%..

4

SST108 SERIES
N-Channel JFETs

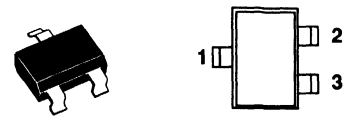
Siliconix incorporated

The SST108 Series is the surface mount equivalent of our J108 device types. It features the lowest $r_{DS(ON)}$ of any SOT-23 JFET device, which makes it especially well suited for analog switching applications. Siliconix' surface mount commitment features low cost performance for a wide range of commercial applications as well as tape and reel options for automatic insertion and high-volume assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST108	-10	8	20	4
SST109	-6	12	20	4
SST110	-4	18	20	4

For further design information please consult the typical performance curves NIP.

SOT-23 **TOP VIEW**



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-52, See 2N5432 Series
- TO-92, See J108 Series
- Chips, See NIP Series Die

PRODUCT MARKING	
SST108	I08
SST109	I09
SST110	I10

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS							
				SST108		SST109		SST110		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 μA, V_{DS} = 0 V	-32	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 μA		-3	-10	-2	-6	-0.5	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		80		40		10		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.01		-3		-3		-3	nA
		T_A = 125°C	-5							
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 10 mA	-0.01							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.02		3		3		3	
		T_A = 125°C	1.0							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, $V_{DS} \leq$ 0.1 V			8		12		18	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	17							mS
Common-Source Output Conductance	g_{os}		600							μS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V f = 1 kHz			8		12		18	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V f = 1 MHz	60		85		85		85	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	11		15		15		15	
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	3.5							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	3							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	1							
Turn-Off Time	$t_{d(OFF)}$	SST108 10mA -12V 150Ω SST109 10mA -7V 150Ω SST110 10mA -5V 150Ω	4							
	t_f		18							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 μS, duty cycle $\leq$ 3%.

4

SST111 SERIES
N-Channel JFETs

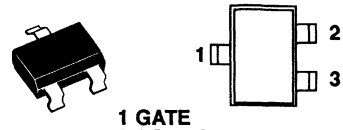
Siliconix incorporated

The SST111 Series is the surface mount equivalent of our J111 device types. Its low cost and $r_{DS(ON)}$ make it a good choice for an all-purpose analog switch, while its high g_{fs} and good high-frequency response also make this product useful in a high-gain amplifier mode. Like all SOT-23 products available from Siliconix, tape and reel capabilities exist for automated assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST111	-10	30	5	4
SST112	-5	50	5	4
SST113	-3	100	5	4

For further design information please consult the typical performance curves NCB.

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-92, See J111 Series
- TO-18, See 2N4391 Series
- Duals, See 2N5564 Series
- Chips, See NCB Series Die

PRODUCT MARKING	
SST111	C11
SST112	C12
SST113	C13

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-35	V
Gate-Source Voltage	V_{GS}	-35	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS							
				SST111		SST112		SST113		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-3	-10	-1	-5		-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		20		5		2		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		T_A = 125°C	-3							
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -12 V	0.005		1		1		1	nA
		T_A = 125°C	3							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = 0.1 V			30		50		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V f = 1 kHz			30		50		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	7		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		5		5		5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 1 mA f = 1 kHz	4							$\frac{nV}{\sqrt{Hz}}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							
Turn-Off Time	$t_{d(OFF)}$	SST111 12.5mA -12V 800Ω SST112 6.25mA -7V 1600Ω SST113 3.1mA -5V 3200Ω	6							
	t_f		15							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

SST174 SERIES
P-Channel JFETs

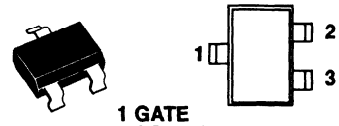
Siliconix incorporated

The SST174 Series are low-cost p-channel analog switches designed to provide low on-resistance and fast switching. They work well in conjunction with Siliconix' SST111 Series for complimentary switching applications. The series features a SOT-23 package and is available tape and reeled to support automated assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (nA)	t_{ON} TYP (ns)
SST174	10	85	-1	25
SST175	6	125	-1	25
SST176	4	250	-1	25
SST177	2.25	300	-1	25

For further design information please consult the typical performance curves PSCIA.

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-18, See 2N5114 Series
- TO-92, See J174 Series
- Chips, See PSCIA Series Die

PRODUCT MARKING	
SST174	S74
SST175	S75
SST176	S76
SST177	S77

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	-50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS					
				SST174		SST175		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -15 V, I_D = -10 nA		5	10	3	6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = -15 V, V_{GS} = 0 V		-20	-135	-7	-70	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = -15 V, I_D = -1 mA	10					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = -15 V, V_{GS} = 10 V	-10					
		T_A = 125°C	-5					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = -0.1 V			85		125	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V	-0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = -15 V, I_D = -1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			85		125	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = -10 V, I_D = -1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r	P/N V_{DD} $V_{GS(OFF)}$ R_L	15					
Turn-Off Time	$t_{d(OFF)}$	SST174 -10 V 12 V 560Ω SST175 -6 V 8 V 1200Ω	10					
	t_f		20					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				SST176		SST177		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −10 nA		1	4	0.8	2.25	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−2	−35	−1.5	−20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	10					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−10					
		T_A = 125°C	−5					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = −0.1 V			250		300	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = −15 V, I_D = −1 mA f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA f = 1 kHz			250		300	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V f = 1 MHz	5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = −10 V, I_D = −1 mA f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r	P/N V_{DD} $V_{GS(OFF)}$ R_L	15					
Turn-Off Time	$t_{d(OFF)}$	SSt176 −6 V 6 V 5600Ω SST177 −6 V 3 V 10000Ω	10					
	t_f		20					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

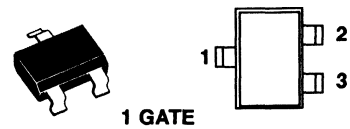
SST201 SERIES
N-Channel JFETs

The SST201 Series is the SOT-23 equivalent of our popular J201 Series. It features low leakage, very low noise, and low cutoff voltage for use with low level power supplies. The SST201 is excellent for battery operated equipment and low current amplifiers. The SST201 Series SOT-23 package affords low cost and compatibility with automated assembly techniques. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
SST201	-1.5	-40	0.5	1
SST202	-4	-40	1	4.5

For further design information please consult the typical performance curves NPA.

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-92, See J201 Series
- TO-18, See 2N4338 Series
- Chips, See NPA Series Die

PRODUCT MARKING	
SST201	P01
SST202	P02

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]			LIMITS					
				SST201		SST202		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA		-0.3	-1.5	-0.8	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.2	1	0.9	4.5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 125°C	-1					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	2					
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, V_{GS} = 0 V f = 1 kHz		0.5		1		mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V f = 1 MHz	4.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	6					$nV/\sqrt{Hz}$

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.

Siliconix incorporated

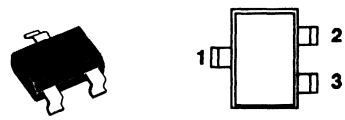
SST304 SERIES
N-Channel JFETs

The SST304 Series of n-channel JFETs is designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise, high gain and provide wide bandwidth.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
SST304	-6	-30	4.5	15
SST305	-3	-30	3	8

For additional design information please see performance curves NH.

SOT-23 **TOP VIEW**



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-92, See J304 Series
- Chips, See NH Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]			LIMITS					
				SST304		SST305		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA		-2	-6	-0.5	-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		5	15	1	8	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-250		-250	pA
		T_A = 100°C	-0.2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-20					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -6 V	2					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 1 V, I_D = 1 mA	200					Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, V_{GS} = 0 V f = 1 kHz		4.5	7.5	3		mS
Common-Source Output Conductance	g_{os}				50		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	2.2					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7					
Common-Source Output Capacitance	C_{oss}		1					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 100 Hz	10					$nV/\sqrt{Hz}$

SPECIFICATIONS[a]			LIMITS (Typical)				
			SST304		SST305		
PARAMETER	SYMBOL	TEST CONDITIONS	100 MHz	400 MHz	100 MHz	400 MHz	UNIT
HIGH-FREQUENCY							
Common-Source Input Conductance	g_{iss}	V_{DS} = 15 V, V_{GS} = 0 V	80	800	80		µS
Common-Source Input Susceptance	b_{iss}		2	7.5	2		mS
Common-Source Output Conductance	g_{oss}		60	80	60		µS
Common-Source Output Susceptance	b_{oss}		0.8	3.6	0.8		mS
Common-Source Forward Transconductance	g_{fs}			4.2	3		
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_G = 5 mA	20	11			dB
Noise Figure	NF	R_G = 1 kΩ	1.7	3.8			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

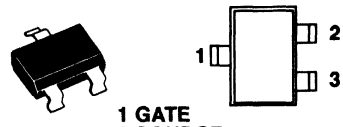
SST308 SERIES
N-Channel JFETs

The SST308 Series is the surface mount equivalent of our popular J308 Series. It features high-gain (> 8000 µS), low noise (typically < 6nV√Hz) and low gate leakage (typically < 2 pA). Of special interest, however, is performance at high frequency. Even at 450 MHz, the SST308 Series offers high power gain and low noise. Tape and reel options are available to support automated assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
SST308	-6.5	-25	8	60
SST309	-4.0	-25	8	30
SST310	-6.5	-25	8	60

For additional design information and a closer look at high-frequency characteristics, please consult performance curves NZB.

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-52, See U309 Series
- TO-92, See J308 Series
- Dual, See U430 Series
- Chips, See NZB Series Die

PRODUCT MARKING	
SST308	Z08
SST309	Z09
SST310	Z10

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS							
				SST308		SST309		SST310		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-1	-6.5	-1	-4	-2	-6.5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		12	60	12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.002		-1		-1		-1	nA
		T_A = 125°C	-0.008		-1		-1		-1	µA
Gate Operating Current	I_G	V_{DG} = 9 V, I_D = 10 mA	-15							pA
Drain Cutoff Current	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	35							Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA , V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA f = 1 kHz	14	8		8		8		mS
Common-Source Output Conductance	g_{os}		110		250		250		250	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = -10 V f = 1 MHz	4		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.9		2.5		2.5		2.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA f = 100 Hz	6							$nV/\sqrt{Hz}$
HIGH FREQUENCY										
Common-Gate Forward Transconductance	g_{fg}	V_{DS} = 10 V I_D = 10 mA	f = 105 MHz	15							mS
			f = 450 MHz	13							
Common-Gate Output Conductance	g_{og}		f = 105 MHz	0.16							
			f = 450 MHz	0.55							
Common-Gate Power Gain[d]	G_{pg}		f = 105 MHz	16							dB
			f = 450 MHz	11.5							
Noise Figure	NF		f = 105 MHz	1.5							
			f = 450 MHz	2.7							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.
d. Gain (G_{pg}) measured at optimum input noise match.

Siliconix incorporated

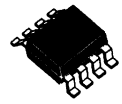
SST404 SERIES
N-Channel JFET Pairs

The SST404 Series is the surface mount equivalent of our U401 Series. It is available in a SO-8 package with three ranges of offset and drift specifications. It features extremely low noise and gate leakage and is intended for use in a wide range of precision instrumentation. For ease of manufacturing, the symmetrical pinout prevents improper orientation. Finally, tape and reel options are available to make this product compatible with automatic assembly methods. (See Section 7.)

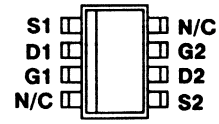
PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS1}-V_{GS2}\rvert$ MAX (mV)
SST404	-50	2	-15	15
SST406	-50	2	-15	40

For additional design information please see performance curves NNR.

SO-8



TOP VIEW



SIMILAR PRODUCTS

- TO-71, See U401 Series
- Chips, See NNR1CHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Drain Voltage		V_{GD}	-50	V
Gate-Source Voltage		V_{GS}	-50	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

SPECIFICATIONS[a]			LIMITS					
				SST404		SST406		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-58	-50		-50		V
	$V_{(BR)G1-G2}$	I_G = ±1 µA, V_{DS} = 0 V, V_{GS} = 0 V	-58	±50		±50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-1.5	-0.5	-2.5	-0.5	-2.5	V
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	3.5	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-25		-25	pA
		T_A = 125°C	-1					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	-2		-15		-15	pA
		T_A = 125°C	-0.8		-10		-10	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250					Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	-1		-2.3		-2.3	V
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 200 µA, f = 1 kHz	1.5	1	2	1	2	mS
Common-Source Output Conductance	g_{os}		1.3		2		2	µS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	4	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		10		20		20	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz			8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 15 V, I_D = 200 µA, f = 10 Hz	10		20		20	$nV/\sqrt{Hz}$
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 200 µA, V_{DG} = 10 V			15		40	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 200 µA, V_{DG} = 10 V, T = -55 to 25°C			25		80	µV/°C
		T = 25 to 125°C			25		80	µV/°C
Common Mode Rejection Ratio[d]	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	102	95				dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

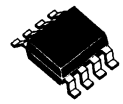
SST440 SERIES
N-Channel JFET Pairs

The SST440 Series are monolithic pairs of JFETs mounted in a single SO-8 package. The SST440 Series features high-speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its SO-8 package is available in tape and reel to support automated assembly. (See Section 7.)

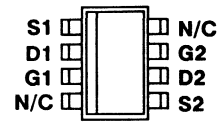
PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS1}-V_{GS2}\rvert$ MAX (mV)
SST440	-25	4.5	-500	10
SST441	-25	4.5	-500	20

For additional design information please see performance curves NNZ.

SO-8



TOP VIEW



SIMILAR PRODUCTS

- TO-71, See U440 Series
- Low Noise, See SST404 Series
- Chips, See NNZ1 Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

SPECIFICATIONS[a]			LIMITS					
				SST440		SST441		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-6	-1	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-500		-500	pA
		T_A = 125°C	-0.2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-500		-500	pA
		T_A = 125°C	-0.2					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		20		200		200	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA f = 100 MHz	5.5					mS
Common-Source Output Conductance	g_{os}		30					µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA f = 1 MHz	3.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA f = 10 kHz	4					$nV/\sqrt{Hz}$
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 5 mA, V_{DG} = 10 V	7		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 5 mA, V_{DG} = 10 V; T = -55 to 25°C	10					µV/°C
		T = 25 to 125°C	10					
Saturation Drain Current Ratio[d]	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98					
Transconductance Ratio[d]	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA f = 1 kHz	0.98					
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	90					dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.
d. Assumes smaller value in the numerator.

Siliconix incorporated

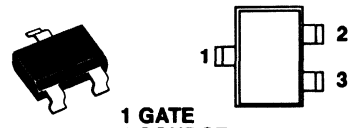
SST4391 SERIES
N-Channel JFETs

The SST4391 Series is the surface mount equivalent of our popular 2N4391 device types. Its low cost and low $r_{DS(on)}$ make it a good choice for an all-purpose analog switch, while its high g_{fs} and good high-frequency response also make this product useful in a high-gain amplifier mode. Like all SOT-23 products available from Siliconix, tape and reel capabilities exist for automated assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST4391	-10	30	5	4
SST4392	-5	60	5	4
SST4393	-3	100	5	4

For additional design information please consult the typical performance curves NCB.

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-18, See 2N4391 Series
- TO-92, See PN4391 Series
- Duals, See 2N5564 Series
- Chips, See NCB Series Die

PRODUCT MARKING	
SST4391	C91
SST4392	C92
SST4393	C93

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-35	V
Gate-Source Voltage	V_{GS}	-35	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SST4391 SERIES

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS							
				SST4391		SST4392		SST4393		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 10 nA		-4	-10	-2	-5	-0.5	-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		50		25		5		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -5 V, V_{DS} = 0 V	-5		-100		-100		-100	pA
		T_A = 125°C	-3		-200		-200		-200	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -10 V	5		100		100		100	
		T_A = 125°C	3		200		200		200	nA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 3 mA	0.25						0.4	V
		V_{GS} = 0 V, I_D = 6 mA	0.3				0.4			
		V_{GS} = 0 V, I_D = 12 mA	0.3		0.4					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			30		60		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			30		60		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	13		16		16		16	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz, V_{GS} = -5V	4						5	
		V_{DS} = 0 V, f = 1 MHz, V_{GS} = -7 V	3.8				5			
		V_{DS} = 0 V, f = 1 MHz, V_{GS} = -12 V	3.5		5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3.0							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							
Turn-Off Time	$t_{d(OFF)}$	SST4391 12mA -12V 800Ω SST4392 6mA -7V 1600Ω SST4393 3mA -5V 3200Ω	6							
	t_f		13							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%..

Siliconix incorporated

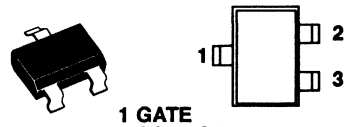
SST4416
N-Channel JFET

The SST4416 is the SOT-23 equivalent of our popular PN4416 Series, designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise, high gain, and provide a wide bandwidth. To support the needs of automated assembly techniques these low-cost devices are available with tape and reel options. (See Section 7.)

For additional design information please see performance curves NH.

$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
-6	-30	4.5	15

SOT-23 **TOP VIEW**



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-92, See J304
- TO-72. See 2N4416
- Chips, See NH Series Die

PRODUCT MARKING	
SST4416	H16

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Power Dissipation	P_D	350	mW
Power Derating		3.18	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-65 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]			LIMITS			
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**TYP[b]**	**MIN**	**MAX**	**UNIT**
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-36	-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-3		-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	10	5	15	mA
Drain Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.002		-1	nA
		T_A = 125°C	-0.6			
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-20			pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -6 V	2			
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	150			Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V	0.7			V
DYNAMIC						
Common-Source Forward Transconductance[c]	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz	6	4.5	7.5	mS
Common-Source Output Conductance[c]	g_{os}		15		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	2.2		4	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		0.8	
Common-Source Output Capacitance	C_{oss}		1		2	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	9			$nV/\sqrt{Hz}$

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 2%.

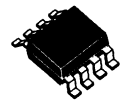
Siliconix incorporated

SSTDPAD5 SERIES
Dual Low-Leakage Pico-Amp Diodes

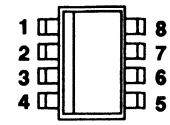
The SSTDPAD5 Series of extremely low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. With two diodes per package, the SSTDPAD5 Series is well suited for use in applications such as input protection for operational amplifiers. Its SO-8 package allows designers to maximize circuit performance while maintaining the objectives of low cost and compact packaging. Tape and reel is available for use with automated assembly techniques. (See Section 7.)

PART NUMBER	I_R (pA)
SSTDPAD5	-5
SSTDPAD100	-100

SO-8



TOP VIEW



1 CATHODE 1
2 CATHODE 1
3 ANODE 1
4 N/C
5 CATHODE 2
6 CATHODE 2
7 ANODE 2
8 N/C

SIMILAR PRODUCTS

- TO-71/TO-78,, See DPAD1 Series
- TO-92, See JPAD5 Series
- SOT-23, See SSTPAD5 Series
- TO-18, See PAD1 Series

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Forward Current	I_F	50	mA
Total Device Dissipation	P_D	400	mW
Storage Temperature	T_{stg}	-55 to 125	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	SSTDPAD5	-2		-5	pA
			SSTDPAD100	-10		-100	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA		-50	-30		V
Forward Voltage Drop	V_F	I_F = 1 mA		0.8		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V, f = 1 MHz		2		4	pF
Differential Capacitance	$\lvert C_{R1} - C_{R2} \rvert$	$V_{R1} = V_{R2}$ = -5 V, f = 1 MHz		0.1		0.5	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.

SSTPAD5 SERIES
Low-Leakage Pico-Amp Diodes

Siliconix incorporated

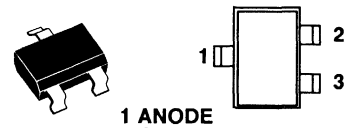
The SSTPAD5 Series of low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. Its SOT-23 package allows designers to maximize circuit performance while maintaining the objectives of low cost and compact packaging. Tape and reel is available for use with automated assembly techniques. (See Section 7.)

PART NUMBER	I_R (pA)
SSTPAD5	-5
SSTPAD100	-100

SIMILAR PRODUCTS

- TO-92, See JPAD5 Series
- TO-18, See PAD1 Series
- Duals, See SSTDPAD5 Series

SOT-23 TOP VIEW



1 ANODE
2 CATHODE
3 CATHODE

PRODUCT MARKING	
SSTPAD5	005
SSTPAD100	100

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Forward Current	I_F	10	mA
Total Device Dissipation	P_D	350	mW
Storage Temperature	T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	SSTPAD5	-1		-5	pA
			SSTPAD100	-10		-100	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA		-60	-35		V
Forward Voltage Drop	V_F	I_F = 1 mA		0.8		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V, f = 1 MHz		1.5		2	pF

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.

Siliconix incorporated

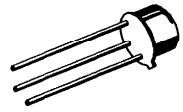
U290 SERIES
N-Channel JFETs

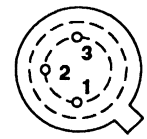
The U290 Series are high-performance JFET analog switches which offer ultra low on-resistance and fast switching. The series features the lowest on-resistance of any JFET in the industry today. Packaged in a hermetically sealed TO-52 can makes the U290 Series suitable for military applications. (See Section 1 for details.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (nA)	t_{ON} MAX (ns)
U290	-10	3	1	35
U291	-4.5	7	1	35

For further design information please consult the typical performance curves NVA.

TO-52 (TO206AC) **BOTTOM VIEW**





1 SOURCE
2 DRAIN
3 GATE & CASE

SIMILAR PRODUCTS

- TO-92, See J105 Series
- Chips, See NVA Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	100	mA
Power Dissipation	P_D	500	mW
Power Derating		4.0	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]			LIMITS					
				U290		U291		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = −1 µA, V_{DS} = 0 V	−35	−30		−30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 3 nA		−4	−10	−1.5	−4.5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		500		200		mA
Gate Reverse Current	I_{GSS}	V_{GS} = −15 V, V_{DS} = 0 V	−0.02		−1		−1	nA
		T_A = 150°C	−0.04		−1		−1	µA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 25 mA	−0.01					nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = −10 V	0.01		1		1	
		T_A = 150°C	0.02		1		1	µA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 mA			30		70	mV
Drain-Source On-Resistance	$r_{DS(ON)}$				3		7	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 25 mA f = 1 kHz	55					mS
Common-Source Output Conductance	g_{os}		5					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA f = 1 kHz			3		7	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V f = 1 MHz	120		160		160	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = −15 V f = 1 MHz	20		30		30	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 25 mA f = 1 kHz	3					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	6		15		15	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	8		20		20	
Turn-Off Time	$t_{d(OFF)}$	U290 30mA −12V 50Ω U291 30mA −7V 50Ω	5		15		15	
	t_f		9		20		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

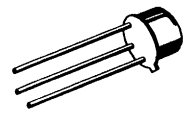
U309 SERIES
N-Channel JFETs

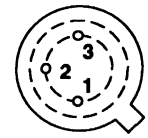
The U309 Series offers superb amplification characteristics. High-gain (> 10,000 μS), low noise (typically < 6 nV√Hz) and low gate leakage (typically < 2 pA) are features of this series. Of special interest, however, is performance at high frequency. Even at 450 MHz, the U309 Series offers high power gain and low noise. Finally, with its TO-52 hermetically sealed package, full military processing is available. (See Section 1.)

For additional design information and a closer look at high-frequency characteristics, please consult performance curves NZB.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
U309	-4	-25	10	30
U310	-6	-25	10	60

TO-52 (TO-206AC) **BOTTOM VIEW**





1 SOURCE
2 DRAIN
3 GATE & CASE

SIMILAR PRODUCTS

- TO-92, See J308 Series
- SOT-23, See SST308 Series
- Dual, See U430 Series
- Chips, See NZB Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	20	mA
Power Dissipation	P_D	500	mW
Power Derating		4	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-65 to 175	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS					
					U309		U310		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V		-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA			-1	-4	-2.5	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V			12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V		-2		-150		-150	nA
			T_A = 125°C	-0.8		-150		-150	
Gate Operating Current	I_G	V_{DG} = 9 V, I_D = 10 mA		-15					pA
Drain Cutoff Current	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA		35					Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA , V_{DS} = 0 V		0.7		1		1	V
DYNAMIC									
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA f = 1 kHz		14	10		10		mS
Common-Source Output Conductance	g_{os}			110		250		250	µS
Common-Source Input Capacitance	C_{gs}	V_{DS} = 10 V, V_{GS} = -10 V f = 1 MHz		4		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{gd}			1.9		2.5		2.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA f = 100 Hz		6					$nV/\sqrt{Hz}$
HIGH FREQUENCY									
Common-Gate Forward Transconductance	g_{fg}	V_{DS} = 10 V I_D = 10 mA	f = 105 MHz	15					mS
			f = 450 MHz	13					
Common-Gate Output Conductance	g_{og}		f = 105 MHz	0.16					
			f = 450 MHz	0.55					
Common-Gate Power Gain[d]	G_{pg}		f = 105 MHz	16	14		14		dB
			f = 450 MHz	11.5	10		10		
Noise Figure	NF		f = 105 MHz	1.5		2		2	
			f = 450 MHz	2.7		3.5		3.5	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.
d. Gain (G_{pg}) measured at optimum input noise match.

Siliconix incorporated

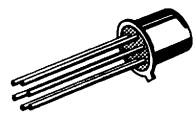
U401 SERIES
N-Channel JFETs

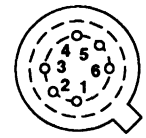
The U401 Series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and drift over temperature specifications. It is targeted for use in a wide range of precision instrumentation applications. The U401 Series has a wide selection of both offset and drift specifications with the prime device, the U401, featuring 5 mV offset and 10 µV/°C drift. The three devices allow designers to make important cost/benefit decisions. This series is available in a TO-71 hermetically sealed package and is available with military screening. (See Section 1.)

For additional design information please see performance curves NNR.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS1}-V_{GS2}\rvert$ MAX (mV)
U401	-50	2	-15	5
U404	-50	2	-15	15
U406	-50	2	-15	40

TO-71 **BOTTOM VIEW**





1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- High-Gain, See 2N5911 Series
- SO-8, See SST404 Series
- Chips, See NNR Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Drain Voltage		V_{GD}	-50	V
Gate-Source Voltage		V_{GS}	-50	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

SPECIFICATIONS[a]			LIMITS							
				U401		U404		U406		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-58	-50		-50		-50		V
	$V_{(BR)G1-G2}$	I_G = ±1 µA, V_{DS} = 0 V, V_{GS} = 0 V	-58	±50		±50		±50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-1.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	V
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-25		-25		-25	pA
		T_A = 125°C	-1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	-2		-15		-15		-15	pA
		T_A = 125°C	-0.8		-10		-10		-10	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 200 µA, f = 1 kHz	1.5	1	2	1	2	1	2	mS
Common-Source Output Conductance	g_{os}		1.3		2		2		2	µS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		5		20		20		20	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3		3	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 15 V, I_D = 200 µA, f = 10 Hz	10		20		20		20	$nV/\sqrt{Hz}$
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 200 µA, V_{DG} = 10 V			5		15		40	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 200 µA, V_{DG} = 10 V, T = -55 to 25°C			10		25		80	µV/°C
		T = 25 to 125°C			10		25		80	µV/°C
Common Mode Rejection Ratio[d]	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	102	95		95		95		dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

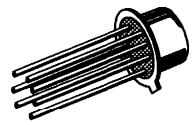
U421 SERIES
N-Channel JFET Pairs

The U421 Series are monolithic pairs of n-channel JFETs designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers operating gate current specified at -250fA, high gain at low operating currents, and tight matching (10 mV for U421). Additionally, its TO-78 package is hermetically sealed and may be screened per MIL-S-19500. (See Section 1.)

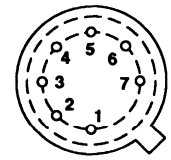
For additional design information please see performance curves NNT.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS1}-V_{GS2}\rvert$ MAX (mV)
U421	-40	0.3	-0.25	10
U423	-40	0.3	-0.25	25

TO-78



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE
5 SOURCE 2
6 DRAIN 2
7 GATE 2

SIMILAR PRODUCTS

- High-Gain, See 2N5911 Series
- Low-Noise, See U401 Series
- Chips, See NNT Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Drain Voltage		V_{GD}	-40	V
Gate-Source Voltage		V_{GS}	-40	
Gate-Gate Voltage		V_{GG}	±40	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	400	mW
	Total		750	
Power Derating	Per Side		3.2	mW/°C
	Total		6	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

U421 SERIES

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				U421		U423		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-60	-40		-40		V
Gate-Gate Breakdown Voltage	V_{GG}	I_G = -1 µA, I_D = 1 nA, I_S = 0	±55	±40		±40		
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-1.2	-0.4	-2	-0.4	-2	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	400	60	1000	60	1000	µA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.6		-1		-1	pA
		T_A = 125°C	-0.3		-1		-1	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 30 µA	-0.2		-0.25		-0.25	pA
		T_A = 125°C	-150		-250		-250	
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 µA	2000					Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 30 µA	-0.8		-1.8		-1.8	V
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7					
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	0.6	0.3	1.5	0.3	1.5	mS
Common-Source Output Conductance	g_{os}		4		10		10	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 30 µA f = 1 kHz	0.2	0.12	0.35	0.12	0.35	mS
Common-Source Output Conductance	g_{os}		0.4		3		3	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz	1.4		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		1.5		1.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 30 µA f = 10 Hz	30		70		70	$nV/\sqrt{Hz}$
Noise Figure	NF	R_G = 10 MΩ			1		1	dB
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 30 µA , V_{DG} = 10 V			10		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 30 µA, V_{DG} = 10 V T= -55 to 25°C			10		40	µV/°C
		T= 25 to 125°C			10		40	
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 30 µA	102	90		80		dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

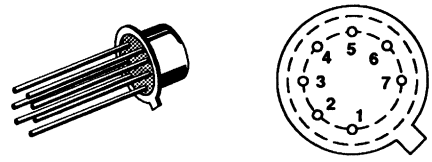
U430 SERIES
N-Channel JFET Pairs

The U430 Series are pairs of matched JFETs assembled in one TO-78 package. They feature high gain, low noise and low gate leakage and are intended for high performance, high slew rate, mixing and differential amplification. Additionally, these devices offer good power gain even as frequencies are increased beyond 250 MHz. The TO-78 package may be processed for military applications. (See Section 1.)

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G TYP (pA)	$\lvert V_{GS1}-V_{GS2}\rvert$ TYP (mV)
U430	-25	10	-15	25
U431	-25	10	-15	25

For additional design information please consult performance curves NZB.

TO-78 BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE
5 SOURCE 2
6 DRAIN 2
7 GATE 2

SIMILAR PRODUCTS

- Low Noise, See U401 Series
- High-Gain, See 2N5911 Series
- Low Leakage, See U421 Series
- Chips, See NZBD Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				U430		U431		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-1	-4	-2	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5		-150		-150	pA
		T_A = 150°C	-10		-150		-150	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-15					pA
		T_A = 150°C	-10					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 10 mA	0.8		1		1	V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA f = 1 kHz	15	10		10		mS
Common-Source Output Conductance	g_{os}		100		250		250	µS
Common-Source Input Capacitance	C_{iss}	V_{GS} = -10 V, V_{DS} = 0 V f = 1 MHz	4.5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		2		2.5		2.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA f = 100 Hz	6					$nV/\sqrt{Hz}$
HIGH FREQUENCY								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA f = 100 MHz	14					mS
Common-Source Output Conductance	g_{os}		0.13					
Power-Match Source Admittance	g_{ig}		12					
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 10 mA , V_{DG} = 10 V	25					mV
Saturation Drain Current Ratio[d]	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.95	0.9	1	0.9	1	
Transconductance Ratio[d]	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 10 mA f = 1 kHz	0.95	0.9	1	0.9	1	
Gate-Source Cutoff Voltage Ratio[d]	$\frac{V_{GS(OFF)1}}{V_{GS(OFF)2}}$	V_{DS} = 10 V, I_D = 1 nA	0.95	0.9	1	0.9	1	
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	-2					pA
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 10 mA	75					dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.
d. Assumes smaller value in the numerator.

Siliconix incorporated

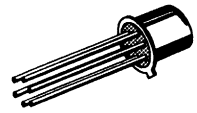
U440 SERIES
N-Channel JFET Pairs

The U440 Series are matched pairs of JFETs mounted in a single TO-71 package. This two chip design reduces parasitic performance at high frequency while ensuring extremely tight matching. The U440 features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its TO-71 hermetically sealed package is available with military screening per MIL-S-19500. (See Section 1.)

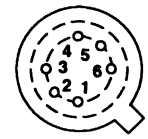
For additional design information please see performance curves NZF.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS1}-V_{GS2}\rvert$ MAX (mV)
U440	-25	4.5	-500	10
U441	-25	4.5	-500	20

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- SO-8, See SST440 Series
- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, See NZFD1 Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Gate-Gate Voltage		V_{GG}	±50	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	250	mW
	Total		350	
Power Derating	Per Side		2	mW/°C
	Total		2.8	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

4

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				U440		U441		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-6	-1	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-500		-500	pA
		T_A = 150°C	-2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-500		-500	pA
		T_A = 125°C	-0.3					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		70		200		200	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA f = 10 kHz	4					$nV/\sqrt{Hz}$
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 5 mA, V_{DG} = 10 V	6		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 5 mA, V_{DG} = 10 V, T = -55 to 25°C	20					µV/°C
		T = 25 to 125°C	20					
Saturation Drain Current Ratio[d]	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.97					
Transconductance Ratio[d]	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA f = 1 kHz	0.97					
Common Mode Rejection Ratio[d]	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	85					dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.
d. Assumes smaller value in the numerator.

Siliconix incorporated

VCR2N, VCR4N, VCR7N
JFET Voltage Controlled Resistors

The VCR2N, VCR4N, and VCR7N line of JFET voltage controlled resistors utilize the JFET's linear output characteristics in the resistive region. This area of operation is around V_{DS} = 0 V and extends for a range up to several hundred millivolts - up to the point I_D begins to saturate. Key to device performance is the predictable r_{DS} change versus V_{GS} bias where:

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	$r_{DS(ON)}$ MIN (Ω)	$r_{DS(ON)}$ MAX (Ω)
VCR2N	-7	-15	20	60
VCR4N	-7	-15	200	600
VCR7N	-5	-15	4000	8000

$$r_{DS}\ \text{bias} \approx \frac{r_{DS}\ (@\ V_{GS} = 0)}{1 - \left|\frac{V_{GS}}{V_{GS(OFF)}}\right|}$$

This series features three n-channel devices with $r_{DS(ON)}$ ranging from 20 - 8000 Ω. All packages are hermetically sealed and may be processed per MIL-S-19500. (See Section 1.)

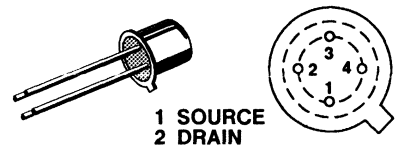
For additional design information please consult typical performance curves as follows:

VCR2N . . . NCB TO-18
VCR4N . . . NPA TO-18
VCR7N . . . NT TO-72

TO-18 **BOTTOM VIEW**

1 SOURCE
2 DRAIN
3 GATE & CASE

TO-72 (TO-206AF) **BOTTOM VIEW**



1 SOURCE
2 DRAIN
3 GATE
4 CASE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-15	V
Gate-Source Voltage	V_{GS}	-15	
Forward Gate Current	I_G	10	mA
Power Dissipation	P_D	300	mW
Power Derating		2	mW/°C
Operating Junction Temperature	T_J	-55 to 175	°C
Storage Temperature	T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS							
				VCR2N		VCR4N		VCR7N		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-55	-15		-15		-15		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 µA		-3.5	-7	-3.5	-7	-2.5	-5	
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V			-5		-0.2		-0.1	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA		20	60	200	600	4000	8000	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7							V
DYNAMIC										
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA f = 1 kHz		20	60	200	600	4000	8000	Ω
Drain-Gate Capacitance	C_{dg}	V_{GD} = -10 V, I_S = 0 mA f = 1 MHz			7.5		3		1.5	pF
Source-Gate Capacitance	C_{sg}	V_{GS} = -10 V, I_D = 0 mA f = 1 kHz			7.5		3		1.5	pF

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.

JFET DIE

Siliconix incorporated

NCB SERIES DIE
N-Channel JFETs

The NCB Series features many of the superior characteristics of JFETs. Its low on-resistance and fast switching make it a good choice for demanding analog switching applications, while its high-gain, low-noise, and impressive frequency response make it the choice for specialized amplifier circuits. Die are supplied with 100% visual sort to criteria of MIL-STD-750C, Method 2072.

For additional design information please consult the typical performance curves NCB.

NCB1CHP*	NCB2CHP*	NCB3CHP*	NCB4CHP*
2N4391	2N4392	2N4858	2N4393
2N4856	2N4857	2N4858A	PN4393
2N4856A	2N4857A	2N4861	J113
2N4859	2N4860	2N4861A	SST4393
2N4859A	2N4860A		SST113
PN4391	PN4392		
J111	J112		
SST111	SST112		
SST4391	SST4392		

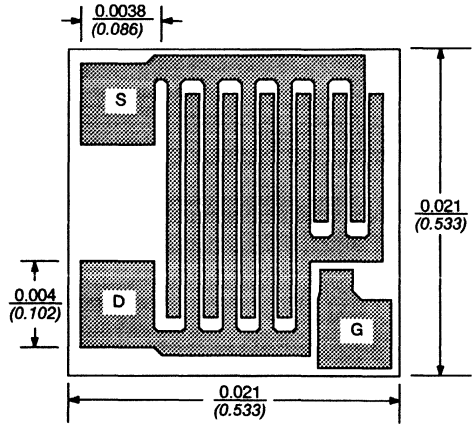
*Meets or exceeds specification for all part numbers listed below

DESIGNED FOR:

- Analog Switches
- Commutators
- Choppers
- Voltage Controlled Resistors
- Integrator Reset Switch

FEATURES

- High Speed t_{ON} < 20 ns
- High Off-Isolation $I_{D(OFF)}$ < 100 pA
- No Offset or Error Voltages Generated by Closed Switch. Purely Resistive. High Isolation Resistance from Driver



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

NCB SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS					
					NCB1CHP		NCB2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-55	-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA			-4	-10	-2	-5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			50	150	25	75	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V		-5					pA
			T_A = 150°C	-13					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA		-5					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 20 V	V_{GS} = -5 V	5					pA
			V_{GS} = -7 V	5					
			V_{GS} = -12 V	5					
		V_{DS} = 20 V, T_A = 150°C	V_{GS} = -5 V	13					nA
			V_{GS} = -7 V	13					
			V_{GS} = -12 V	13					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = 5 mA	0.25					V
			I_D = 6 mA	0.3					
			I_D = 12 mA	0.35					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA				25		40	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V		0.7					V
DYNAMIC									
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz		6					mS
Common-Source Output Conductance	g_{os}			25					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz				25		40	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		12					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = -5 V	3.3					
			V_{GS} = -7 V	3.2					
			V_{GS} = -12 V	2.8					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz		3.0					$nV/\sqrt{Hz}$
SWITCHING									
Turn-On Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V		2					ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L		2					
Turn-Off Time	$t_{d(OFF)}$	NCB1CHP 12mA -12V 800Ω NCB2CHP 6mA -7V 1600Ω		6					
	t_f			19					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.

SPECIFICATIONS[a]				LIMITS					
					NCB3CHP		NCB4CHP		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V		-55	-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA			-0.8	-4	-0.5	-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			8	80	5	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V		-5					pA
			T_A = 150°C	-13					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA		-5					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 20 V	V_{GS} = -5 V	5					
			V_{GS} = -7 V	5					
			V_{GS} = -12 V	5					
		V_{DS} = 20 V, T_A = 150°C	V_{GS} = -5 V	13					nA
			V_{GS} = -7 V	13					
			V_{GS} = -12 V	13					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = 3 mA	0.25					V
			I_D = 5 mA	0.25					
			I_D = 12 mA	0.35					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA				60		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V		0.7					V
DYNAMIC									
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz		6					mS
Common-Source Output Conductance	g_{os}			25					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz				60		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		12					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = -5 V	3.3					
			V_{GS} = -7 V	3.2					
			V_{GS} = -12 V	2.8					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz		3.0					$nV/\sqrt{Hz}$
SWITCHING									
Turn-On Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V		2					ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L		2					
Turn-Off Time	$t_{d(OFF)}$	NCB3CHP 5mA -7V 1910Ω NCB4CHP 3mA -5V 3000Ω		6					
	t_f			19					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

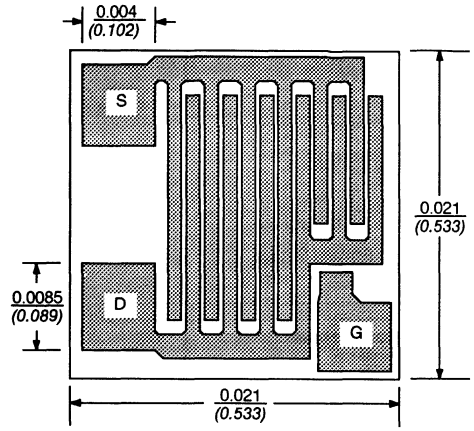
NCBD1 DIE
N-Channel JFET Pair

Siliconix incorporated

The NCBD1 Die is a matched pair of JFETs. This two-chip design reduces parasitic performance at high frequency while ensuring extremely tight matching. The die features high breakdown voltage ($V_{(BR)GSS}$ typically >55 V), high gain (typically >9 mS), and less than 5 mV offset betweeen the two die. Die are supplied with 100% visual sort to criteria of MIL-STD-750C, Method 2072.

NCBD1CHP*
2N5566
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves NCB.



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Analog Switches
- Commutators
- Choppers
- Voltage Controlled Resistors
- Integrator Reset Switch

FEATURES

- High Speed t_{ON} < 20 ns
- High Off-Isolation $I_{D(OFF)}$ < 100 pA
- No Offset or Error Voltages Generated by Closed Switch. Purely Resistive. High Isolation Resistance from Driver

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

NCBD1 DIE

SPECIFICATIONS[a]			LIMITS			
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**TYP[b]**	**MIN**	**MAX**	**UNIT**
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-2	-0.5	-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	20	5	30	mA
Gate Reverse Current[c]	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-5			pA
		T_A = 150°C	-10			nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 2 mA	-3			pA
		T_A = 125°C	-1			nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	50		100	Ω
Gate-Source Voltage	V_{GS}	V_{DS} = 15 V, I_D = 2 mA	-1.2			V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 2 mA, V_{DS} = 0 V	0.7			
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 2 mA, f = 1 kHz	9			mS
Common-Source Output Conductance	g_{os}		35			µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 2 mA, f = 100 MHz	8.5			mS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 2 mA, f = 1 MHz	10			pF
Common-Source Reverse Transfer Capacitance	C_{rss}		2.5			
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 15 V, I_D = 2 mA, f = 10 Hz	12			$nV/\sqrt{Hz}$
Noise Figure	NF	R_G = 10 MΩ	0.1			dB
MATCHING						
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 2 mA, V_{DS} = 15 V	12		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 2 mA, V_{DS} = 15 V; T = -55 to 25°C	25			µV/°C
		T = 25 to 125°C	25			
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 15 V, V_{GS} = 0 V	0.98			
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 15 V, I_D = 2 mA, f = 1 kHz	0.98			
Common Mode Rejection Ratio	CMRR	V_{DD} = 10 to 20 V, I_D = 2 mA	76			dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

NH SERIES DIE
N-Channel JFETs

Siliconix incorporated

The NH Series of n-channel JFETs is designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise (4 dB max @ 400 MHz), high gain (5.5 mS typical @ 400 MHz) and provide wide bandwidth. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

For additional design information please consult the typical performance curves NH.

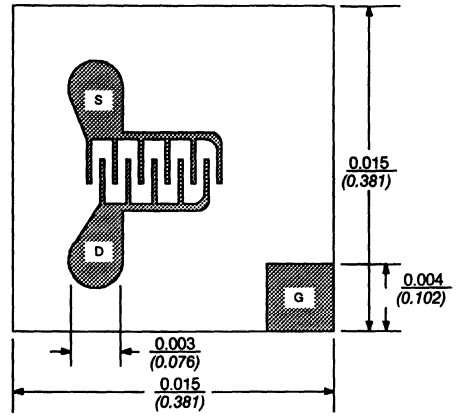
NH1CHP*	NH2CHP*	NH3CHP*
2N5484 J305 SST305	2N5485 2N3819	2N5486 2N4416 2N4416A J304 SST4416 SST304
*Meets or exceeds specification for all part numbers listed below		

DESIGNED FOR:

- VHF/UHF Amplifiers
- Oscillators
- Mixers
- Low Input Capacitance High-Speed Switch

FEATURES

- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wideband High g_{fs}/C_{iss} Ratio



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

SPECIFICATIONS[a]				LIMITS							
					NH1CHP		NH2CHP		NH3CHP		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V		-35	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 10 nA			-0.5	-3	-0.5	-4	-2.5	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V			1	5	4	10	8	15	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V		-0.002							pA
			T_A = 100°C	-0.2							nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA		-20							pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA , V_{DS} = 0 V		0.8							V
DYNAMIC											
Common-Source Forward Transconductance[c]	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz		6							mS
Common-Source Output Conductance[c]	g_{os}			15							µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz		2.2							pF
Common-Source Reverse Transfer Capacitance	C_{rss}			0.7							
Common-Source Output Capacitance	C_{oss}			1							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 15 V, V_{GS} = 0 V f = 100 Hz		10							$\frac{nV}{\sqrt{Hz}}$
HIGH-FREQUENCY											
Common-Source Transconductance	Y_{fs}	V_{DS} = 15 V V_{GS} = 0 V	f = 100 MHz	4.5							mS
			f = 400 MHz	5.5							
Common-Source Output Conductance	Y_{os}		f = 100 MHz	30							µS
			f = 400 MHz	50							
Common-Source Input Conductance	Y_{is}		f = 100 MHz	2							mS
			f = 400 MHz	9							
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_D = 1 mA f = 100 MHz		20							dB
		V_{DS} = 15 V I_D = 4 mA	f = 100 MHz	21							
			f = 400 MHz	13							
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V R_G = 1 MΩ, f = 1 kHz		0.3							
		V_{DS} = 15 V, I_D = 1 mA R_G = 1 MΩ, f = 100 MHz		2							
		V_{DS} = 15 V I_D = 4 mA	f = 100 MHz	1							
		R_G = 1 MΩ	f = 400 MHz	2.5							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%..

4

NIP SERIES DIE
N-Channel JFET

Siliconix incorporated

The NIP Series offers the designer an alternative for true high performance analog switching applications. Good breakdown voltage characteristics coupled with low on-resistance and very fast switching make these devices suitable for a wide range of applications. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NIP1CHP*	NIP2CHP*	NIP3CHP*
2N5432 J108 SST108	2N5433	2N5434 J109 J110 SST109 SST110
*Meets or exceeds specification for all part numbers listed below		

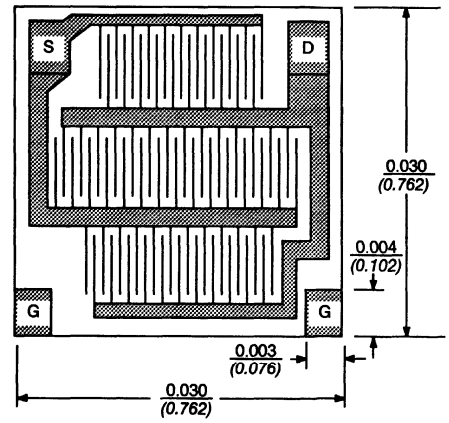
For additional design information please consult the typical performance curves NIP.

DESIGNED FOR:

- Low On-Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

FEATURES

- Low Insertion Loss
- Small Error in Measurement Systems
  $V_{DS(ON)}$ < 50 mV (2N5432)
- High Off-Isolation $I_{D(OFF)}$ < 200 pA
- High Speed $t_{d(ON)}$ < 4 ns
  Low Noise Audio-Frequency Amplification
  $\overline{e}_n$ < 2 nV/√Hz at 1 kHz



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	100	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS							
				NIP1CHP		NIP2CHP		NIP3CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-32	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 3 nA		-4	-10	-3	-9	-2	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		150		100		40		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5							pA
		T_A = 150°C	-10							nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 10 mA	-10							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	10							
		T_A = 150°C	20							nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 mA		2	5		7		10	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	17							mS
Common-Source Output Conductance	g_{os}		600							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V f = 1 kHz			5		7		10	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	20							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		11							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 5 V, I_D = 10 mA f = 1 kHz	3.5							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	0.5							
Turn-Off Time	$t_{d(OFF)}$	NIP1 10mA -12V 145Ω NIP2 10mA -12V 143Ω NIP3 10mA -12V 140Ω	4							
	t_r		18							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

NNR1 DIE
N-Channel JFET Dual Monolithic

Siliconix incorporated

The NNR is a high-performance monolithic dual JFET features extremely low noise, tight offset voltage and drift over temperature specifications. It is targeted for use in a wide range of precision instrumentation applications. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

For additional design information please consult the typical performance curves NNR.

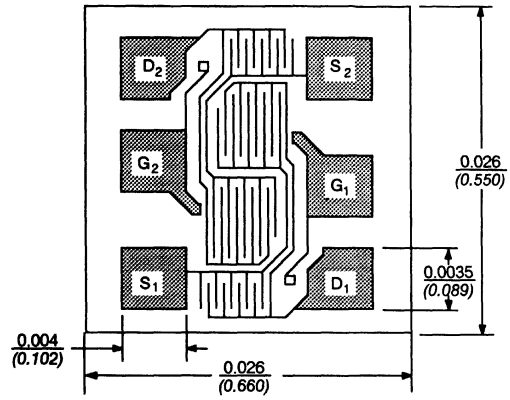
NNR1CHP*
U404 U405 U406
*Meets or exceeds specification for all part numbers listed below

DESIGNED FOR:

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

FEATURES

- Minimum System Error and Calibration
  15 mV Offset (U404)
  100 dB Typical CMRR
- Low Drift with Temperature
  25 μV/°C (U404)
- Simplifies Amplifier Design
  Output Conductance < 2 μS



Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-50	V
Gate-Source Voltage	V_{GS}	-50	
Gate Current	I_G	10	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

NNR1 DIE

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-58	-50		V
	$V_{(BR)G1-G2}$	I_G = ±1 µA, V_{DS} = 0 V, V_{GS} = 0 V	-58	±50		
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-1.5	-0.5	-2.5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	3.5	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2			pA
		T_A = 125°C	-1			nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	-2			pA
		T_A = 125°C	-0.8			nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250			Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	-1			V
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7			
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 200 µA, f = 1 kHz	1.5			mS
Common-Source Output Conductance	g_{os}		1.3			µS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	4			mS
Common-Source Output Conductance	g_{os}		5			µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz	4			pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5			
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 15 V, I_D = 200 µA, f = 10 Hz	10			$nV/\sqrt{Hz}$
MATCHING						
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 200 µA, V_{DG} = 10 V	7		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 200 µA, V_{DG} = 10 V; T = -55 to 25°C	10			µV/°C
		T = 25 to 125°C	10			
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	100			dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

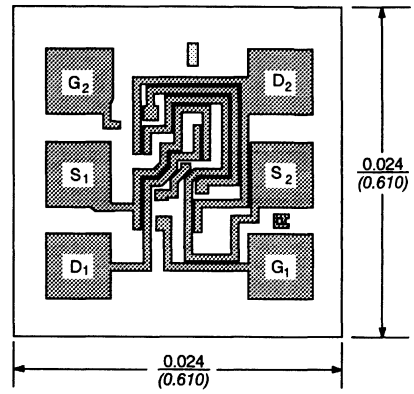
NNT1 DIE
N-Channel JFET Pair

Siliconix incorporated

The NNT die is a monolithic pairs of n-channel JFETs designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers operating gate current specified at -250 fA, high gain at low operating currents, and tight matching. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NNT1CHP*
U423
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves.



Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Ultra-Low Leakage FET Input Op Amps
- pH Meters
- Electrometers

FEATURES

- Ultra-High Input Impedance
- Good Voltage Gain
- Low Noise

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate-Gate Voltage	V_{GG}	±40	
Gate Current	I_G	10	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-60	-40		V
Gate-Gate Breakdown Voltage	V_{GG}	I_G = -1 µA, I_D = 0 nA, I_S = 0	±55	±40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-1.2	-0.4	-2	V
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	400	60	1000	µA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.6			pA
		T_A = 125°C	-0.3			nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 30 µA	-0.2			pA
		T_A = 125°C	-150			pA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 µA	2000			Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 30 µA	-0.8			V
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7			V
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	0.6			mS
Common-Source Output Conductance	g_{os}		4			µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 30 µA, f = 1 kHz	0.2			mS
Common-Source Output Conductance	g_{os}		0.4			µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.4			pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7			pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 30 µA, f = 10 Hz	30			$nV/\sqrt{Hz}$
MATCHING						
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 30 µA, V_{DG} = 10 V	14		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 30 µA, V_{DG} = 10 V, T = -55 to 25°C	25			µV/°C
		T = 25 to 125°C	25			µV/°C
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 30 µA	102			dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

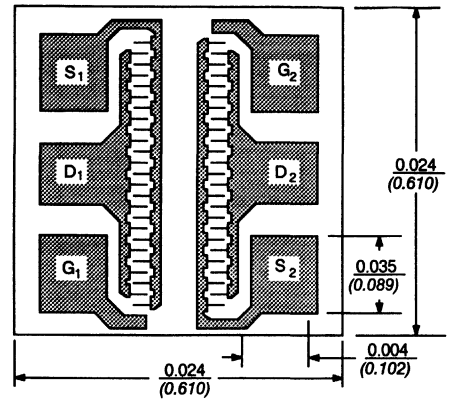
NNZ1 DIE
N-Channel JFET Pair

Siliconix incorporated

The NNZ1 Die is a monolithic pair of JFETs. The die features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NNZ1CHP*
SST440 SST441
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves NNZ.



Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- High-Frequency Amplifiers
- Mixers
- Oscillators
- Hybrid Op Amps

FEATURES

- High Gain
- Low Input Capacitance

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	7	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1			pA
		T_A = 150°C	-2			nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1			pA
		T_A = 125°C	-0.3			nA
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 5 mA	-1.5			V
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7			
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 5 mA, f = 1 kHz	6			mS
Common-Source Output Conductance	g_{os}		20			µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 100 MHz	6			mS
Common-Source Output Conductance	g_{os}		30			µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, I_D = 5 mA, f = 1 kHz	3.5			pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1			
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DS} = 10 V, I_D = 5 mA, f = 10 kHz	4			$nV/\sqrt{Hz}$
Noise Figure	NF	R_G = 100 kΩ	0.1			dB
MATCHING						
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 5 mA, V_{DG} = 10 V	7		10	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 5 mA, V_{DG} = 10 V; T = -55 to 25°C	10			µV/°C
		T = 25 to 125°C	10			
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98			
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.98			
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA, T_A = 125°C	0.005			nA
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	90			dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

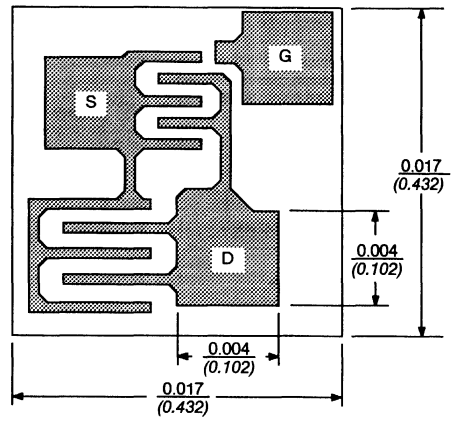
NPA SERIES DIE
N-Channel JFETs

Siliconix incorporated

The NPA Series of n-channel JFETs is designed for sensitive amplifier stages at low to mid frequencies. It features low cut-off voltages to accommodate low-level power supplies and low leakage for improved system accuracy. The NPA1CHP and NPA2CHP are ideal for low current, low battery operation. With their very low noise figure at 1 kHz, system sensitivity will be excellent. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NPA1CHP*	NPA2CHP*	NPA3CHP*	NPA4CHP*
2N4338 J201 SST201	2N4339	2N4340 J202 SST202	2N4341
*Meets or exceeds specification for all part numbers listed below			

For additional design information please consult the typical performance curves NPA.



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Small Signal Amplifiers
- Voltage Controlled Resistors
- Choppers

FEATURES

- Low Noise NF < 1 dB at 1 KHz
- Operation from Low Power Supply Voltages
  $V_{GS(OFF)}$ < 1 V (2N4338)
- High Off-Isolation as a Switch
  $I_{D(OFF)}$ < 50 pA
- High Input Impedance

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-50	V
Gate-Source Voltage	V_{GS}	-50	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS					
				NPA1CHP		NPA2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.1 µA		-0.3	-1	-0.6	-1.8	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		0.2	0.6	0.5	1.5	mA
Drain Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2					pA
		T_A = 150°C	-4					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -5 V	2					
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz	1.5					mS
Common-Source Output Conductance	g_{os}		2					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{DS} = 0 V, V_{GS} = 0 V f = 1 kHz			2500		1700	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	6					$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz, R_G = 1 MΩ	<0.01					dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

NPA SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				NPA3CHP		NPA4CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.1 µA		-1	-3	-2	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		1.2	3.6	4	9	mA
Drain Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2					pA
		T_A = 150°C	-4					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -5 V	2					
		V_{GS} = -10 V	3					
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz	1.5					mS
Common-Source Output Conductance	g_{os}		2					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 kHz			1500		800	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6					$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz, R_G = 1 MΩ	<0.01					dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

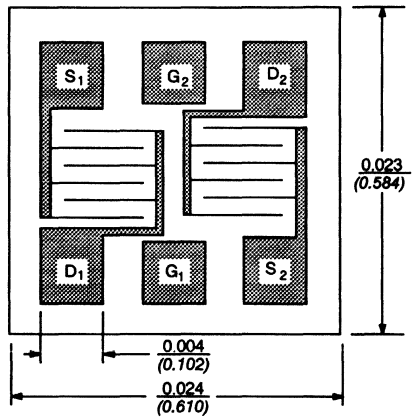
Siliconix incorporated

NQP1 DIE
N-Channel JFET Pair

The NQP1 Die is a monolithic JFET pair designed for high-performance differential amplification for a wide range of precision test instrumentation applications. This die features tight matching specs, low gate leakage for accuracy, and wide dynamic range as I_G is measured at V_{DG} = 20 V. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NQP1CHP*
2N5198 2N5199
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves NQP.



Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- General Purpose Amplifiers

FEATURES

- High Input Impedance

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-50	V
Gate-Source Voltage	V_{GS}	-50	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

NQP1 DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA	-2	-0.7	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	3	0.7	7	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-10			pA
		T_A = 150°C	-20			nA
Gate Operating Current	I_G	V_{DG} = 20 V, I_D = 200 µA	-5			pA
		T_A = 125°C	-0.8			nA
Gate-Source Voltage	V_{GS}	V_{DG} = 20 V, I_D = 200 µA	-1.5			
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	2.5			mS
Common-Source Output Conductance	g_{os}		2			µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 20 µA, f = 1 kHz	0.8			mS
Common-Source Output Conductance	g_{os}		1			µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	3			pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1			
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	9			$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 20 V, V_{GS} = 0 V f = 100 Hz, R_G = 10 MΩ				dB
MATCHING						
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 200 µA, V_{DG} = 20 V	7		10	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 200 µA, V_{DG} = 20 V, T = -55 to 25°C	10			µV/°C
		I_D = 200 µA, V_{DG} = 20 V, T = 25 to 125°C	10			
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 20 V, V_{GS} = 0 V	0.97			
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 20 V, I_D = 200 µA, f = 1 kHz	0.97			
Differential Output Capacitance	$\lvert g_{os1} - g_{os2} \rvert$		0.2			µS
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$	V_{DG} = 20 V, I_D = 200 µA T_A = 125°C	0.1			nA
Common Mode Rejection Ratio	CMRR	V_{DD} = 10 to 20 V, I_D = 200 µA	97			dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

NT SERIES DIE
N-Channel JFETs

The NT Series are n-channel JFETs designed to provide ultra-high input impedance. The series features I_{GSS} of -0.2 pA typical. These devices, therefore, make perfect choices for use as sensitive front-end amplifiers in applications such as microphones, smoke detectors, and precision test equipment. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NT1CHP*	NT2CHP*	NT3CHP*
2N4117A PN4117A	2N4118A PN4118A	2N4119A PN4119A
*Meets or exceeds specification for all part numbers listed below		

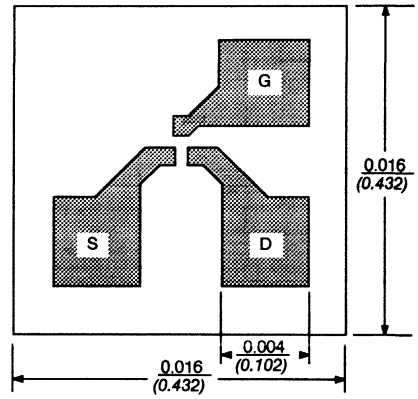
For additional design information please consult the typical performance curves NT.

DESIGNED FOR:

- Ultra-High Input Impedance Amplifier Electrometers:
  - Infrared Detectors
  - Smoke Detectors
  - pH Meters

FEATURES

- Low Power
- High Input Impedance
  I_G < 1 pA (2N4117A)



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

NT SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS						
				NT1CHP		NT2CHP		NT3CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-70	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-0.6	-1.8	-1	-3	-2	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		0.03	0.09	0.08	0.24	0.2	0.6	mA
Drain Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.2							pA
		T_A = 150°C	-0.4							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 30 µA	-0.2							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	0.2							
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	150							µS
Common-Source Output Conductance	g_{os}		1.5							
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz	1.2							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.3							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	15							$nV/\sqrt{Hz}$

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.

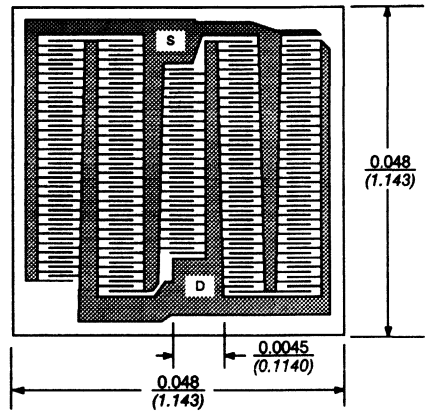
Siliconix incorporated

NVA SERIES DIE
N-Channel JFETs

The NVA Series is a high-performance JFET analog switch designed to offer low on-resistance and fast switching. $r_{DS(ON)}$ <3 Ω is guaranteed with the NVA1CHP which makes this device the lowest of any commercially available JFET. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NVA1CHP*	NVA2CHP*	NVA3CHP*
J105 U290	J106	J107 U291
*Meets or exceeds specification for all part numbers listed below		

For additional design information please consult the typical performance curves NVA.



Gate is backside contact

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Analog Swiches
- Commutators
- Choppers

FEATURES

- Very Low Insertion Loss
  $r_{DS(ON)}$ < 3.0 Ω (NVA1CHP)
- High Off-Isolation

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

NVA SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS							
				NVA1CHP		NVA2CHP		NVA3CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-35	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-4.5	-10	-2	-6	-1.5	-4.5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		500		200		200		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.02							nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 25 mA	-0.01							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.01							
		T_A = 150°C	0.02							µA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = ≤ 0.1 mA			3		6		7	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 25 mA f = 1 kHz	55							mS
Common-Source Output Conductance	g_{os}		5							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA f = 1 kHz			3		6		7	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V f = 1 MHz	120							pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	20							
Equivalent Input Noise Voltage	$\overline{e_n}$	V_{DG} = 10 V, I_D = 25 mA f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	6							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	8							
Turn-Off Time	$t_{d(OFF)}$	NVA1 30mA -12V 50Ω NVA2 30mA -7V 50Ω NVA3 30mA -7V 50Ω	5							
	t_r		9							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

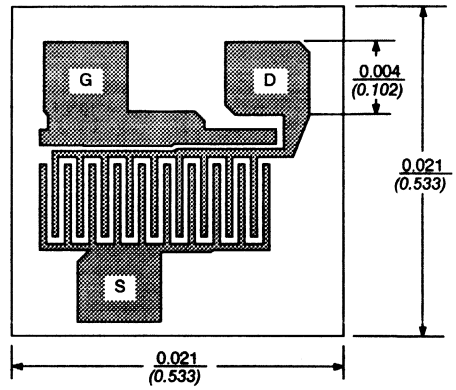
Siliconix incorporated

NZB SERIES DIE
N-Channel JFETs

The NZB Series offers superb amplification characteristics. High-gain (> 10,000 μS), low noise (typically < 6 nV√Hz) and low gate leakage (typically < 2 pA) are features of this series. Of special interest, however, is performance at high frequency. Even at 450 MHz, the NZB Series offers high power gain and low noise. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NZB1CHP*	NZB2CHP*	NZB3CHP*
J308 SST308	U309 J309 SST309	U310 J310 SST310
*Meets or exceeds specification for all part numbers listed below		

For additional design information please consult the typical performance curves NZB.



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- VHF/UHF Amplifers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

FEATURES

- 16 dB at 100 MHz, Common Gate
- 11 dB at 450 MHz, Common Gate

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	20	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

NZB SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS							
					NZB1CHP		NZB2CHP		NZB3CHP		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V		-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA			-1	-6	-1	-4	-2.5	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V			12	60	12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V		-2							nA
			T_A = 125°C	-0.8							µA
Gate Operating Current	I_G	V_{DG} = 9 V, I_D = 10 mA		-15							pA
Drain Cutoff Current	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA		35							Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA , V_{DS} = 0 V		0.7							V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA f = 1 kHz		14							mS
Common-Source Output Conductance	g_{os}			110							µS
Common-Source Input Capacitance	C_{gs}	V_{DS} = 10 V, V_{GS} = -10 V f = 1 MHz		4							pF
Common-Source Reverse Transfer Capacitance	C_{gd}			1.9							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA f = 100 Hz		6							$nV/\sqrt{Hz}$
HIGH FREQUENCY											
Common-Gate Forward Transconductance	g_{fg}	V_{DS} = 10 V I_D = 10 mA	f = 105 MHz	15							mS
			f = 450 MHz	13							
Common-Gate Output Conductance	g_{og}		f = 105 MHz	0.16							
			f = 450 MHz	0.55							
Common-Gate Power Gain[d]	G_{pg}		f = 105 MHz	16							dB
			f = 450 MHz	11.5							
Noise Figure	NF		f = 105 MHz	1.5							
			f = 450 MHz	2.7							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.
d. Gain (G_{pg}) measured at optimum input noise match.

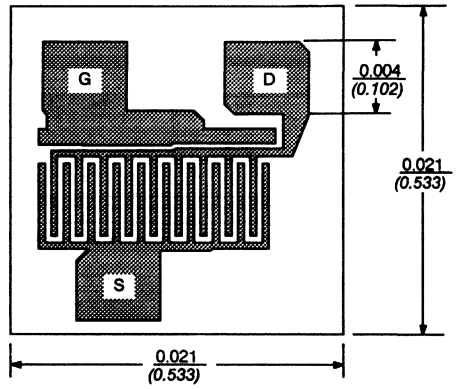
Siliconix incorporated

NZBD SERIES DIE
N-Channel JFET Pairs

The NZBD Series are pairs of matched JFETs assembled in one TO-78 package. They feature high gain, low noise and low gate leakage and are intended for high performance, high slew rate, mixing and differential amplification. Additionally, these devices offer good power gain even as frequencies are increased beyond 250 MHz. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NZBD1CHP*	NZBD2CHP*
U430	U431
*Meets or exceeds specification for all part numbers listed below	

For additional design information please consult the typical performance curves NZB.



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- VHF/UHF Amplifers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

FEATURES

- 16 dB at 100 MHz, Common Gate
- 11 dB at 450 MHz, Common Gate

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 200	°C

NZBD SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				NZBD1CHP		NZBD2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA , V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-1	-4	-2	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	20					mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5					pA
		T_A = 150°C	-10					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-15					pA
		T_A = 150°C	-10					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 10 mA	0.8					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA f = 1 kHz	15					mS
Common-Source Output Conductance	g_{os}		100					µS
Common-Source Input Capacitance	C_{iss}	V_{GS} = -10 V, V_{DS} = 0 V f = 1 MHz	4.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		2					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA f = 100 kHz	6					$nV/\sqrt{Hz}$
HIGH FREQUENCY								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA f = 100 MHz	14					mS
Common-Source Output Conductance	g_{os}		0.13					
Power-Match Source Admittance	g_{ig}		12					
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 10 mA , V_{DG} = 10 V	25					mV
Saturation Drain Current Ratio[d]	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.95					
Transconductance Ratio[d]	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 10 V, I_D = 10 mA f = 1 kHz	0.95					
Gate-Source Cutoff Voltage Ratio	$\frac{V_{GS(OFF)1}}{V_{GS(OFF)2}}$	V_{DS} = 10 V, I_D = 1 nA	0.95					
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	-2					pA
Common Mode Rejection Ratio[d]	CMRR	V_{DD} = 5 to 10 V, I_D = 10 mA	75					dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.
d. Assumes smaller value in the numberator.

Siliconix incorporated

NZF SERIES DIE
N-Channel JFETs

The NZF Series of n-channel JFETs provides good general purpose amplifiers for a wide range of test and instrumentation applications. This series features low-leakage (I_{GSS} < 100 pA), high gain (g_{fs} > 7 mS for NZF3CHP), and low noise. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NZF1CHP*	NZF2CHP*	NZF3CHP*
J210	J211	J212
*Meets or exceeds specification for all part numbers listed below		

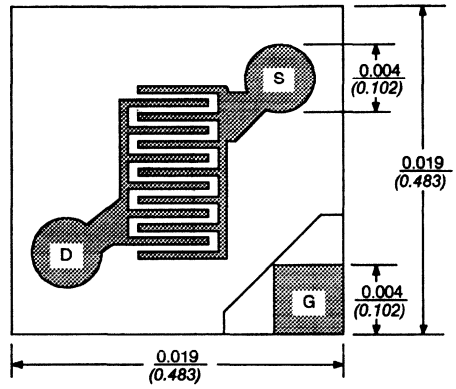
For additional design information please consult the typical performance curves NZF.

DESIGNED FOR:

- High Frequency Amplifiers
- Mixers
- Oscillators

FEATURES

- High Power Gain
- Low Noise



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

NZF SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS							
				NZF1CHP		NZF2CHP		NZF3CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA		-1	-3	-2.5	-4.5	-4	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		2	15	7	20	15	40	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1							pA
		T_A = 125°C	-0.5							nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-1							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	1							
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz	7							mS
Common-Source Output Conductance	g_{os}		60							µs
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	4							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz	5							$nV/\sqrt{Hz}$

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.

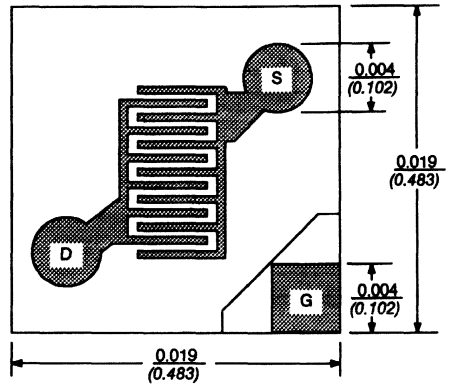
Siliconix incorporated

NZFD1 DIE
N-Channel JFETs

The NZFD1 Die is a JFET matched pair. This two-chip design reduces parasitic performance at high-frequency while ensuring extremely tight matching. The NZFD1 Die features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

For additional design information please consult the typical performance curves NZF.

NZFD1CHP*
2N5912 U440 U441
*Meets or exceeds specification for all part numbers listed below



Gate also backside contact

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- High Frequency Amplifiers
- Mixers
- Oscillators

FEATURES

- High Power Gain
- Low Noise

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate-Gate Voltage	V_{GG}	±80	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

NZFD1 DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	7	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1			pA
		T_A = 150°C	-2			nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1			pA
		T_A = 125°C	-0.3			nA
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 5 mA	-1.5			V
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7			
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6			mS
Common-Source Output Conductance	g_{os}		70			µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 100 MHz	5.8			mS
Common-Source Output Conductance	g_{os}		90			µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	3			pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1			
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4			$nV/\sqrt{Hz}$
Noise Figure	NF	R_G = 100 kΩ	0.1			dB
MATCHING						
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	I_D = 5 mA, V_{DG} = 10 V	4		10	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	I_D = 5 mA, V_{DG} = 10 V; T = -55 to 25°C	15			µV/°C
		T = 25 to 125°C	15			
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98			
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.98			
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA, T_A = 125°C	0.005			nA
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	85			dB

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

PSCIA SERIES DIE
P-Channel JFETs

The PSCIA Series is a p-channel JFET analog switch designed to complement our n-channel NCB Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

PSCIA1CHP*	PSCIA2CHP*	PSCIA3CHP*	PSCIA4CHP*
2N5114 J174 SST174	2N5115 J175 SST175	2N5116 J176 SST176	J177 SST177
*Meets or exceeds specification for all part numbers listed below			

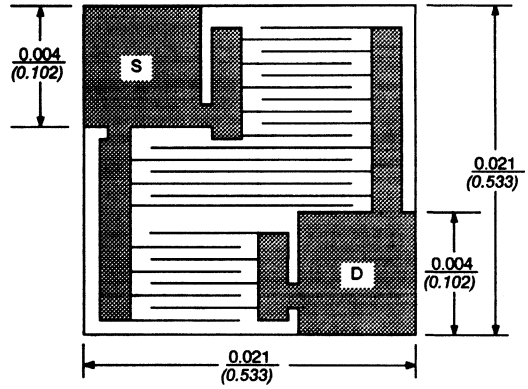
For additional design information please consult the typical performance curves PSCIA.

DESIGNED FOR:

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

FEATURES

- Low Insertion Loss in Switching Systems
  $r_{DS(ON)}$ < 75 Ω (2N5114)
- Short Sample and Hold Aperture Time
  C_{rss} < 7 pF
- High Off-Isolation $I_{D(OFF)}$ < 500 pA



Gate backside contact

Nominal Thickness
0.009 inches
0.228 mm

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

PSCIA SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				PSCIA1CHP		PSCIA2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -15 V, I_D = -1 nA		5	10	3	6	
Saturation Drain Current[c]	I_{DSS}	V_{GS} = 0 V, V_{DS} = -18 V		-30	-90			mA
		V_{DS} = -15 V				-15	-60	
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	5					pA
		T_A = 150°C	0.01					µA
Gate Operating Current	I_G	V_{DG} = -15 V, I_D = -1 mA	-5					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = -15 V, V_{GS} > $V_{GS(OFF)}$	-10					
		T_A = 150°C	-0.02					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = -1 mA			75		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V	-0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = -15 V, I_D = -1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			75		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} > $V_{GS(OFF)}$, f = 1 MHz	5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = -10 V, I_D = -1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	6					ns
	t_r	P/N V_{DD} $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	10					
Turn-Off Time	$t_{d(OFF)}$	PSCIA1 -10V -15mA 20V 130Ω PSCIA2 -6V -7mA 12V 900Ω	6					
	t_r		15					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 2%.

PSCIA SERIES DIE

SPECIFICATIONS[a]			LIMITS					
				PSCIA3CHP		PSCIA4CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -15 V, I_D = -10 nA		1	4	0.3	2.25	
Saturation Drain Current[c]	I_{DSS}	V_{GS} = 0 V, V_{DS} = -18 V						mA
		V_{GS} = 0 V, V_{DS} = -15 V		-5	-25	-1.5	-20	
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	5					pA
		V_{GS} = -20 V, V_{DS} = 0 V, T_A = 150°C	0.01					µA
Gate Operating Current	I_G	V_{DG} = -15 V, I_D = -1 mA	-5					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = -15 V, V_{GS} > $V_{GS(OFF)}$	-10					
		V_{DS} = -15 V, V_{GS} > $V_{GS(OFF)}$, T_A = 150°C	-0.02					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = -1 mA			150		300	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V	-0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = -15 V, I_D = -1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			175		300	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} > $V_{GS(OFF)}$, f = 1 MHz	5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = -10 V, I_D = -1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	6					ns
	t_r	P/N V_{DD} $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	10					
Turn-Off Time	$t_{d(OFF)}$	PSCIA3 -6V -3mA 8V 2000Ω PSCIA4 -6V -3mA 8V 2000Ω	6					
	t_f		15					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 2%.

4

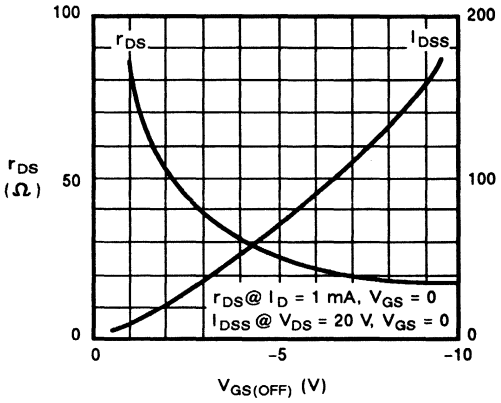
JFET
PERFORMANCE CURVES

NCB
N-Channel JFETs

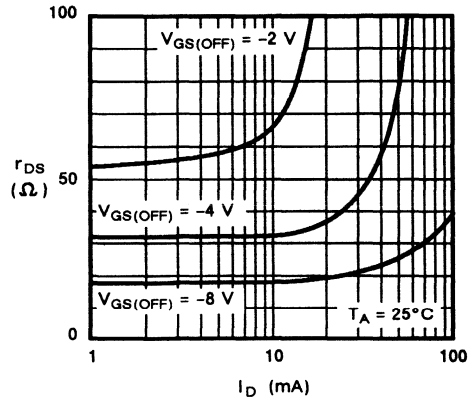
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• J111, J112, J113 PN4391, PN4392, PN4393
Single	SOT-23	• SST111, SST112, SST113, SST4391, SST4392, SST4393
Single	TO-18	• 2N4391, 2N4392, 2N4393 VCR2N
Dual	TO-71	• 2N5564, 2N5565, 2N5566
Single	Chip	• Available as NCB1CHP, NCB2CHP, NCB3CHP, NCB4CHP
Dual	Chip	• Available as NCBD1CHP

TYPICAL CHARACTERISTICS

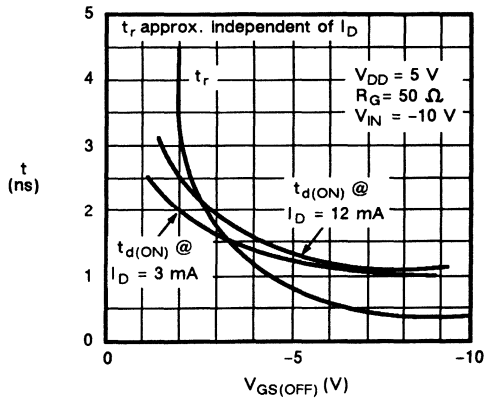
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



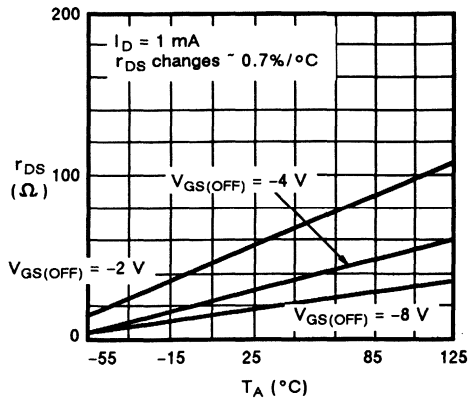
On-Resistance vs. Drain Current



Turn-On Switching



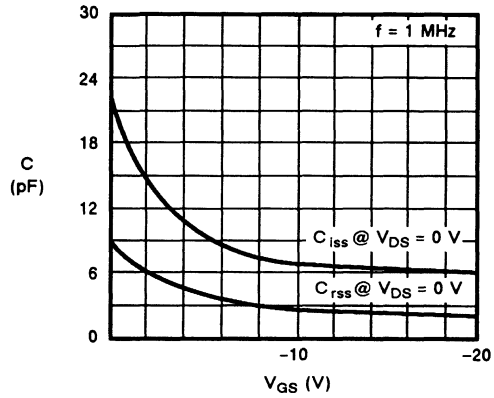
On-Resistance vs. Temperature



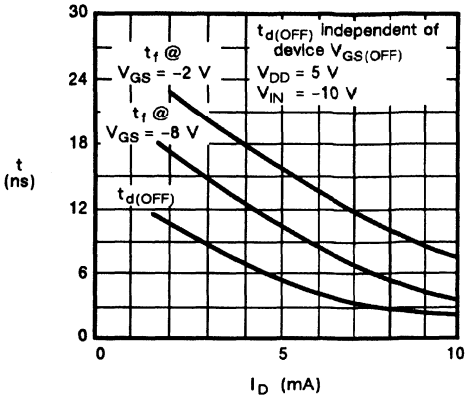
4

TYPICAL CHARACTERISTICS

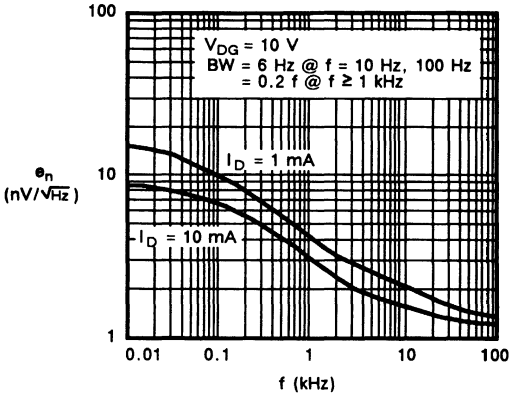
Capacitance vs. Gate-Source Voltage



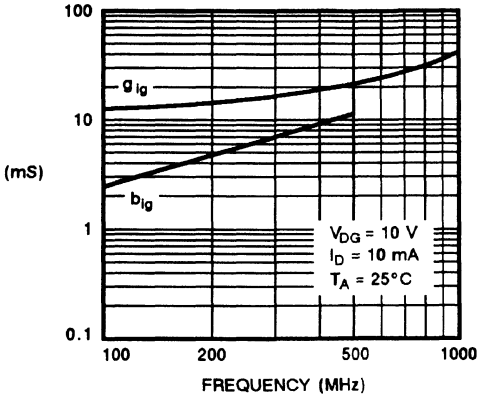
Turn-Off Switching



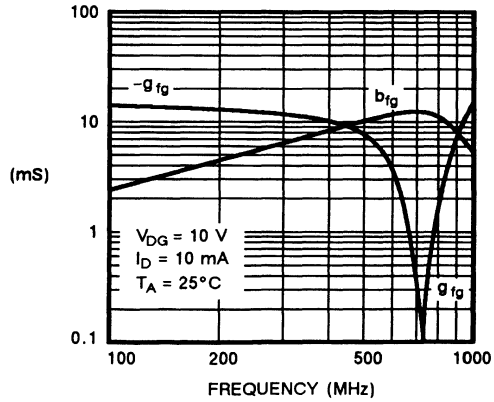
Noise Voltage vs. Frequency



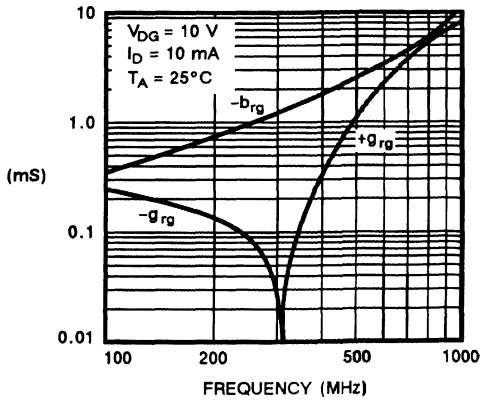
Common-Gate Input Admittance



Common-Gate Forward Admittance

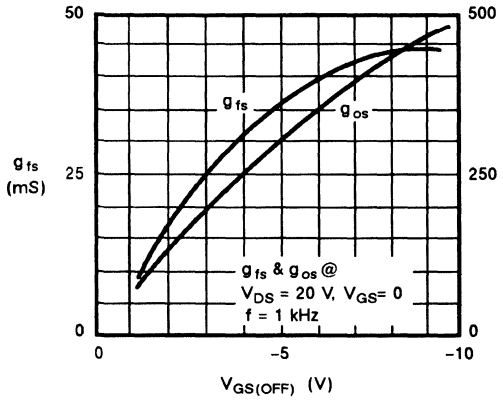


Common-Gate Reverse Admittance

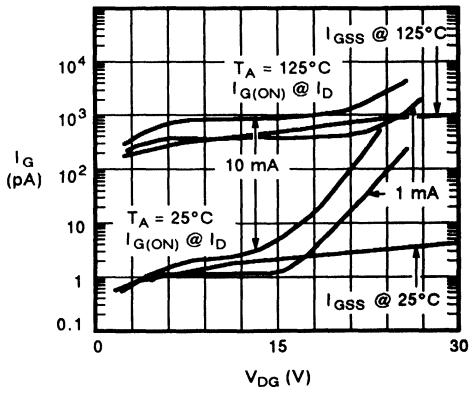


TYPICAL CHARACTERISTICS

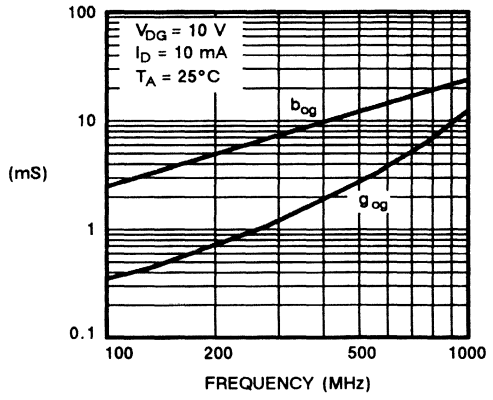
Forward Transconductance & Output Conductance vs. Gate-Source Cutoff Voltage



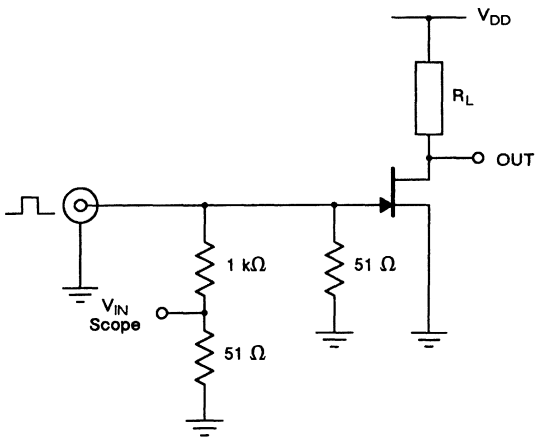
Operating Gate Current



Common-Gate Output Admittance



SWITCHING CIRCUIT



4

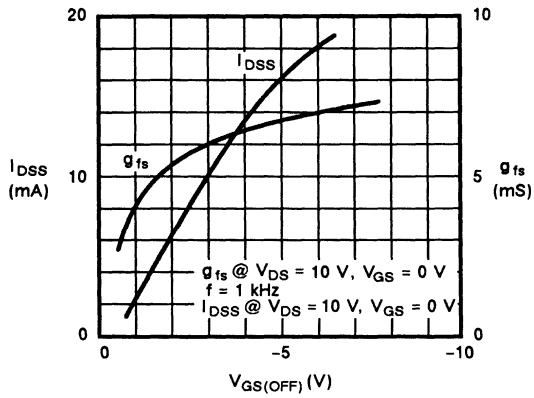
NH
N-Channel JFETs

Siliconix incorporated

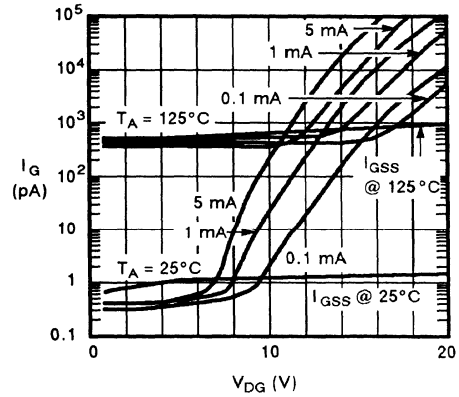
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• 2N5484, 2N5485, 2N5486 J304, J305
Single	SOT-23	• SST4416
Single	TO-72 (TO-206AF)	• 2N4416, 2N4416A
Single	Chip	• Available as NH1CHP, NH2CHP, NH3CHP

TYPICAL CHARACTERISTICS

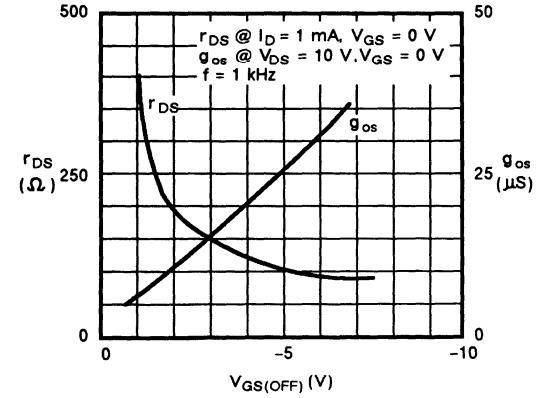
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



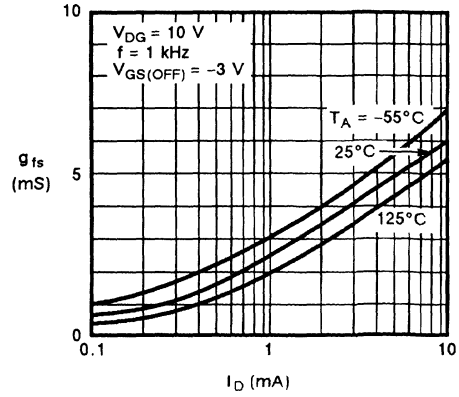
Leakage Current vs. Drain Voltage



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



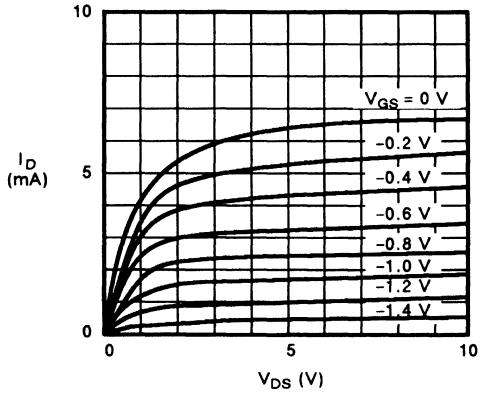
Common-Source Forward Transconductance vs. Drain Current



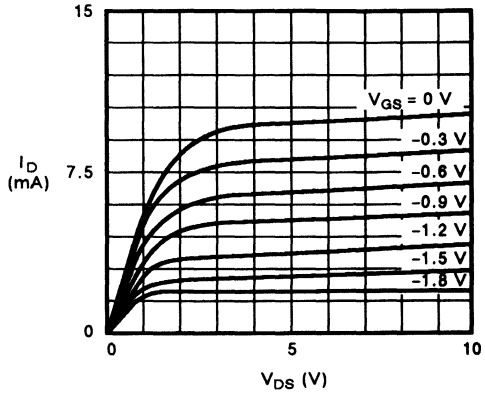
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

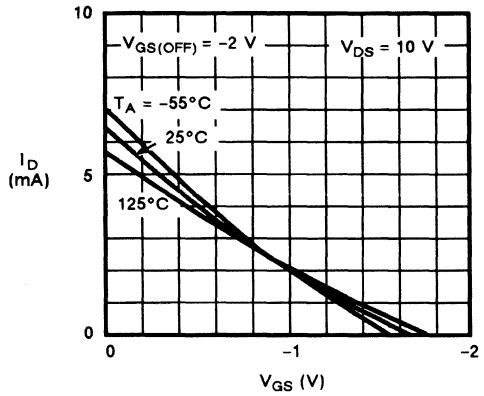
Output Characteristics ($V_{GS(OFF)} = -2$ V)



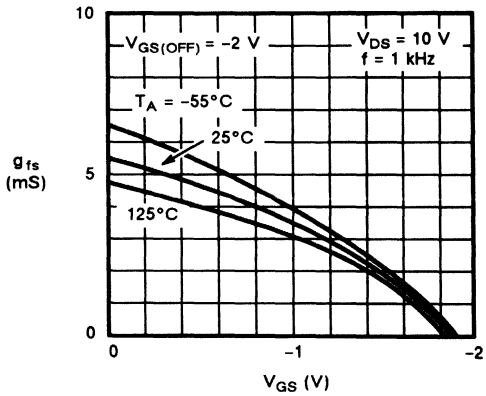
Output Characteristics ($V_{GS(OFF)} = -3$ V)



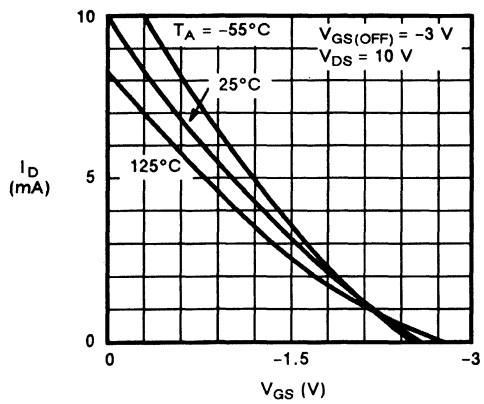
Transfer Characteristics



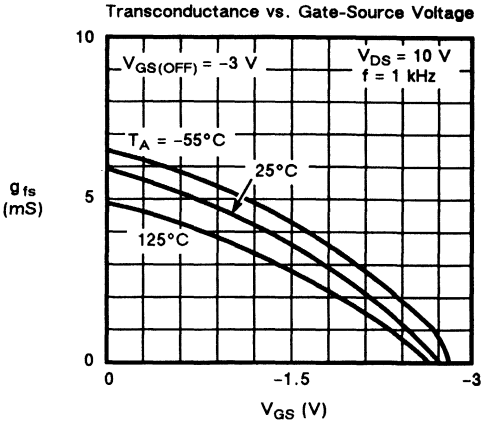
Transconductance vs. Gate-Source Voltage



Transfer Characteristics



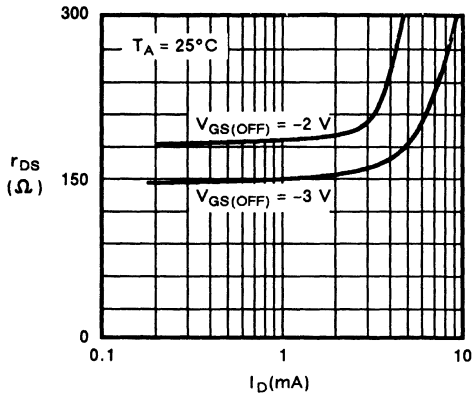
Transconductance vs. Gate-Source Voltage



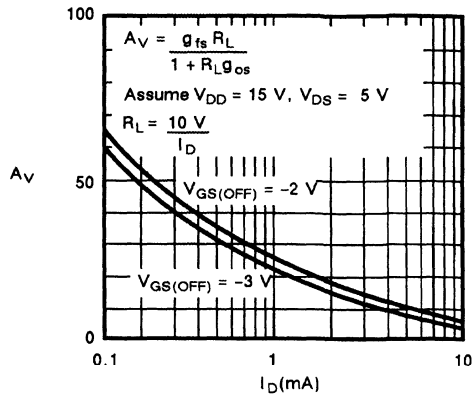
4

TYPICAL CHARACTERISTICS (Cont'd)

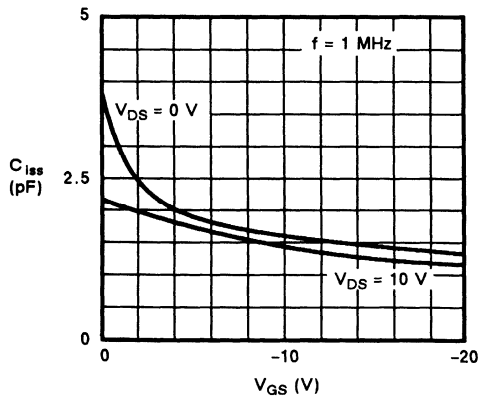
On-Resistance vs. Drain Current



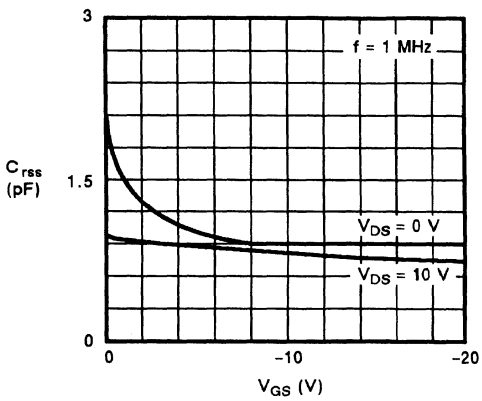
Circuit Voltage Gain vs. Drain Current



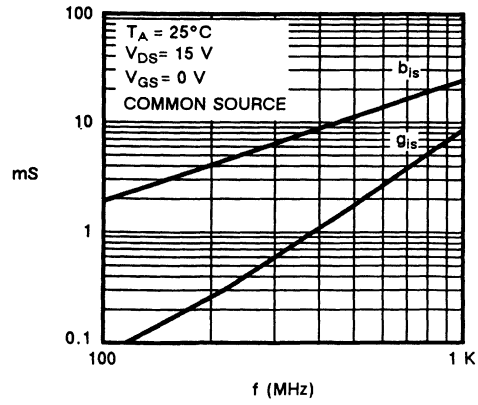
Common-Source Input Capacitance vs. Gate-Source Voltage



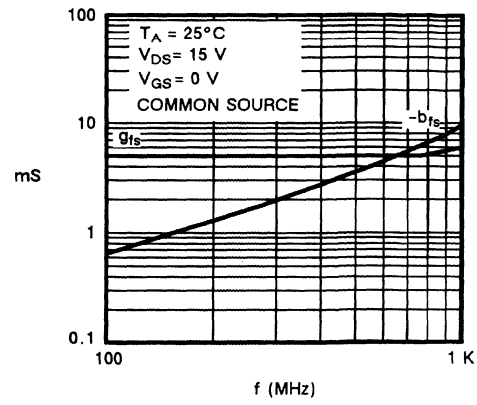
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Input Admittance

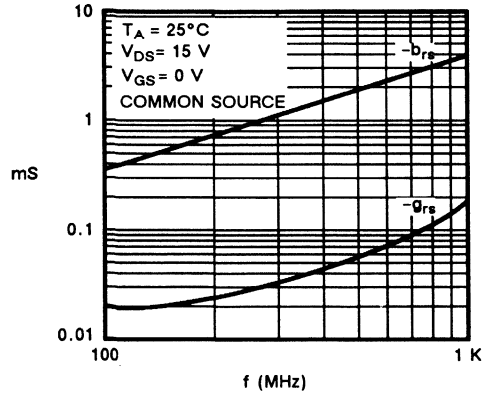


Forward Admittance

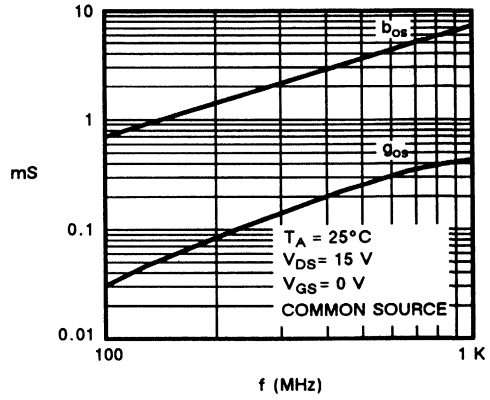


TYPICAL CHARACTERISTICS (Cont'd)

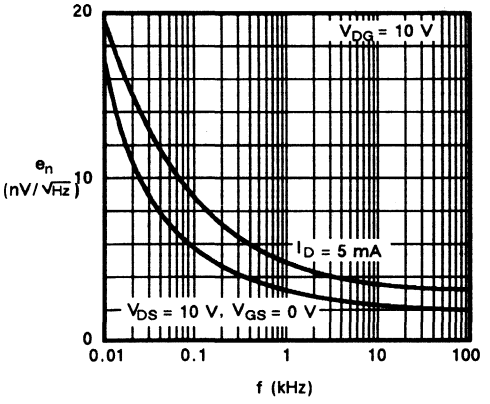
Reverse Admittance



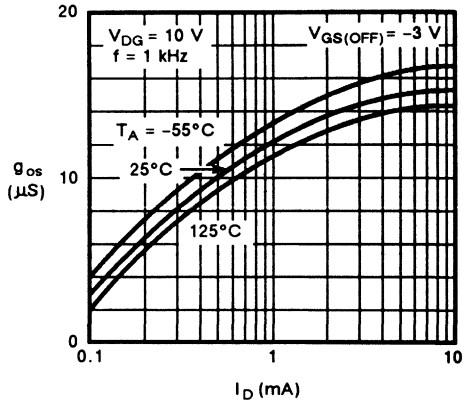
Output Admittance



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



4

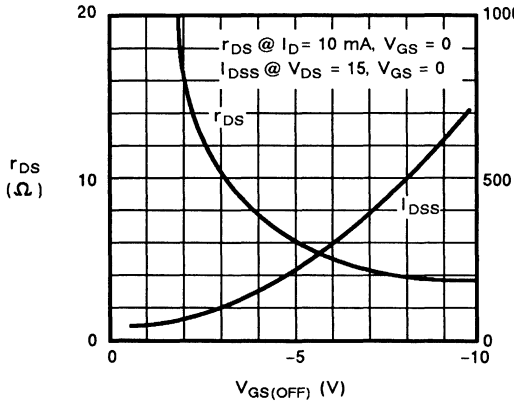
NIP
N-Channel JFET
Current Regulator Diodes

Siliconix incorporated

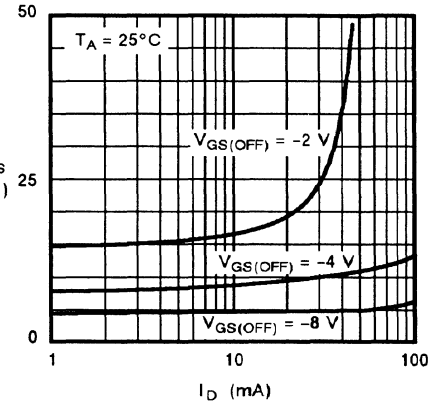
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• J108, J109, J110
Single	SOT-23	• SST108, SST109, SST110
Single	TO-52 (TO-206AC)	• 2N5432, 2N5433, 2N5434
Single	Chip	• Available as NIP1CHP, NIP2CHP, NIIP3CHP

TYPICAL CHARACTERISTICS

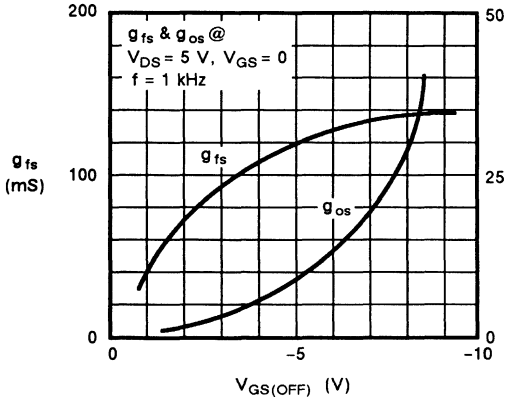
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



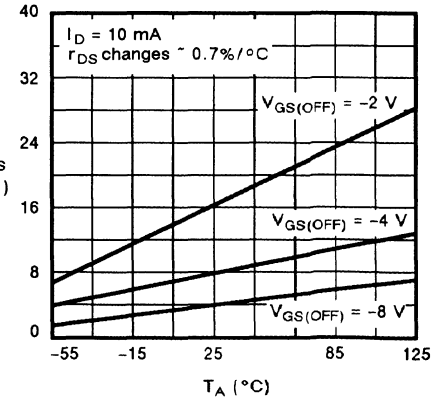
On-Resistance vs. Drain Current



Forward Transconductance & Output Conductance vs. Gate-Source Cutoff Voltage



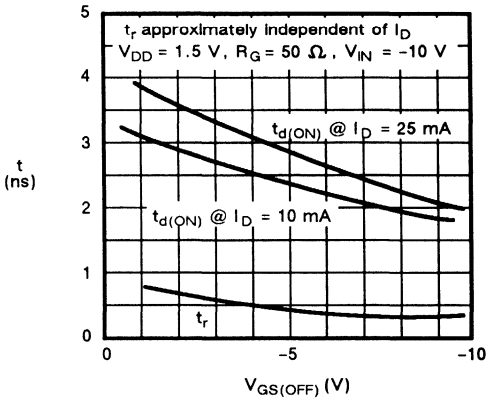
On-Resistance vs. Temperature



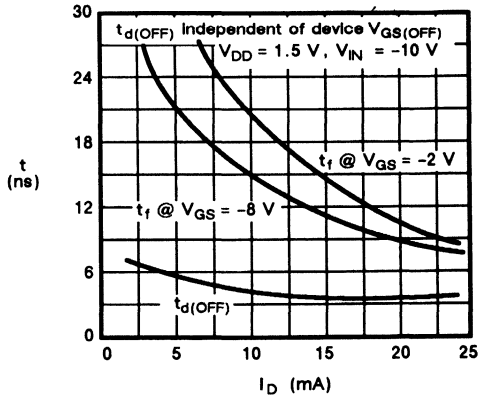
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

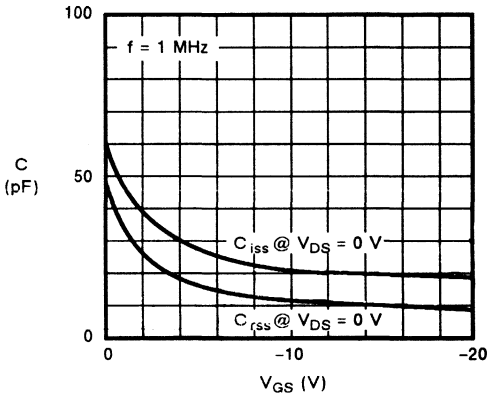
Turn-On Switching



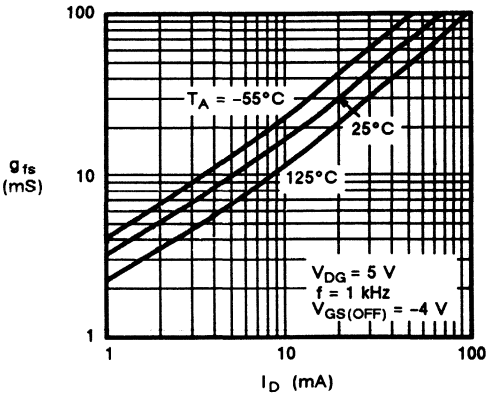
Turn-Off Switching



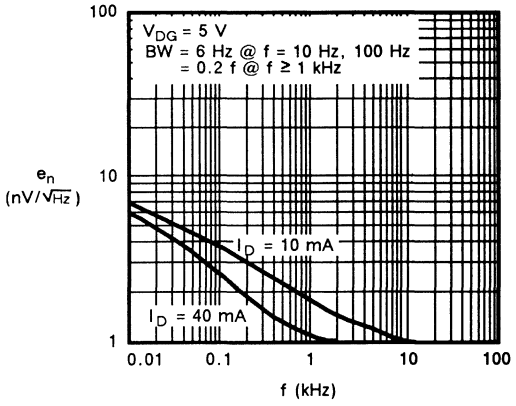
Capacitance vs. Gate-Source Voltage



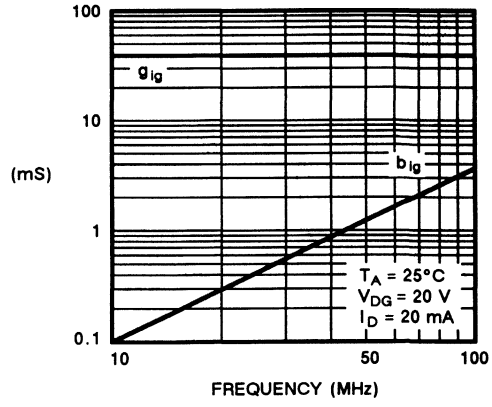
Transconductance vs. Drain Current



Noise Voltage vs. Frequency



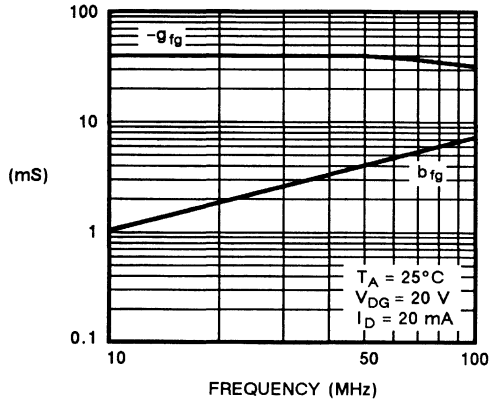
Common Gate Input Admittance



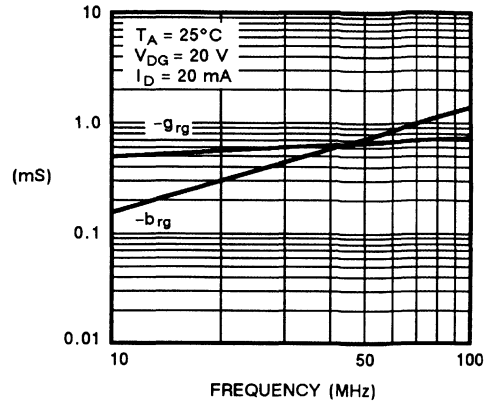
4

TYPICAL CHARACTERISTICS (Cont'd)

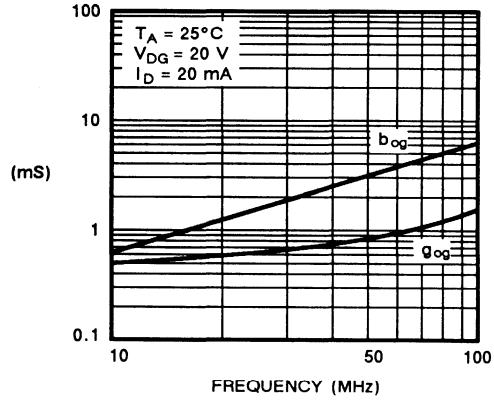
Common Gate Forward Admittance



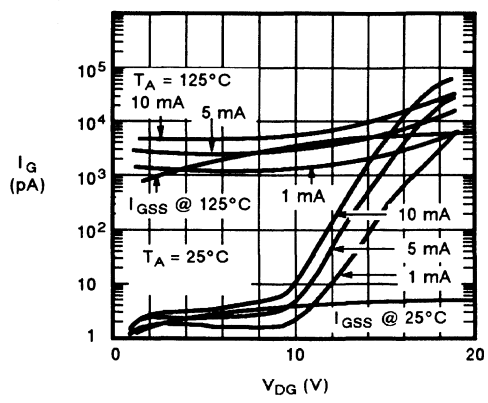
Common Gate Reverse Admittance



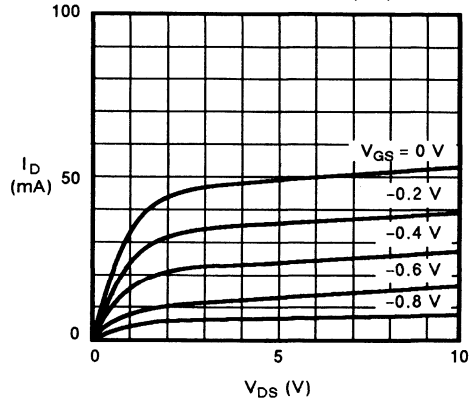
Common Gate Output Admittance



Operating Gate Current



Output Characteristics ($V_{GS(OFF)}$ = -2 V)

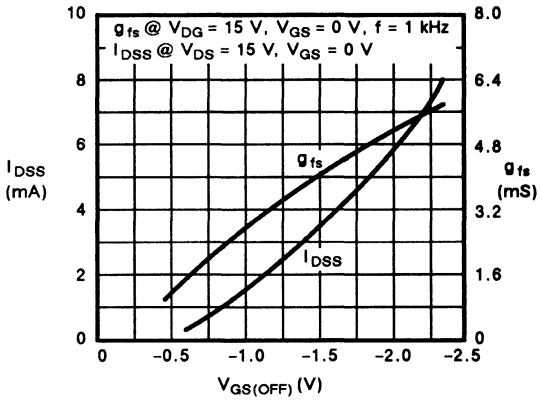


NNR
N-Channel JFET Dual Monolithic

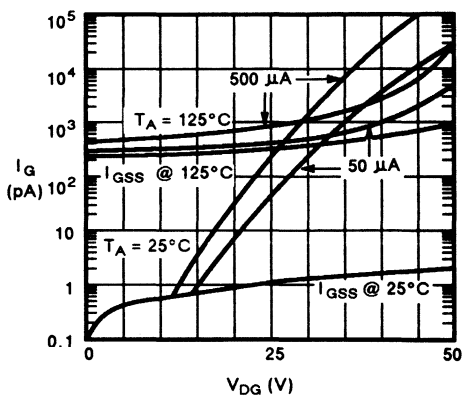
TYPE	PACKAGE	DEVICE
Dual	SOIC-8	• SST404, SST406
Dual	TO-71	• U401, U404, U406
Dual	Chip	• Available as NNR1CHP

TYPICAL CHARACTERISTICS

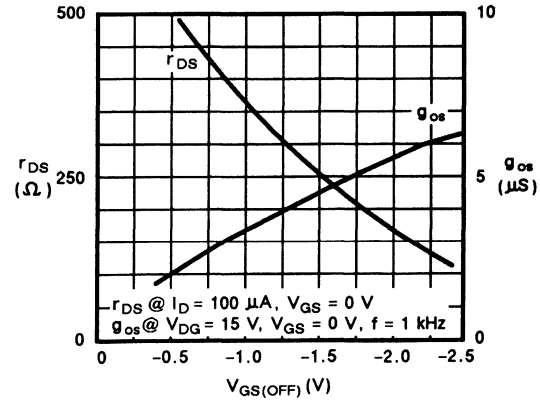
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



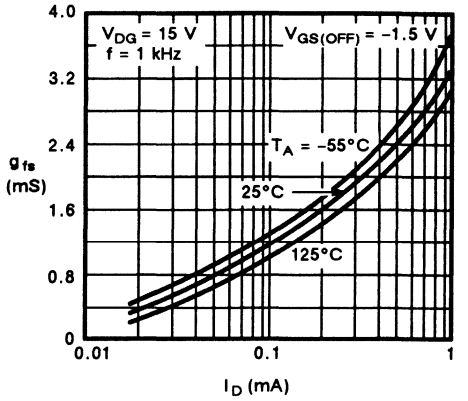
Operating Gate Current



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



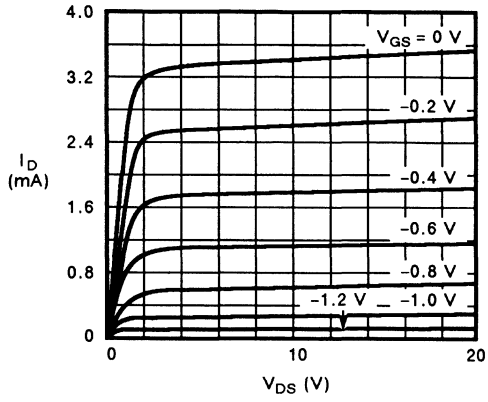
Common-Source Forward Transconductance vs. Drain Current



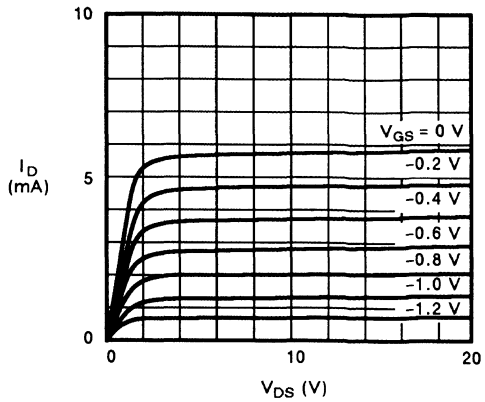
4

TYPICAL CHARACTERISTICS

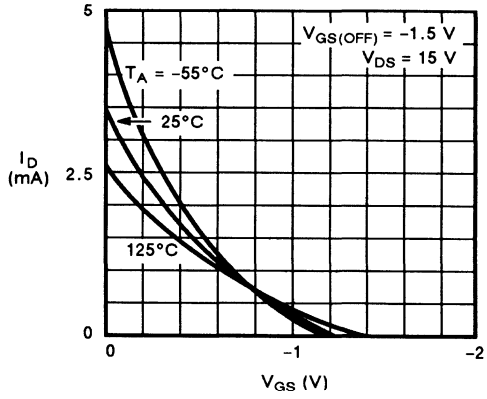
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



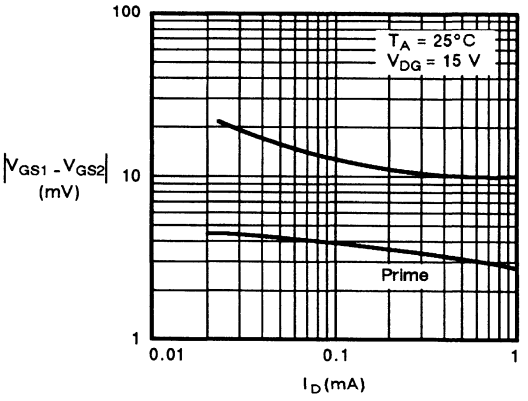
Output Characteristics ($V_{GS(OFF)}$ = -2 V)



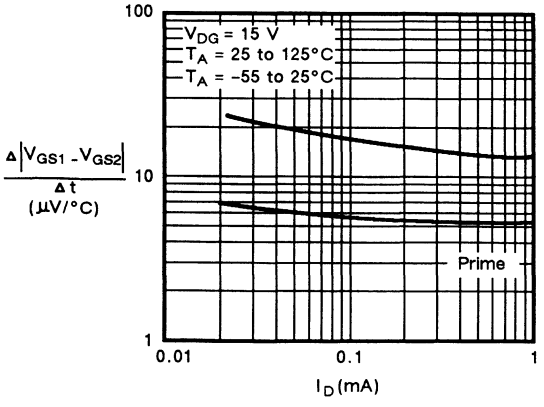
Transfer Characteristics



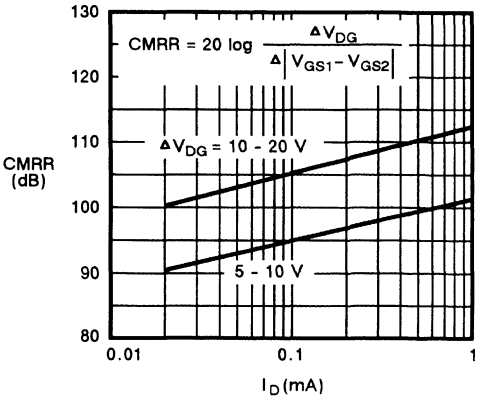
Gate-Source Differential Voltage vs. Drain Current



Voltage Differential with Temperature vs. Drain Current

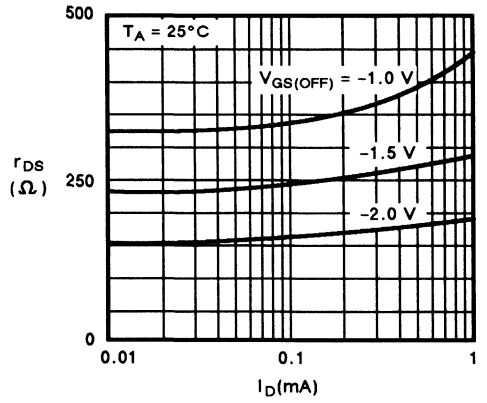


Common Mode Rejection Ratio vs. Drain Current

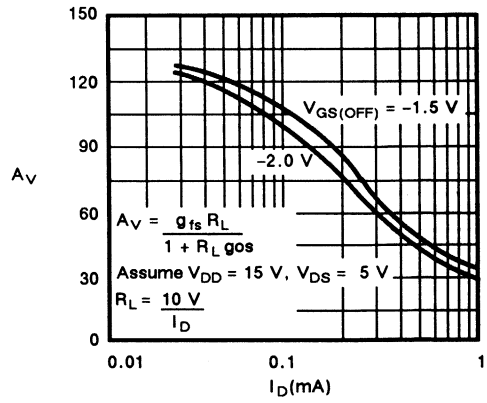


TYPICAL CHARACTERISTICS

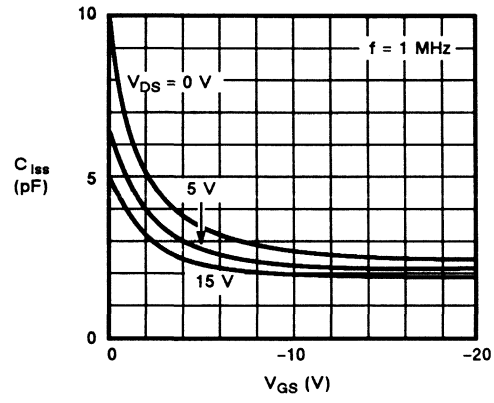
On-Resistance vs. Drain Current



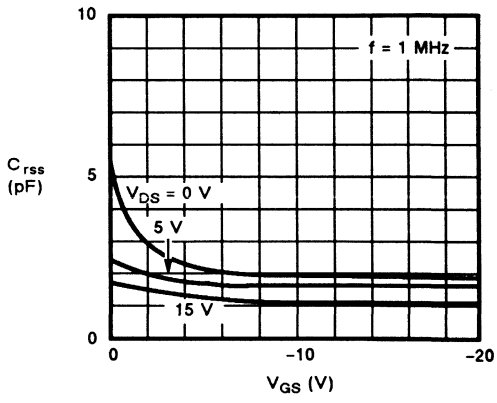
Circuit Voltage Gain vs. Drain Current



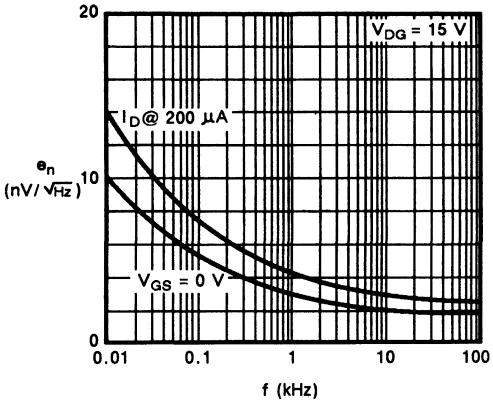
Common-Source Input Capacitance vs. Gate-Source Voltage



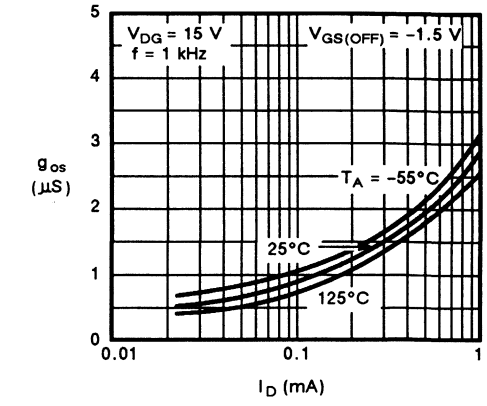
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



4

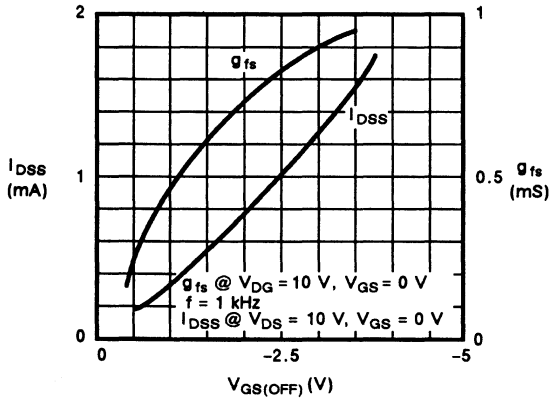
NNT
N-Channel JFET Dual Monolithic

Siliconix incorporated

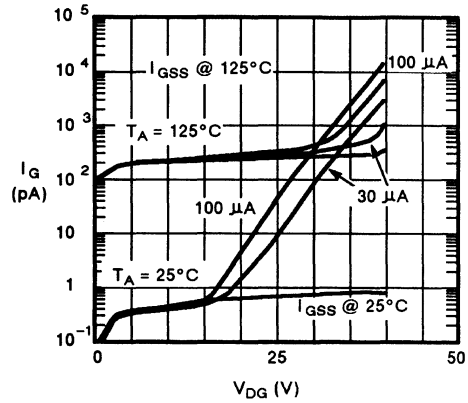
TYPE	PACKAGE	DEVICE
Dual	TO-78	• U421, U423
Dual	Chip	• Available as NNT1CHP

TYPICAL CHARACTERISTICS

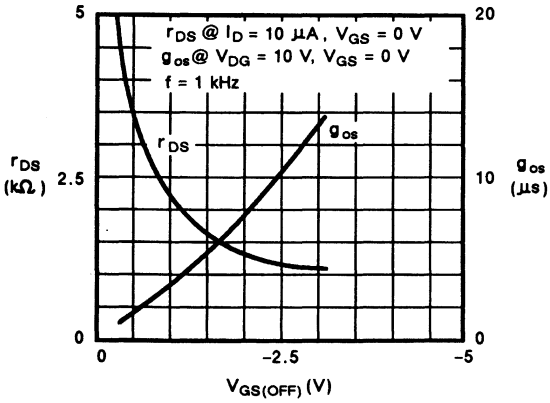
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



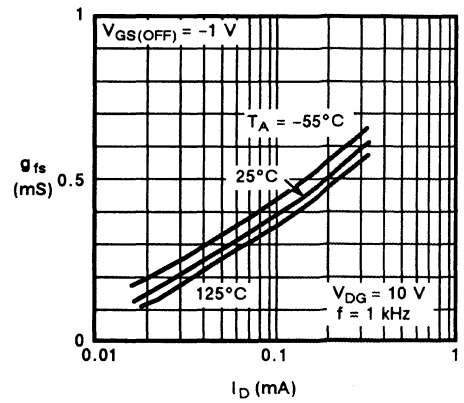
Operating Gate Current



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



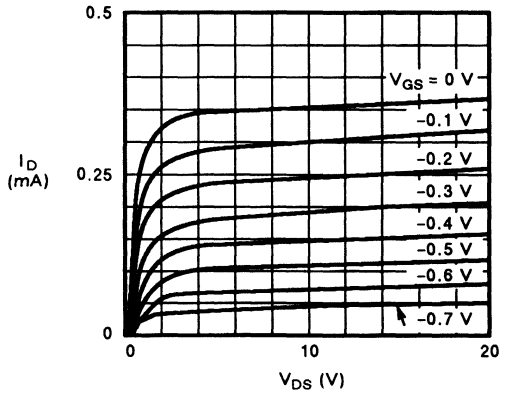
Common-Source Forward Transconductance vs. Drain Current



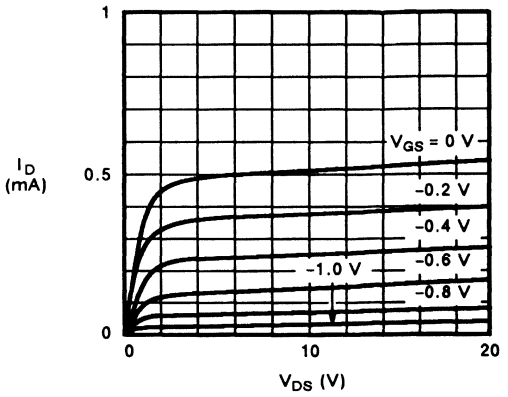
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

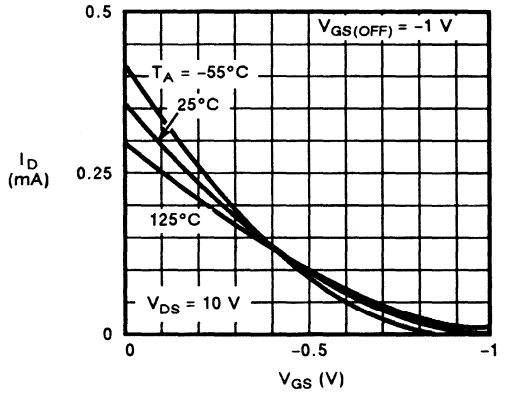
Output Characteristics ($V_{GS(OFF)}$ = -1 V)



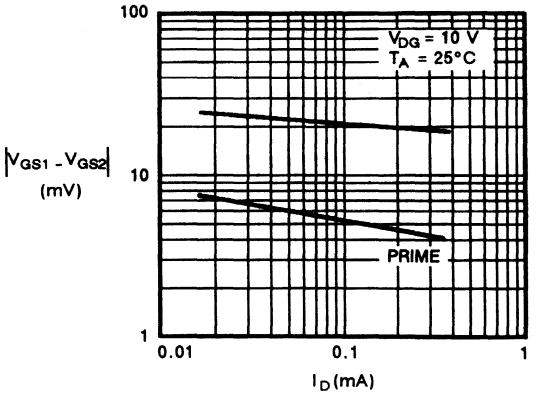
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



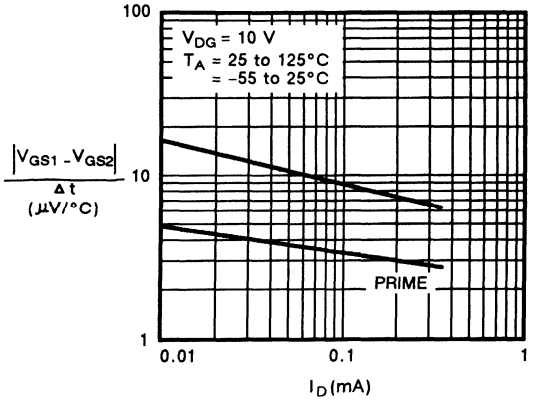
Transfer Characteristics



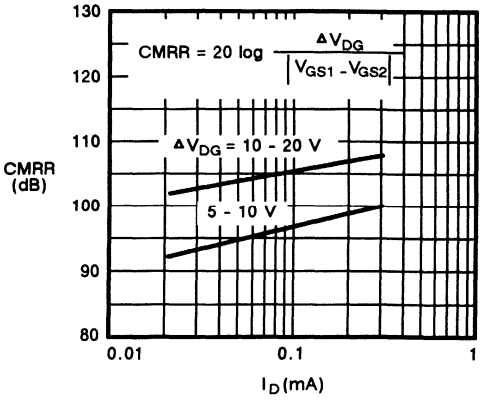
Gate-Source Differential Voltage vs. Drain Current



Voltage Differential with Temperature vs. Drain Current



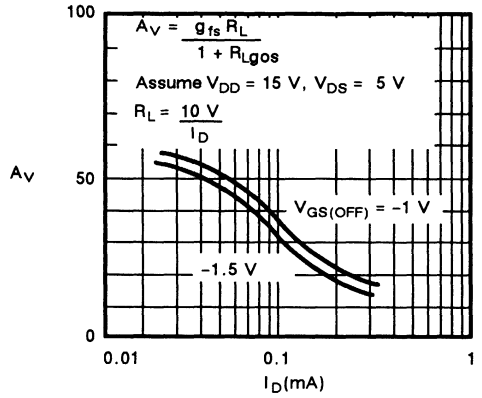
Common Mode Rejection Ratio vs. Drain Current



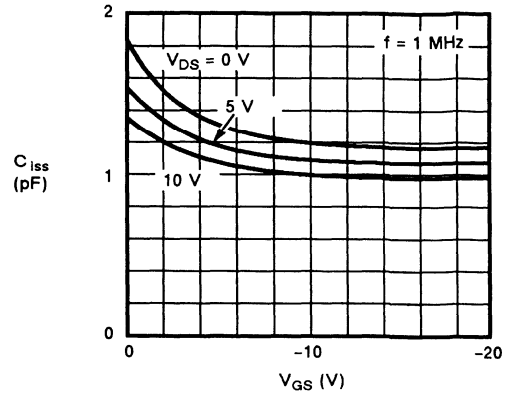
4

TYPICAL CHARACTERISTICS (Cont'd)

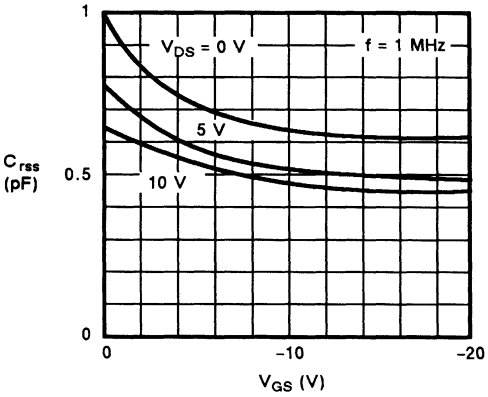
Circuit Voltage Gain vs. Drain Current



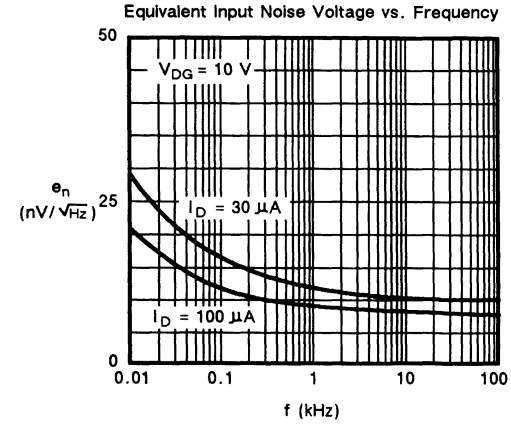
Common-Source Input Capacitance vs. Gate-Source Voltage



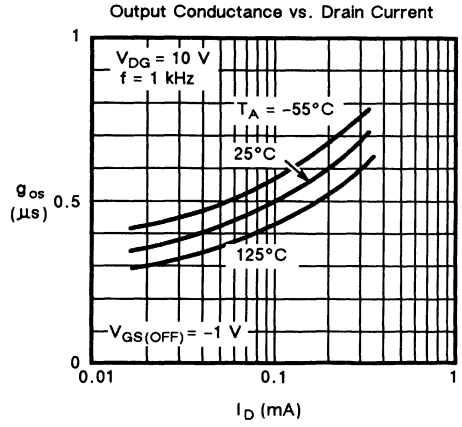
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current

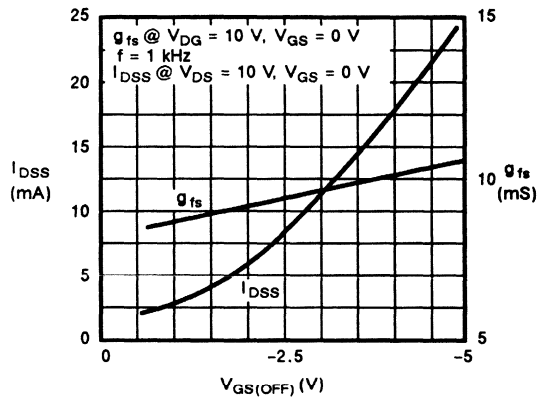


NNZ
N-Channel JFET Pair

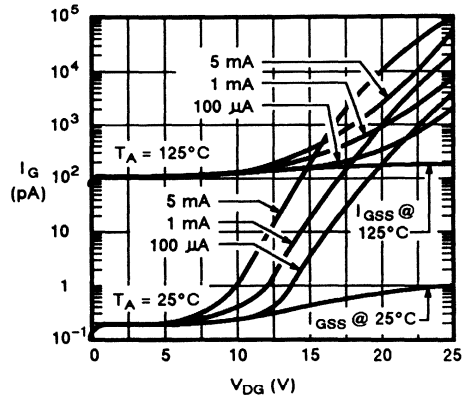
TYPE	PACKAGE	DEVICE
Dual	SOIC-8	• SST440, SST441
Dual	TO-71	• U440, U441
Dual	TO-78	• 2N5911, 2N5912
Dual	Chip	• Available as NNZ1CHP

TYPICAL CHARACTERISTICS

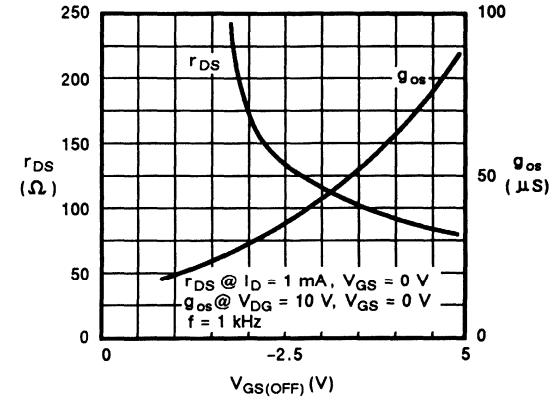
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



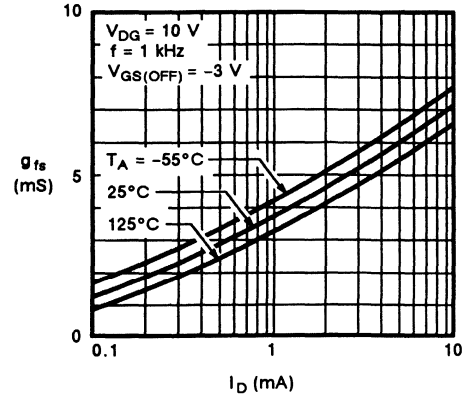
Operating Gate Current



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



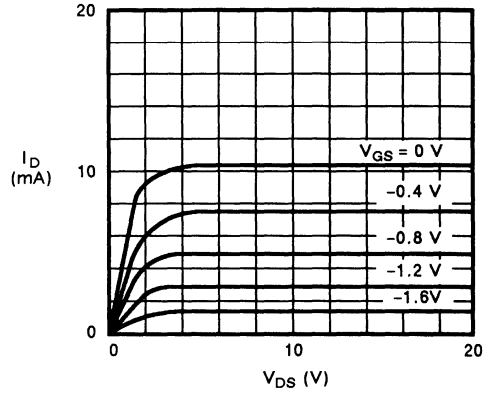
Common-Source Forward Transconductance vs. Drain Current



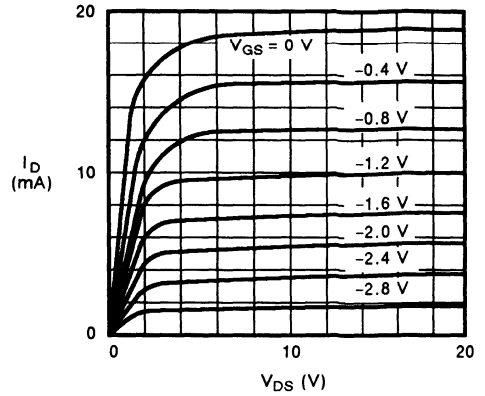
4

TYPICAL CHARACTERISTICS (Cont'd)

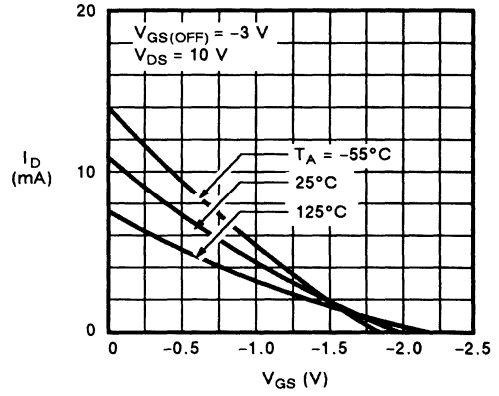
Output Characteristics ($V_{GS(OFF)} = -3$ V)



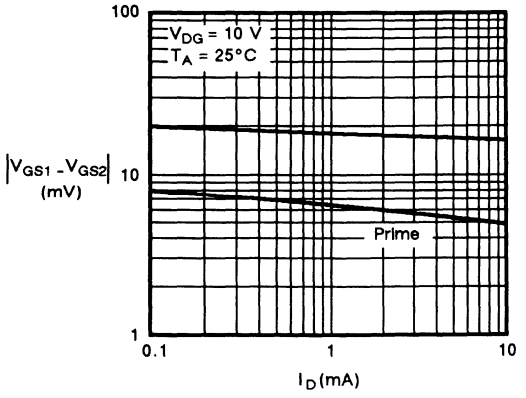
Output Characteristics ($V_{GS(OFF)} = -4$ V)



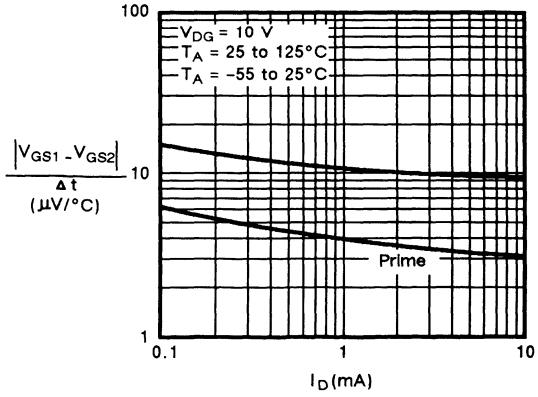
Transfer Characteristics



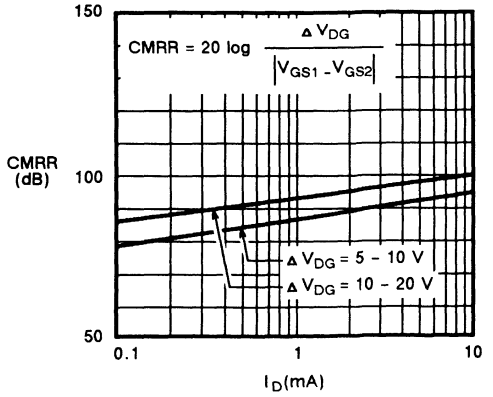
Gate-Source Differential Voltage vs. Drain Current



Voltage Differential with Temperature vs. Drain Current

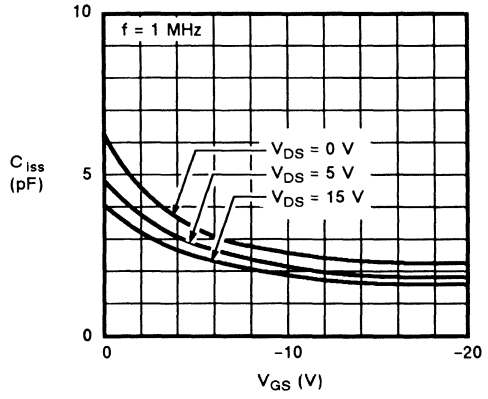


Common Mode Rejection Ratio vs. Drain Current

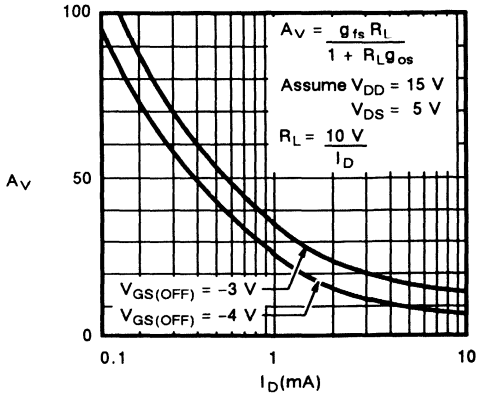


TYPICAL CHARACTERISTICS (Cont'd)

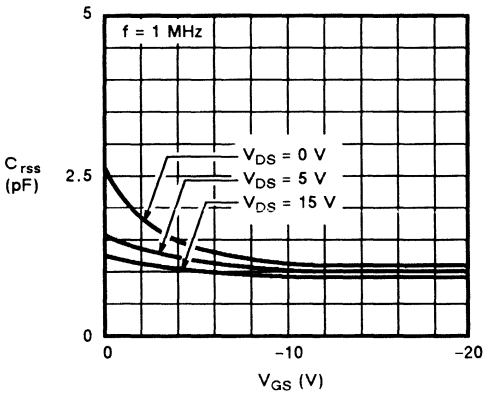
Common-Source Input Capacitance vs. Gate-Source Voltage



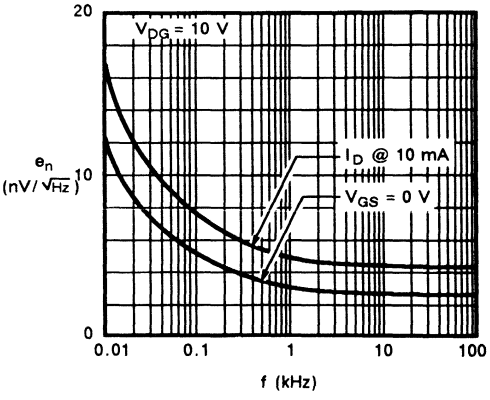
Circuit Voltage Gain vs. Drain Current



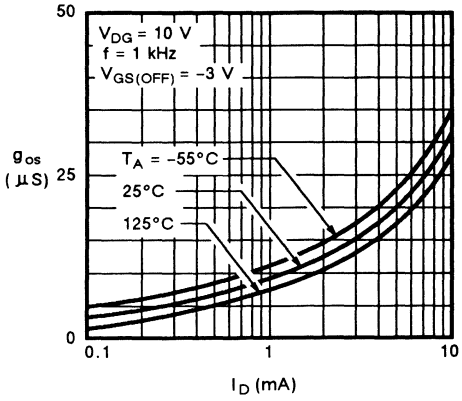
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



4

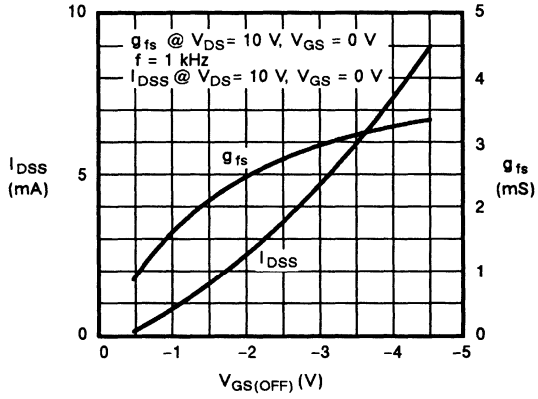
NPA
N-Channel JFETs

Siliconix incorporated

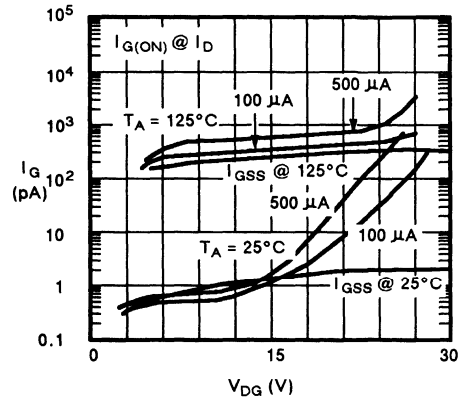
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• J201, J202
Single	SOT-23	• SST201, SST202
Single	TO-18	• 2N4338, 2N4339, 2N4340, 2N4341, VCR4N
Single	Chip	• Available as NPA1CHP, NPA2CHP, NPA3CHP, NPA4CHP

TYPICAL CHARACTERISTICS

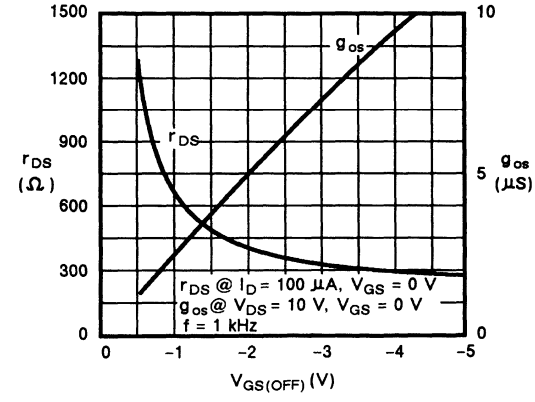
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



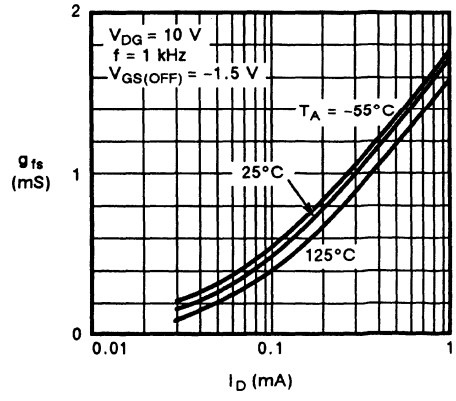
Operating Gate Current



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage

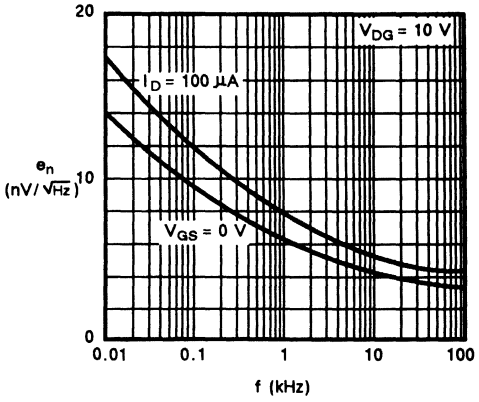


Common-Source Forward Transconductance vs. Drain Current

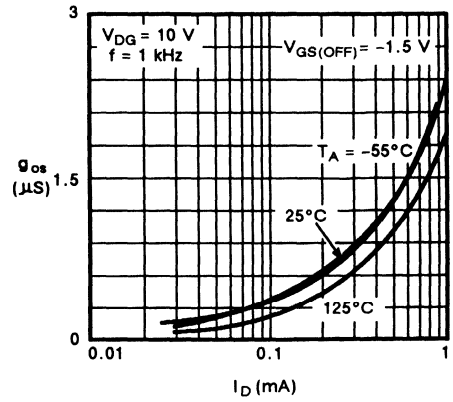


TYPICAL CHARACTERISTICS (Cont'd)

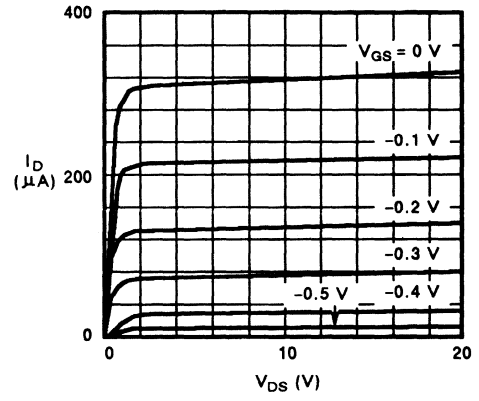
Equivalent Input Noise Voltage vs. Frequency



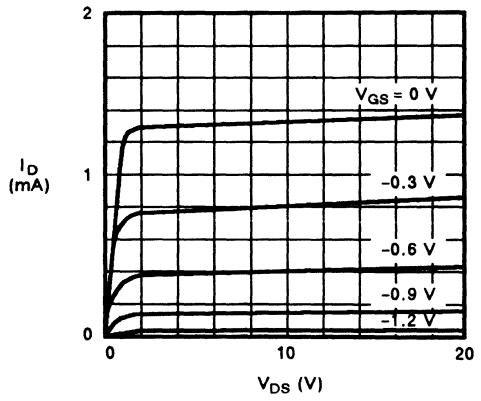
Output Conductance vs. Drain Current



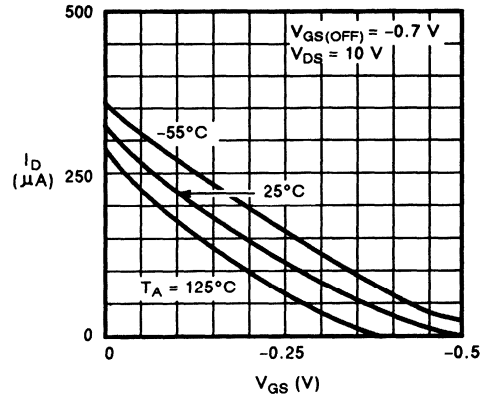
Output Characteristics ($V_{GS(OFF)}$ = -0.7 V)



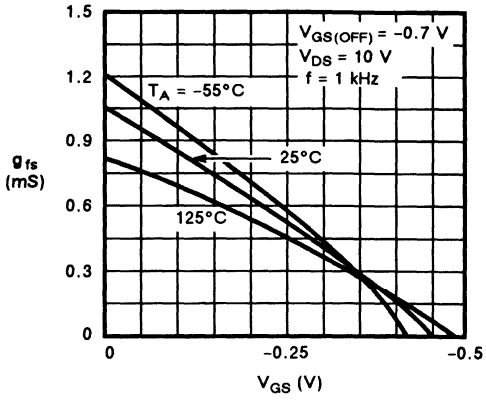
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



Transfer Characteristics



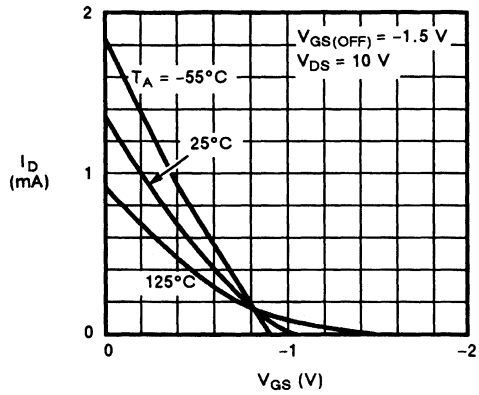
Transconductance vs. Gate-Source Voltage



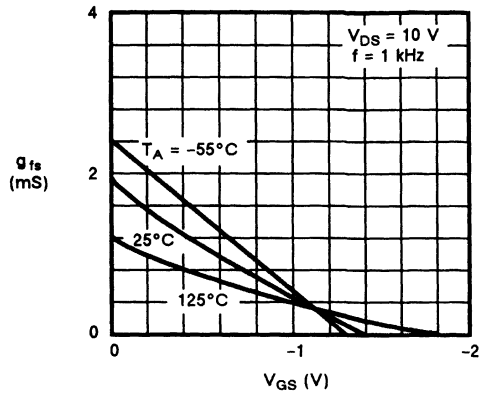
4

TYPICAL CHARACTERISTICS

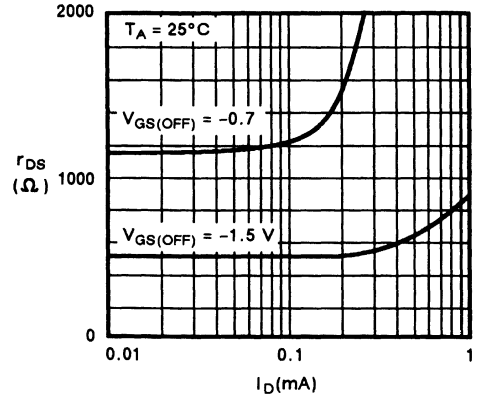
Transfer Characteristics



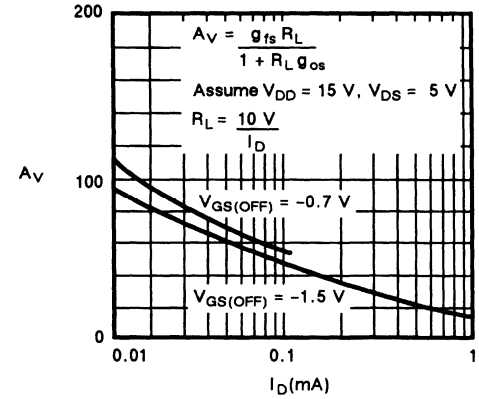
Transconductance vs. Gate-Source Voltage



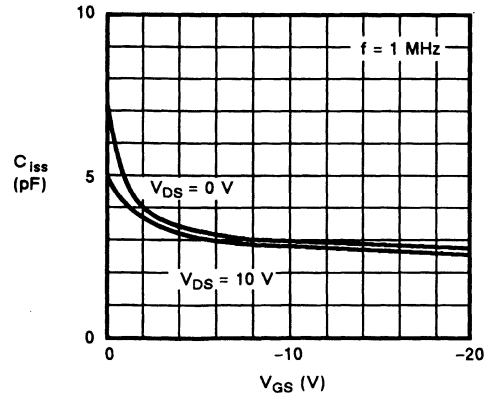
On-Resistance vs. Drain Current



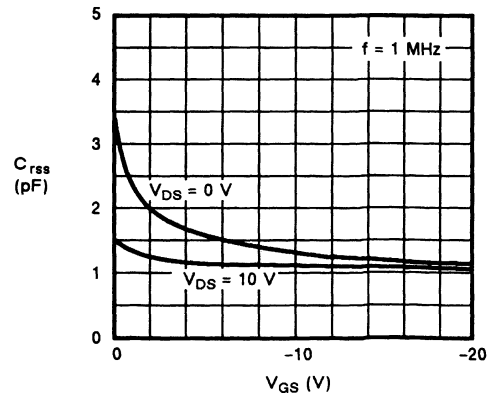
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



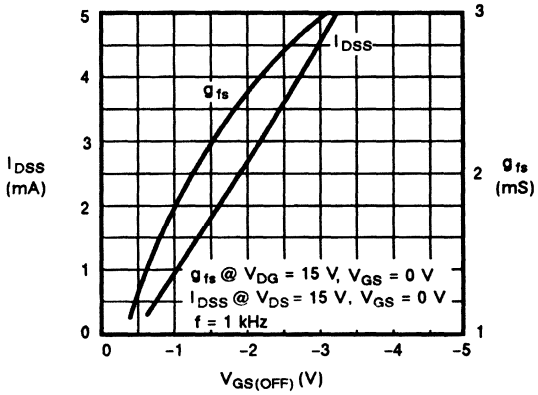
Siliconix incorporated

NQP
N-Channel JFET Pairs

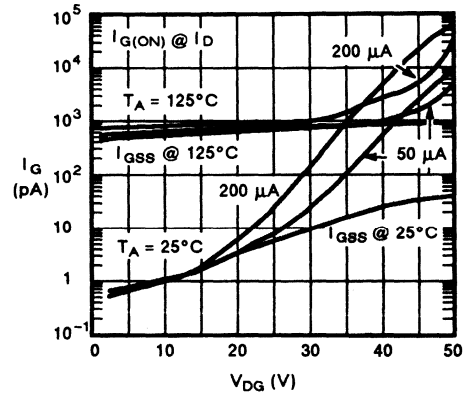
TYPE	PACKAGE	DEVICE
Dual	TO-71	• 2N5196, 2N5197, 2N5198, 2N5199
Dual	Chip	• Available as NQP1CHP

TYPICAL CHARACTERISTICS

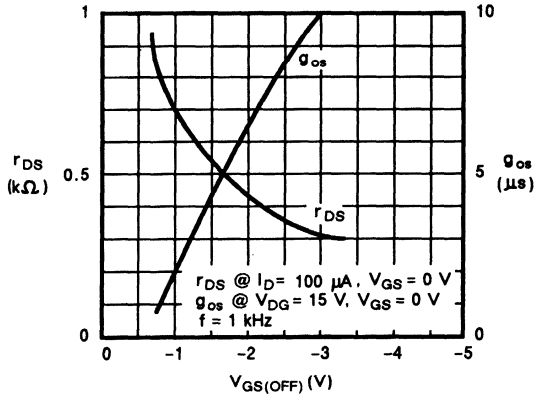
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



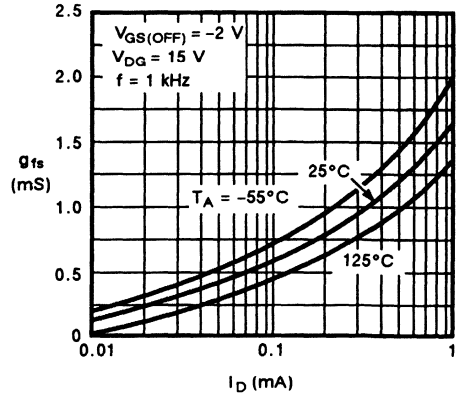
Operating Gate Current



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



Common-Source Forward Transconductance vs. Drain Current



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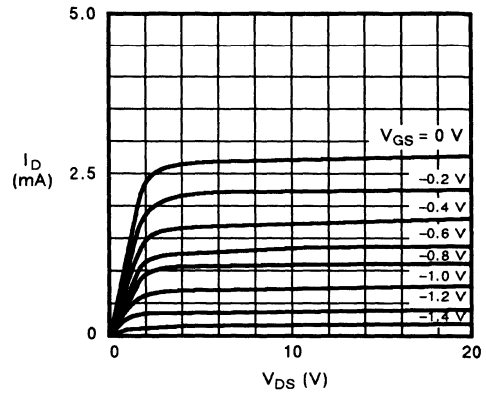
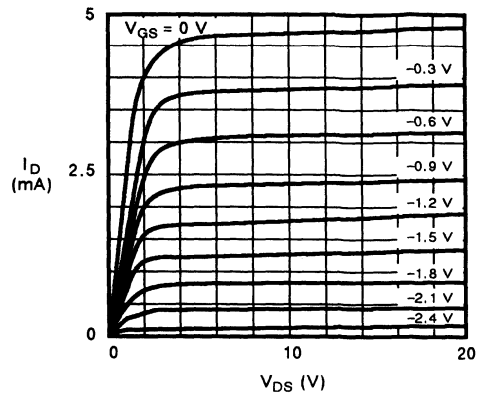
TYPICAL CHARACTERISTICS (Cont'd)

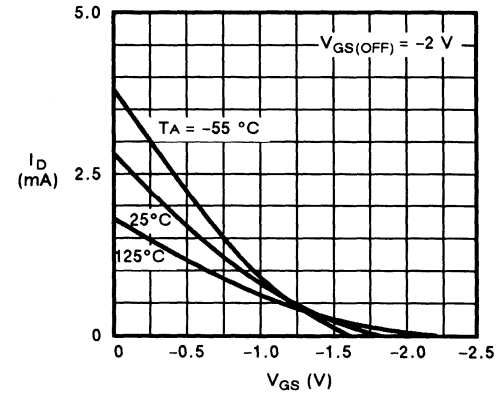
Output Characteristics ($V_{GS(OFF)} = -2$ V)



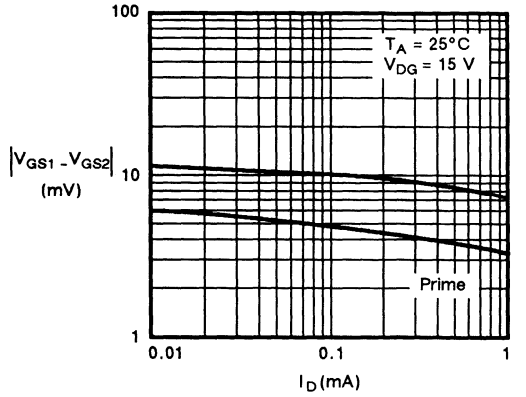
Output Characteristics ($V_{GS(OFF)} = -3$ V)



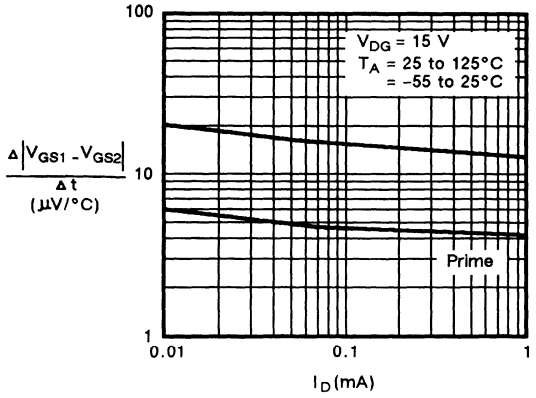
Transfer Characteristics



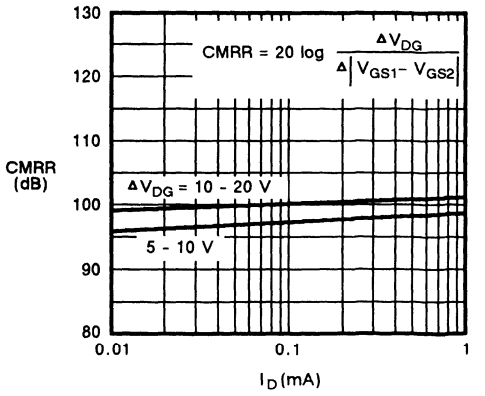
Gate-Source Differential Voltage vs. Drain Current



Voltage Differential with Temperature vs. Drain Current

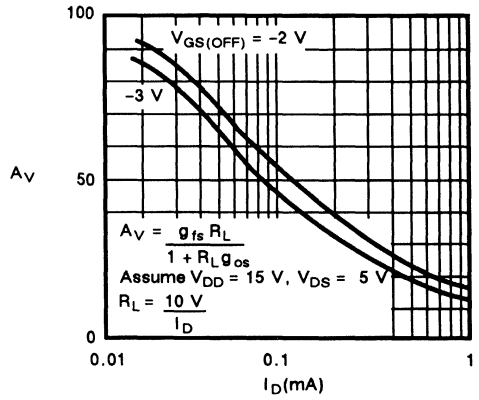


Common Mode Rejection Ratio vs. Drain Current

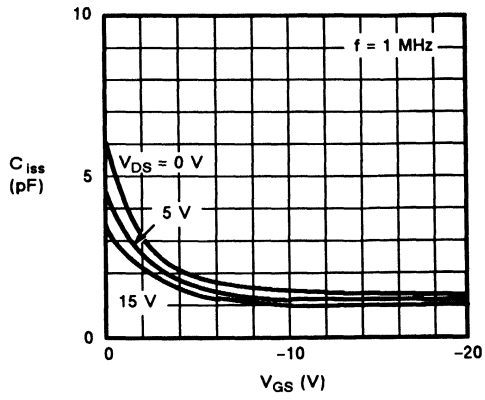


TYPICAL CHARACTERISTICS (Cont'd)

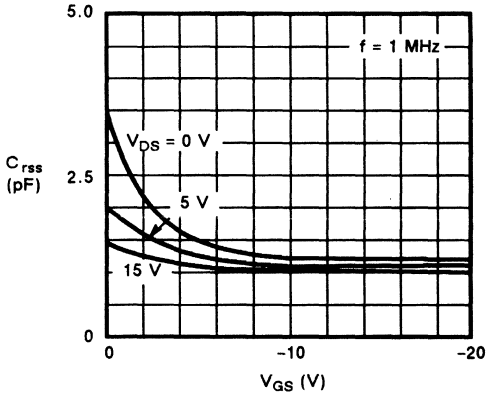
Circuit Voltage Gain vs. Drain Current



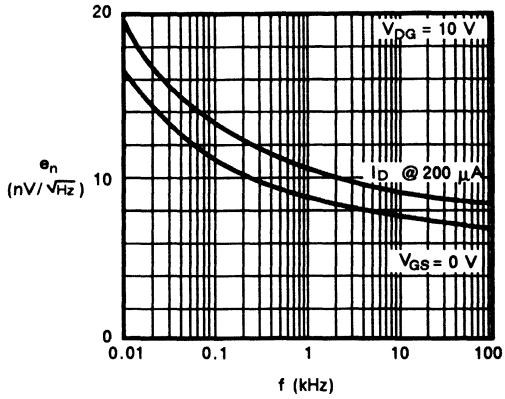
Common-Source Input Capacitance vs. Gate-Source Voltage



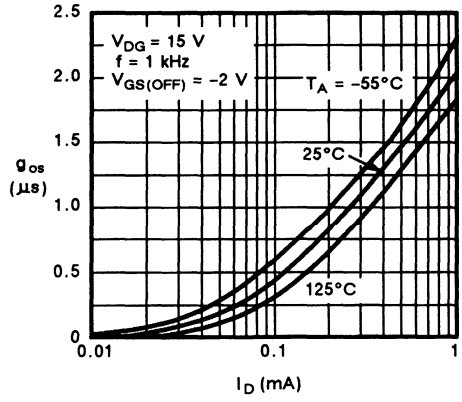
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



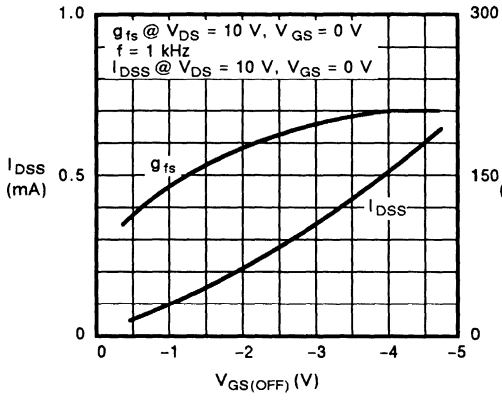
NT
N-Channel JFETs

Siliconix incorporated

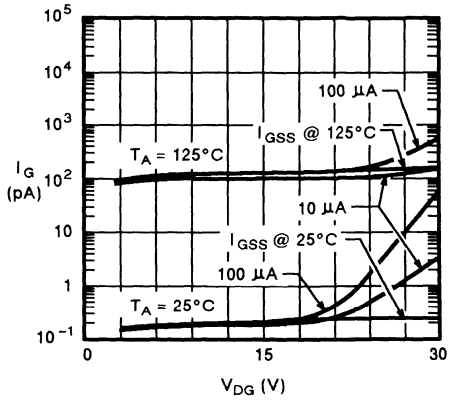
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• PN4117A, PN4118A, PN4119A
Single	TO-72 (TO-206AF)	• 2N4117A, 2N4118A, 2N4119A
Chip	Chip	• Available as NT1CHP, NT2CHP, NT3CHP

TYPICAL CHARACTERISTICS

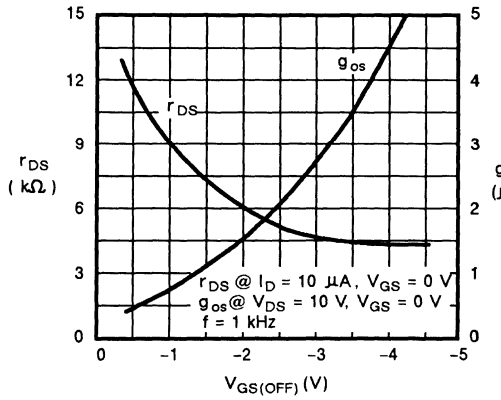
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



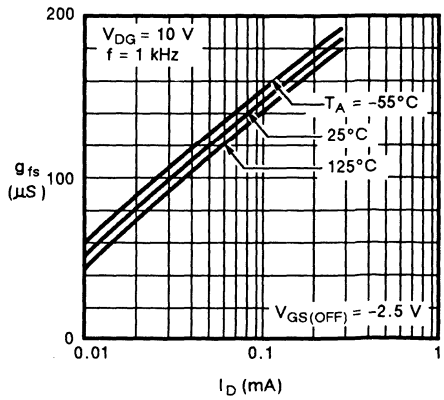
Operating Gate Current



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



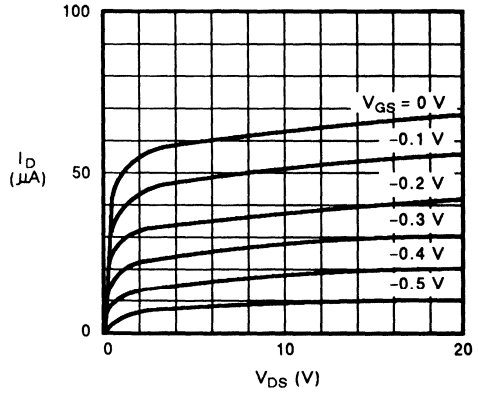
Common-Source Forward Transconductance vs. Drain Current



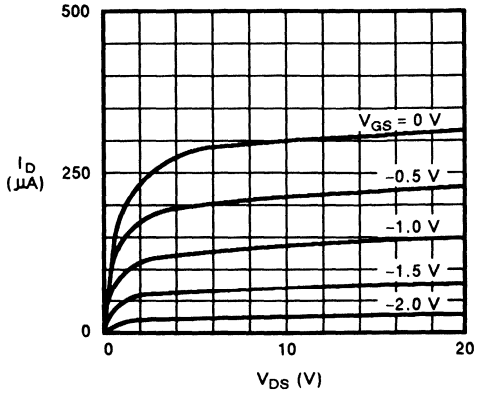
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

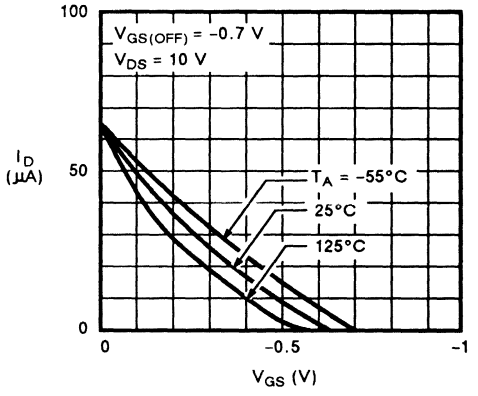
Output Characteristics ($V_{GS(OFF)}$ = -0.7 V)



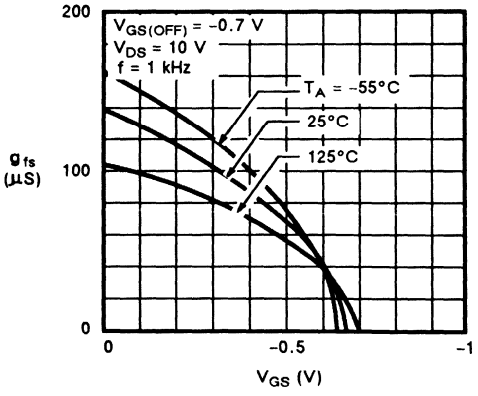
Output Characteristics ($V_{GS(OFF)}$ = -2.5 V)



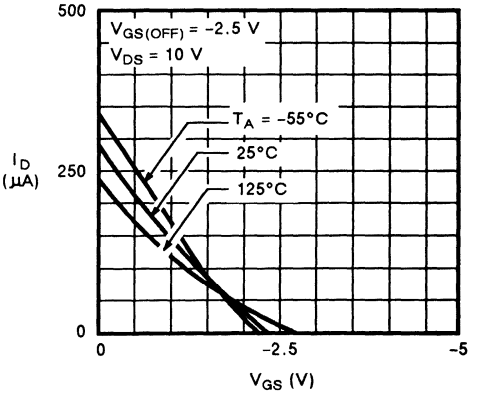
Transfer Characteristics



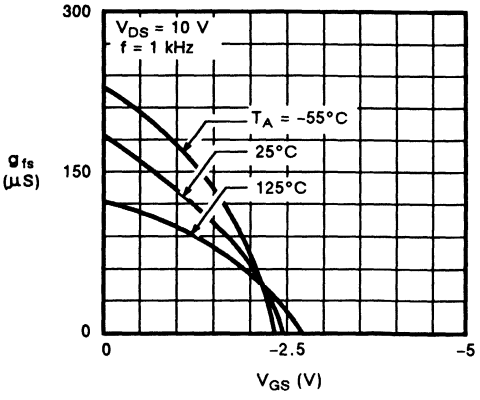
Transconductance vs. Gate-Source Voltage



Transfer Characteristics



Transconductance vs. Gate-Source Voltage



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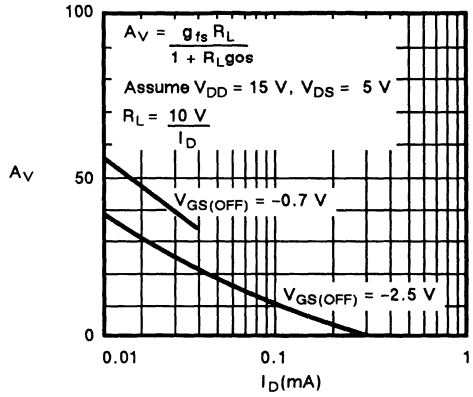
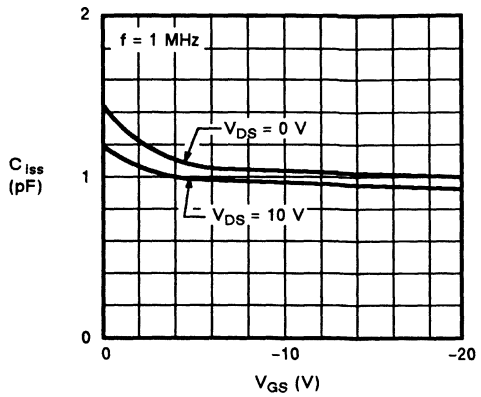
TYPICAL CHARACTERISTICS (Cont'd)

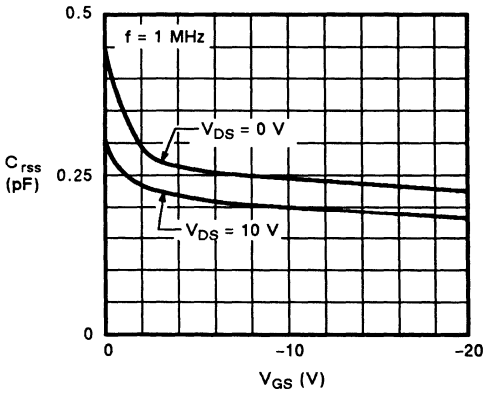
Circuit Voltage Gain vs. Drain Current



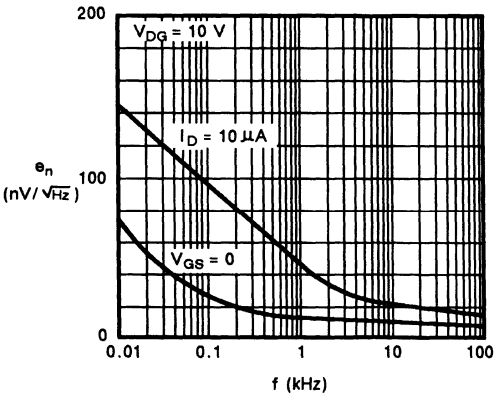
Common-Source Input Capacitance vs. Gate-Source Voltage



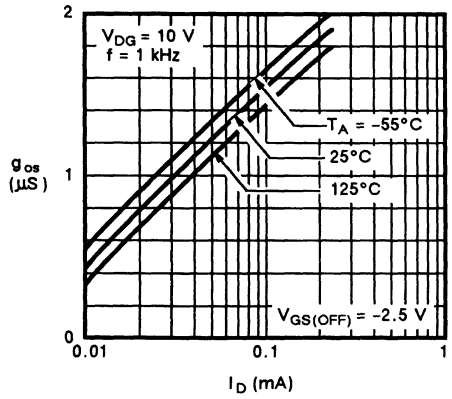
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Equivalent Input Noise Voltage vs. Frequency



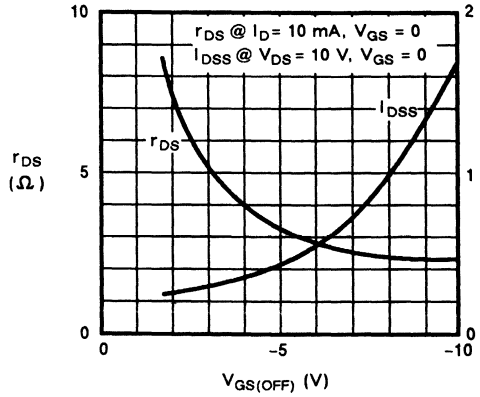
Output Conductance vs. Drain Current



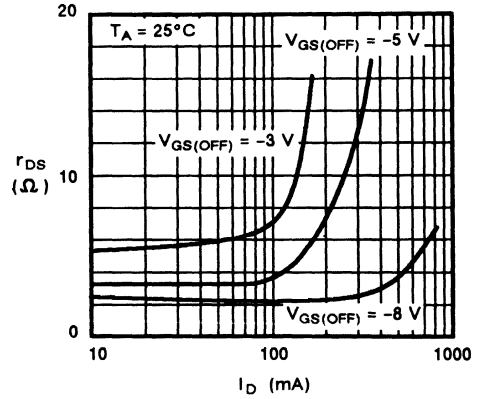
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• J105, J106, J107
Single	TO-52 (TO-206AC)	• U290, U291
Single	Chip	• Available as NVA1CHP, NVA2CHP, NVA3CHP

TYPICAL CHARACTERISTICS

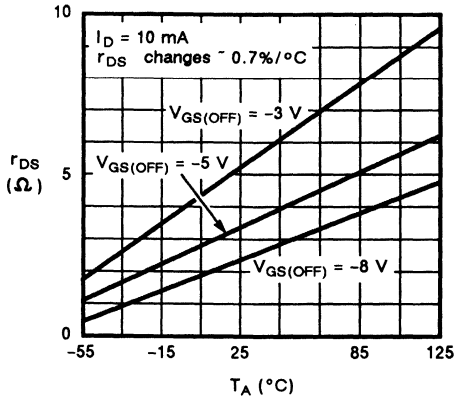
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



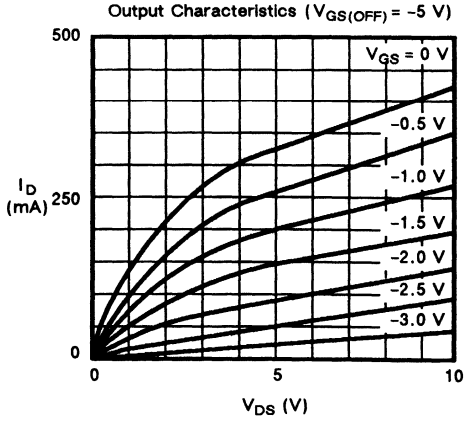
On-Resistance vs. Drain Current



On-Resistance vs. Temperature



Output Characteristics ($V_{GS(OFF)}$ = -5 V)



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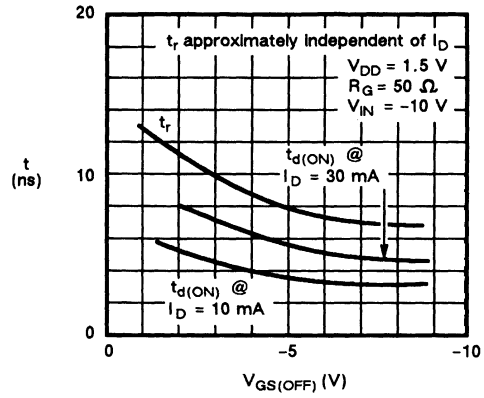
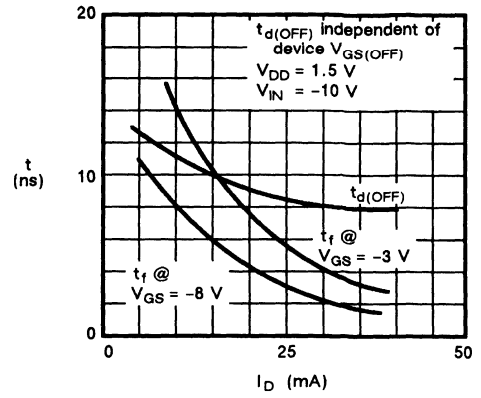
TYPICAL CHARACTERISTICS (Cont'd)

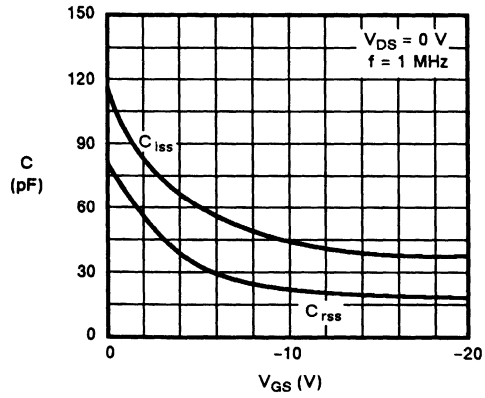
Turn-On Switching



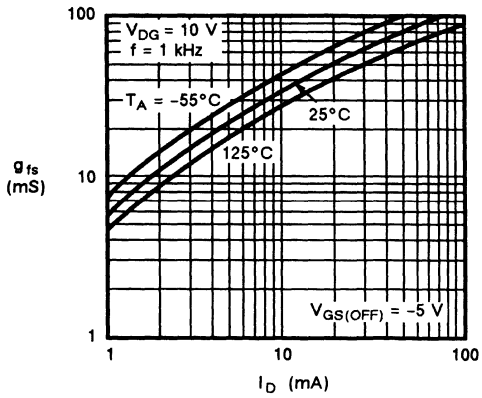
Turn-Off Switching



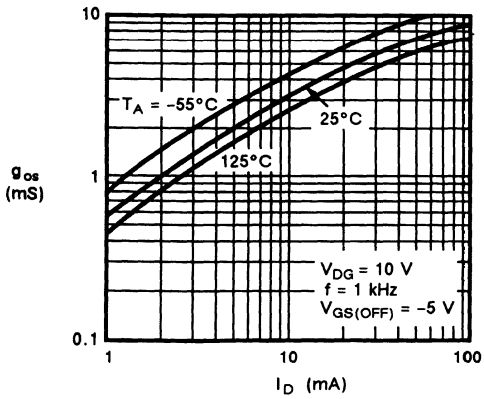
Capacitance vs. Gate-Source Voltage



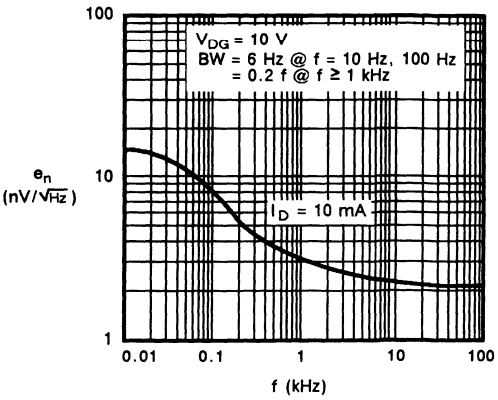
Transconductance vs. Drain Current



Output Conductance vs. Drain Current

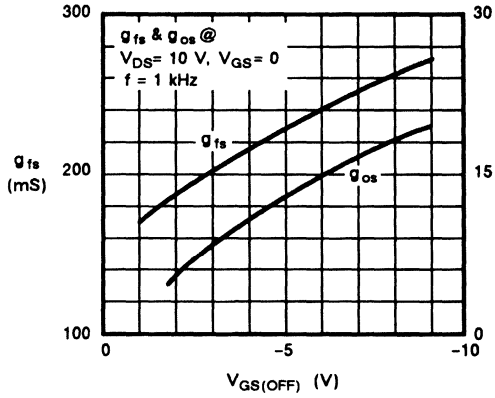


Noise Voltage vs. Frequency

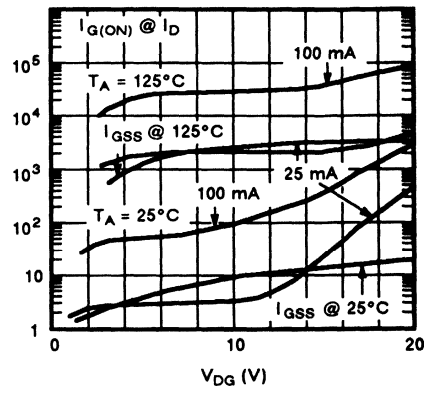


TYPICAL CHARACTERISTICS (Cont'd)

Forward Transconductance & Output Conductance vs. Gate-Source Cutoff Voltage



Operating Gate Current



4

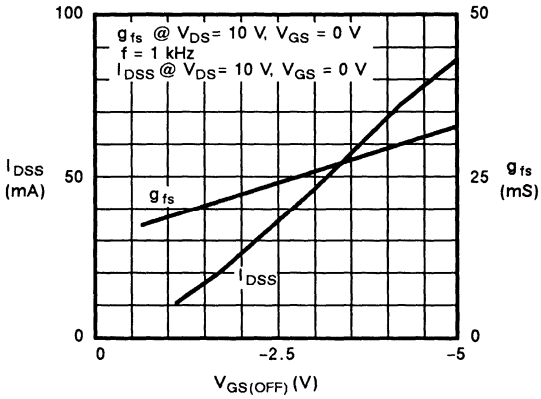
NZB
N-Channel JFETs

Siliconix incorporated

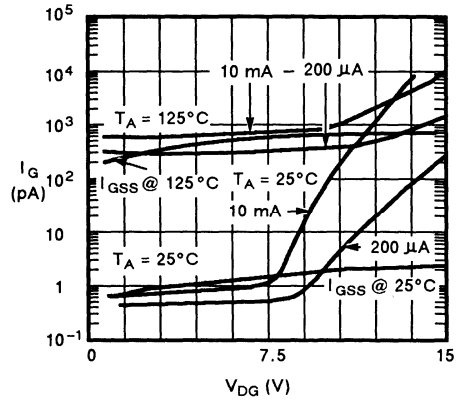
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• J308, J309, J310
Single	SOT-23	• SST308, SST309, SST310
Single	TO-52 (TO-206AC)	• U309, U310
Dual	TO-78	• U430, U431
Single	Chip	• Available as NZB1CHP, NZB2CHP, NZB3CHP
Dual	Chip	• Available as NZBD1CHP, NZBD2CHP

TYPICAL CHARACTERISTICS

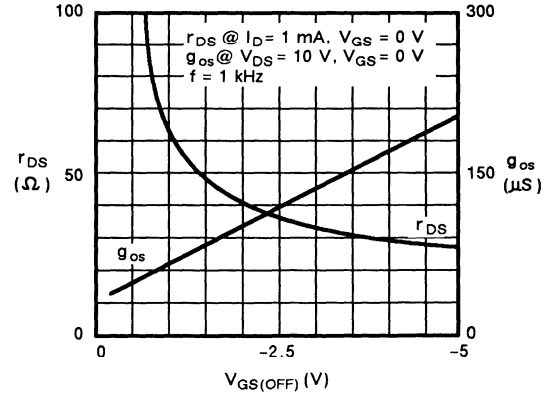
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



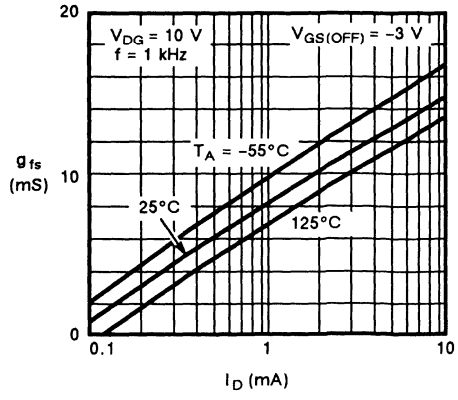
Operating Gate Current



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



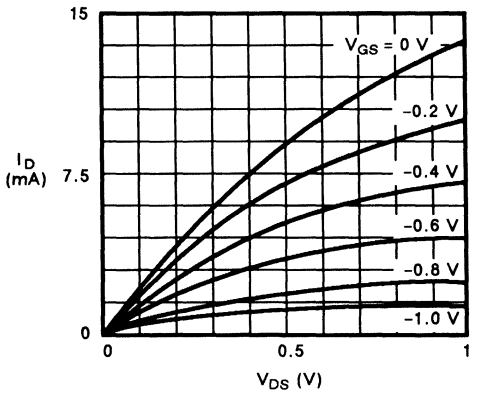
Common-Source Forward Transconductance vs. Drain Current



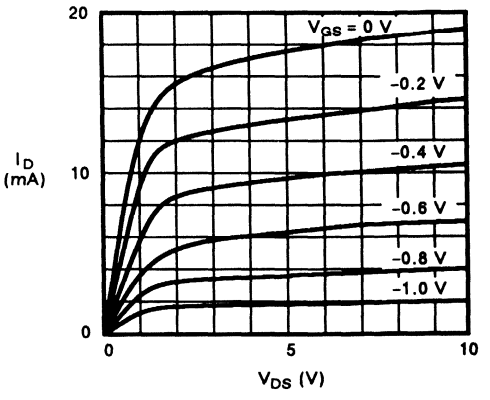
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

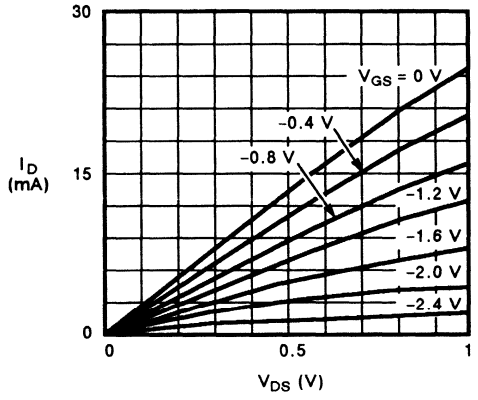
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



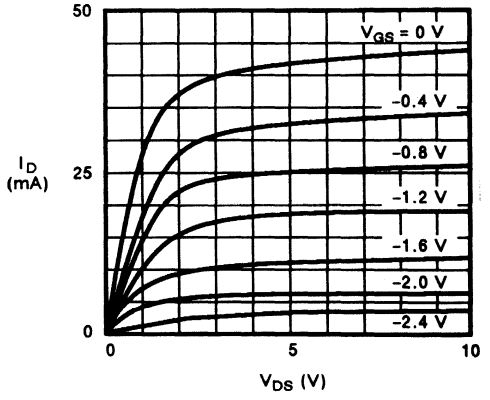
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



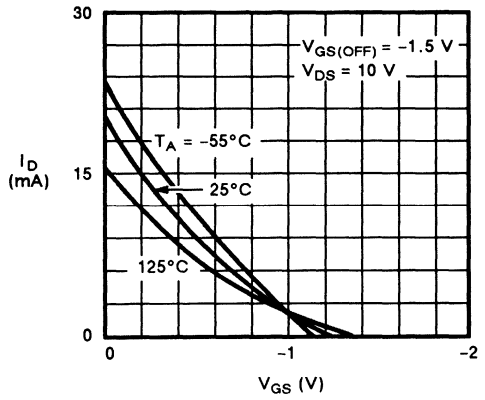
Output Characteristics ($V_{GS(OFF)}$ = -3 V)



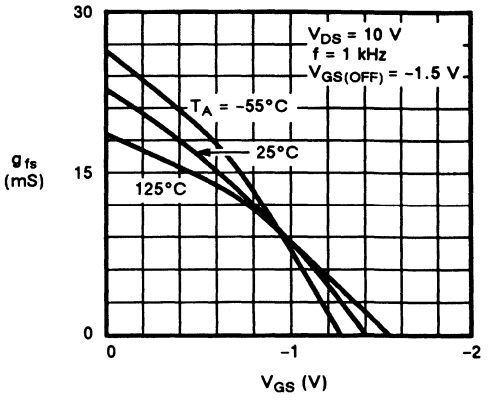
Output Characteristics ($V_{GS(OFF)}$ = -3 V)



Transfer Characteristics



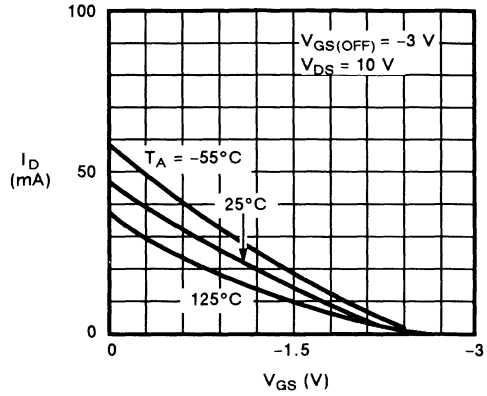
Transconductance vs. Gate-Source Voltage



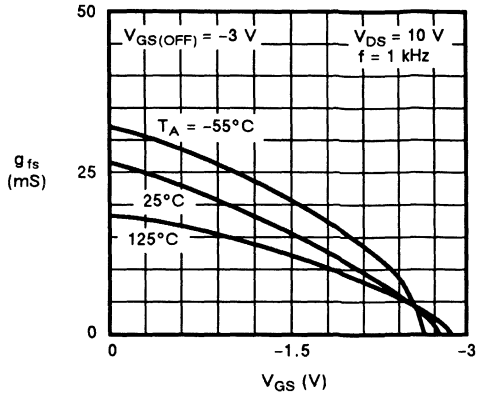
4

TYPICAL CHARACTERISTICS (Cont'd)

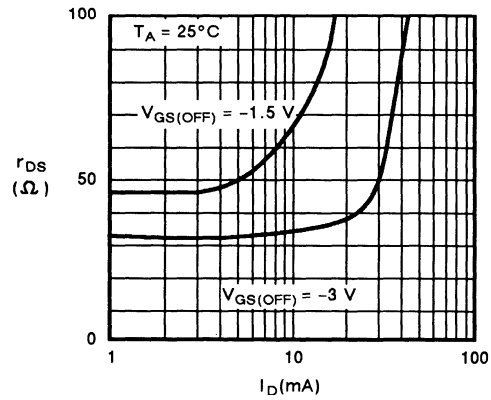
Transfer Characteristics



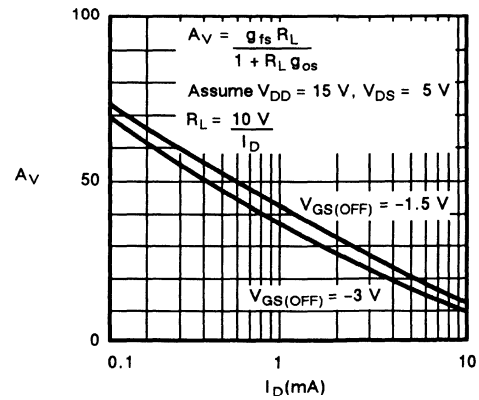
Transconductance vs. Gate-Source Voltage



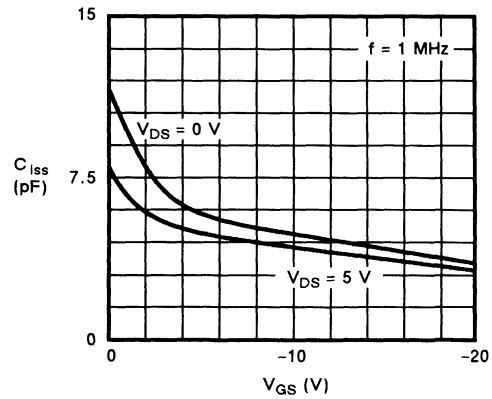
On-Resistance vs. Drain Current



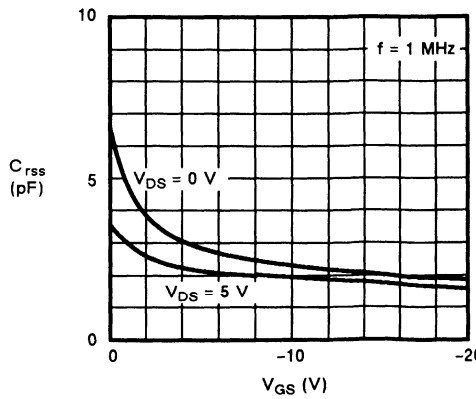
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage

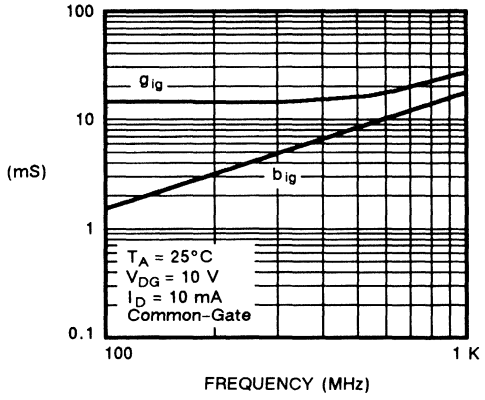


Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage

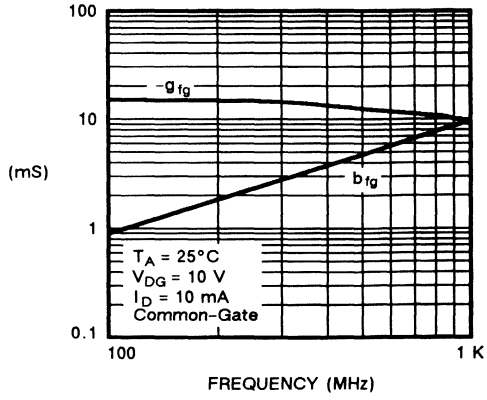


TYPICAL CHARACTERISTICS (Cont'd)

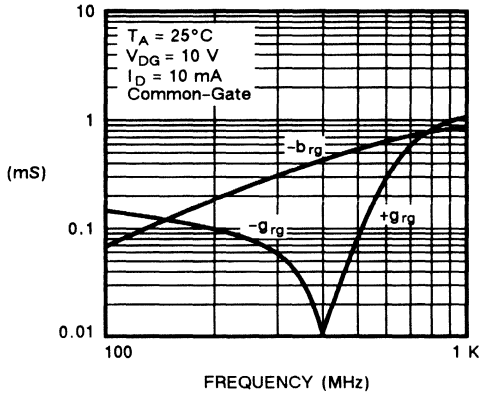
Input Admittance



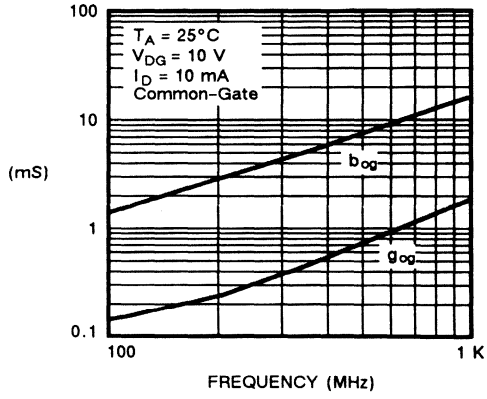
Forward Admittance



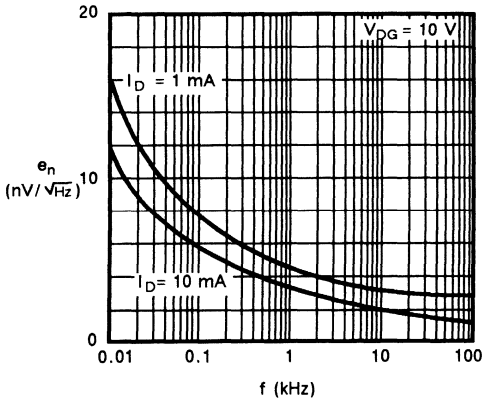
Reverse Admittance



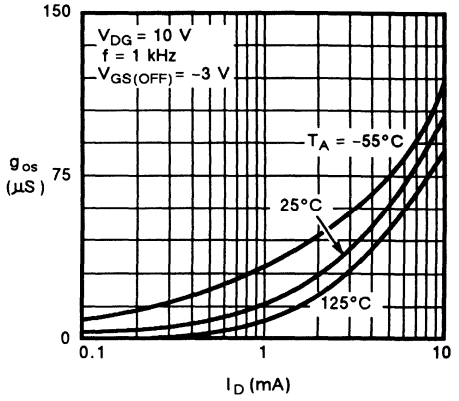
Output Admittance



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



4

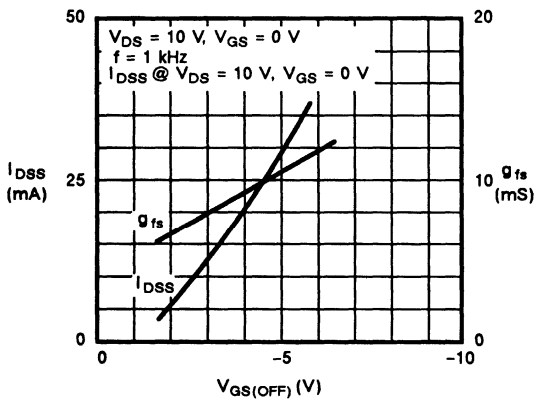
NZF
N-Channel JFETs

Siliconix incorporated

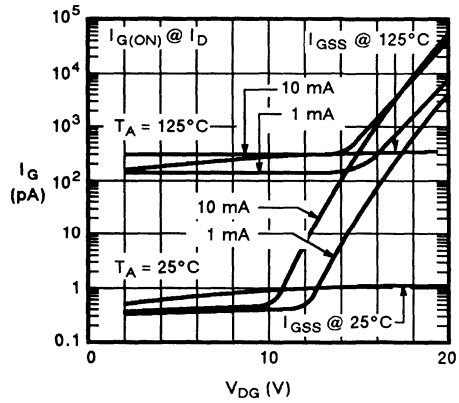
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• J210, J211, J212
Single	TO-71	• U440. U441
Dual	TO-78	• 2N5911, 2N5912
Single	Chip	• Available as NZF1CHP, NZF2CHP, NZF3CHP
Dual	Chip	• Available as NZFD1CHP

TYPICAL CHARACTERISTICS

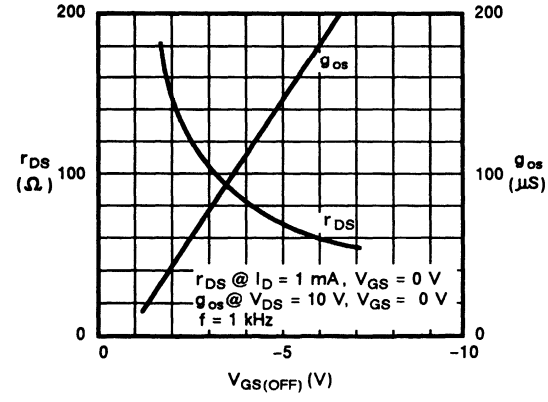
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



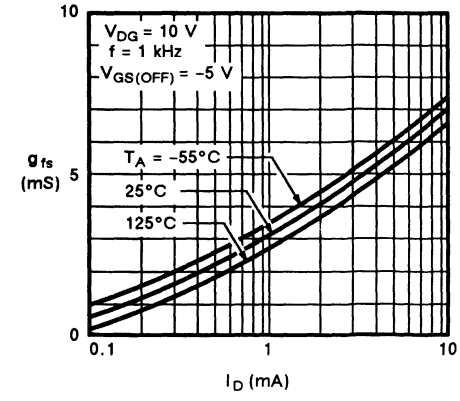
Operating Gate Current



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



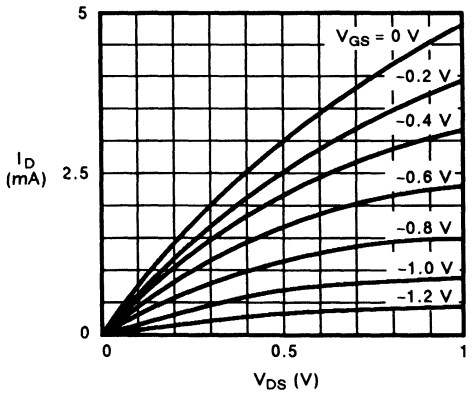
Common-Source Forward Transconductance vs. Drain Current



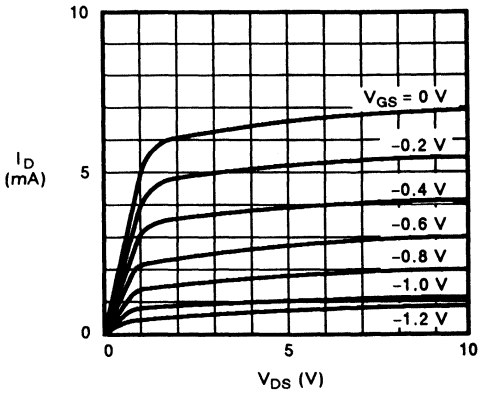
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

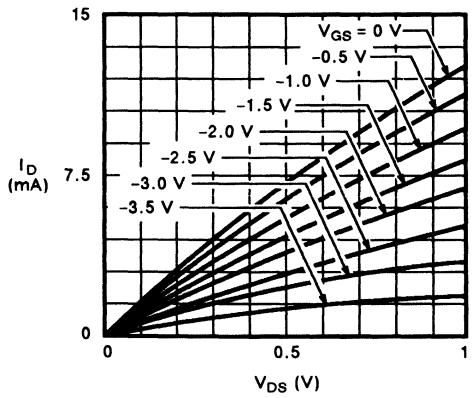
Output Characteristics ($V_{GS(OFF)}$ = -2 V)



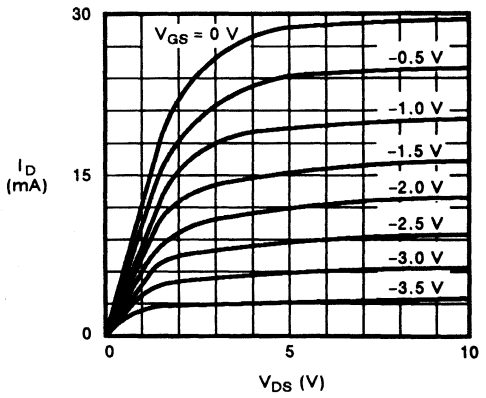
Output Characteristics ($V_{GS(OFF)}$ = -2 V)



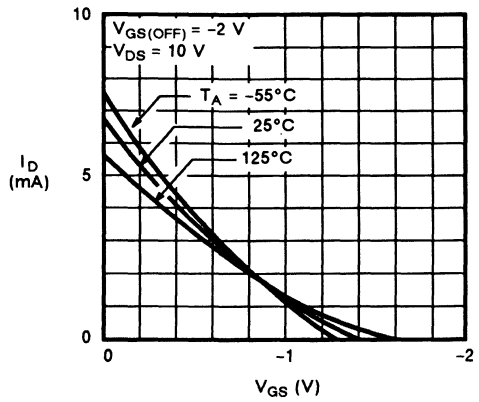
Output Characteristics ($V_{GS(OFF)}$ = -5 V)



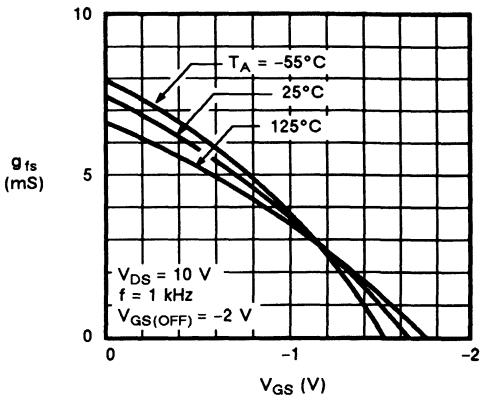
Output Characteristics ($V_{GS(OFF)}$ = -5 V)



Transfer Characteristics



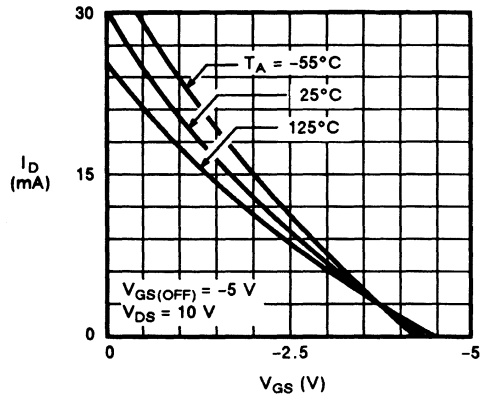
Transconductance vs. Gate-Source Voltage



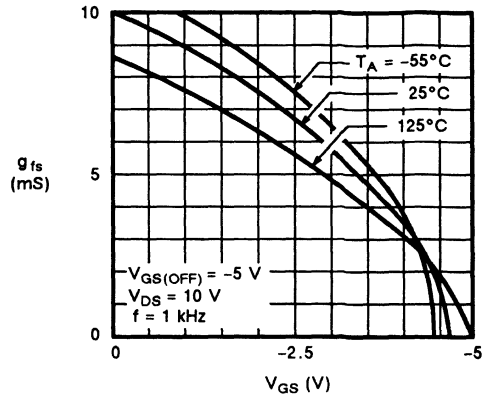
4

TYPICAL CHARACTERISTICS (Cont'd)

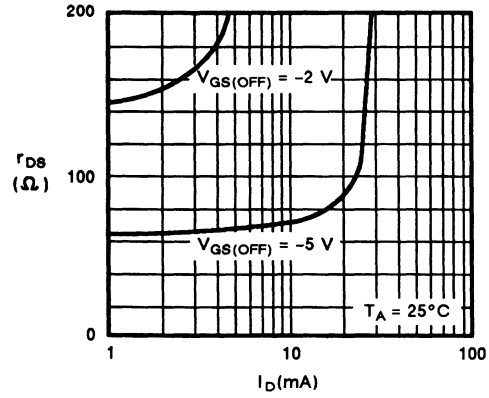
Transfer Characteristics



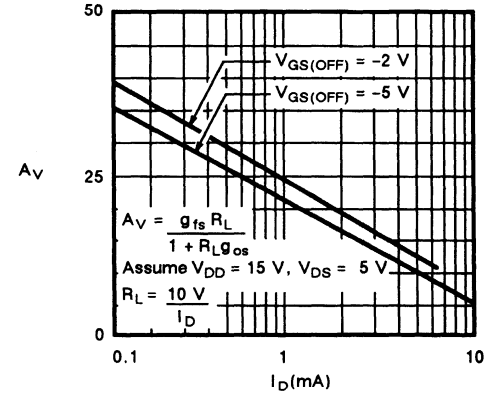
Transconductance vs. Gate-Source Voltage



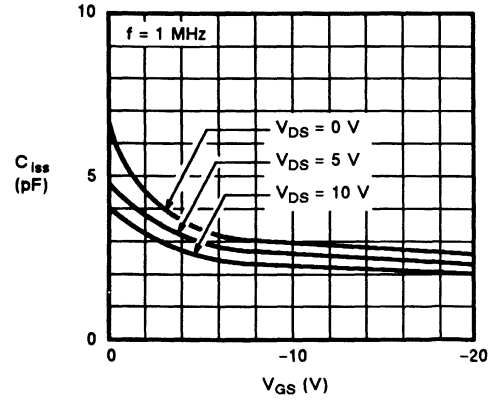
On-Resistance vs. Drain Current



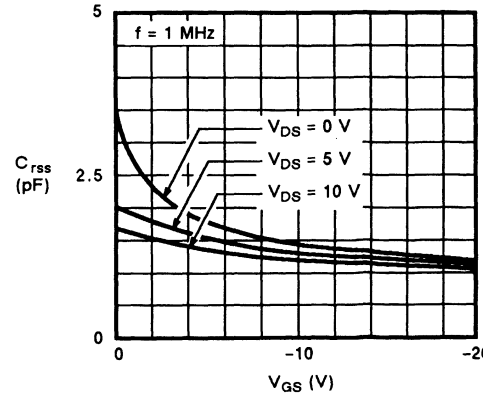
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage

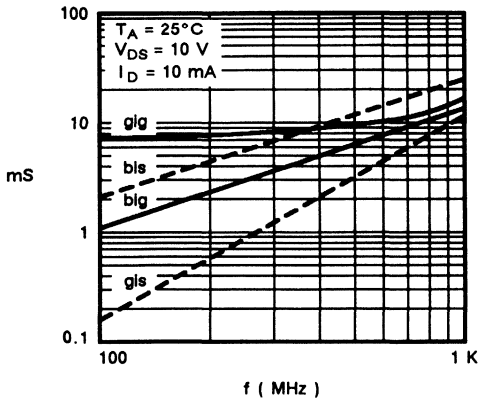


Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage

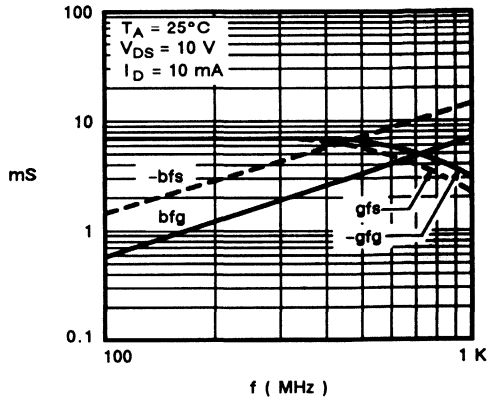


TYPICAL CHARACTERISTICS (Cont'd)

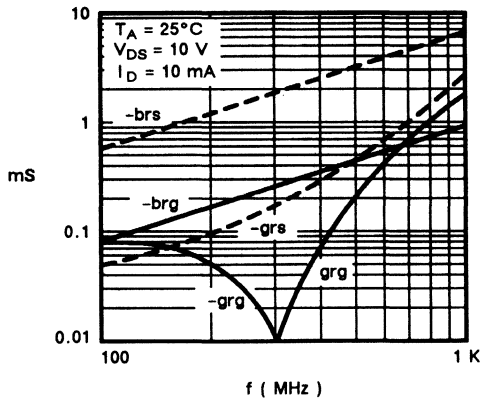
Input Admittance



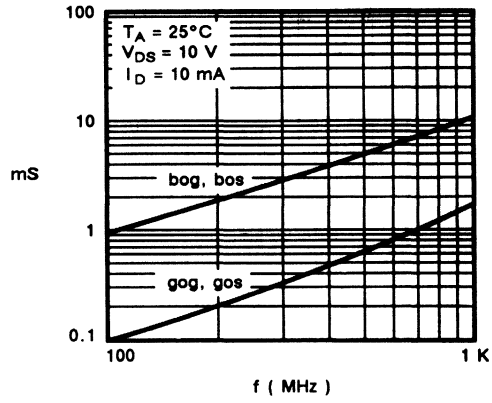
Forward Admittance



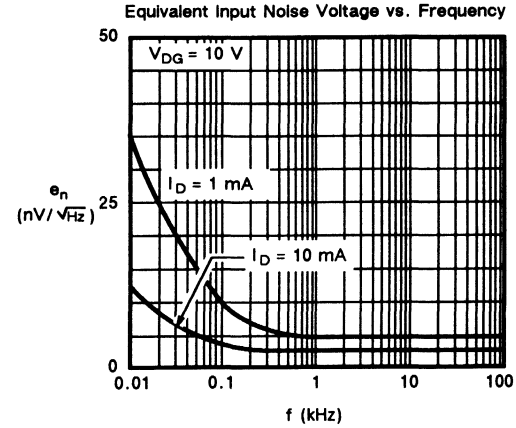
Reverse Admittance



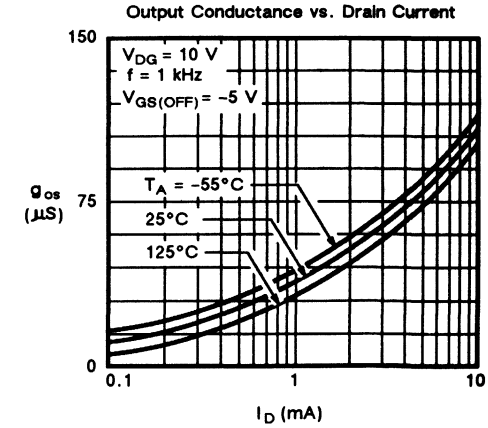
Output Admittance



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



4

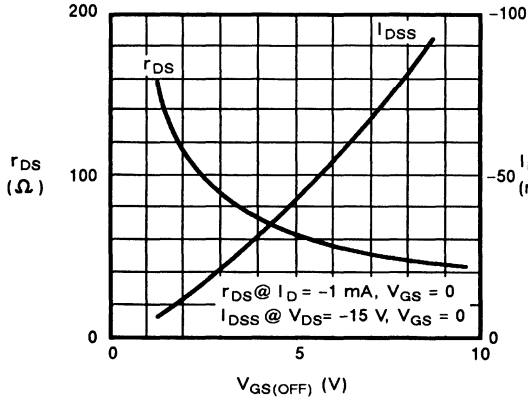
PSCIA
P-Channel JFETs

Siliconix incorporated

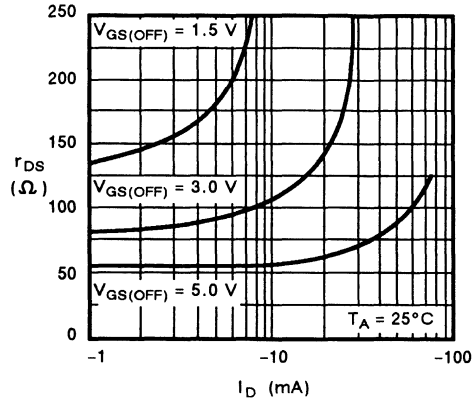
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• J174, J175, J176, J177
Single	SOT-23	• SST174, SST175, SST176, SST177
Single	TO-18	• 2N5114, 2N5115, 2N5116 (TX, TXV)
Single	Chip	• Available as PSCIA1CHP, PSCIA2CHP, PSCIA3CHP

TYPICAL CHARACTERISTICS

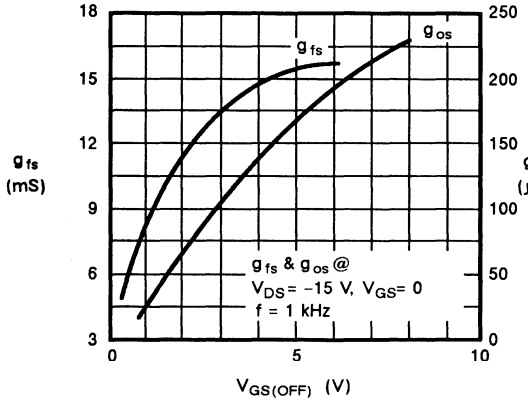
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



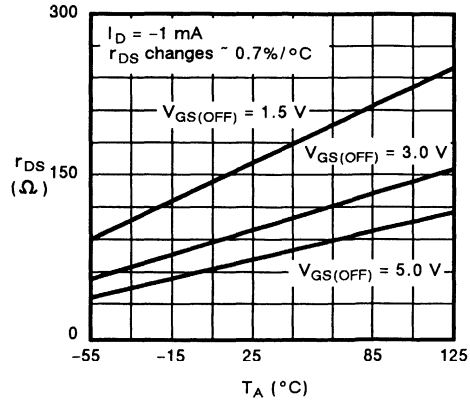
On-Resistance vs. Drain Current



Forward Transconductance & Output Conductance vs. Gate-Source Cutoff Voltage



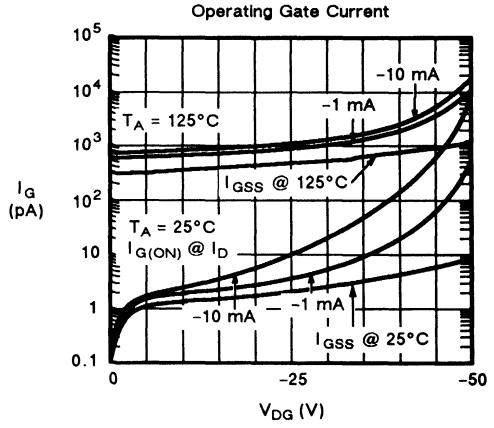
On-Resistance vs. Temperature



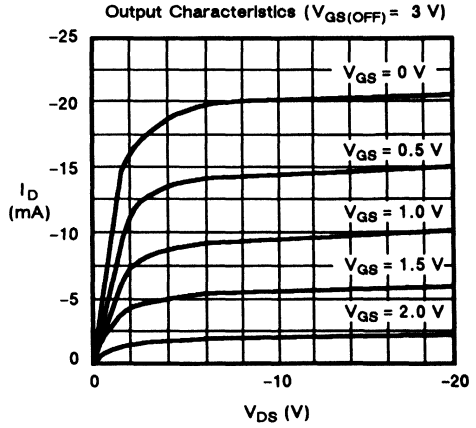
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

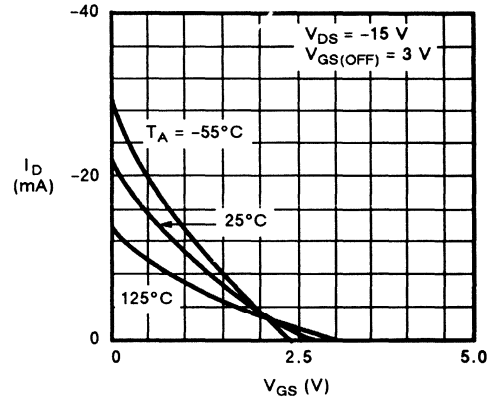
Operating Gate Current



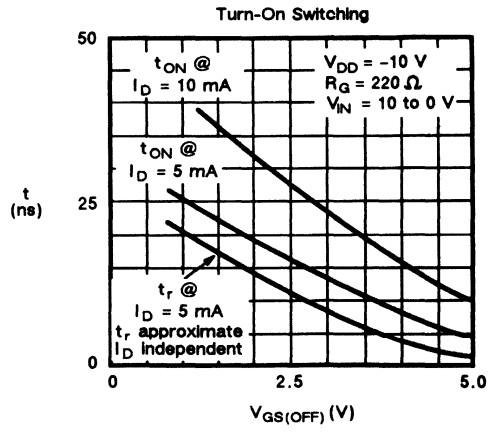
Output Characteristics ($V_{GS(OFF)}$ = 3 V)



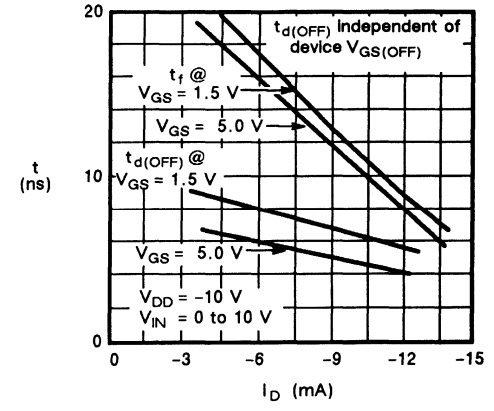
Transfer Characteristics



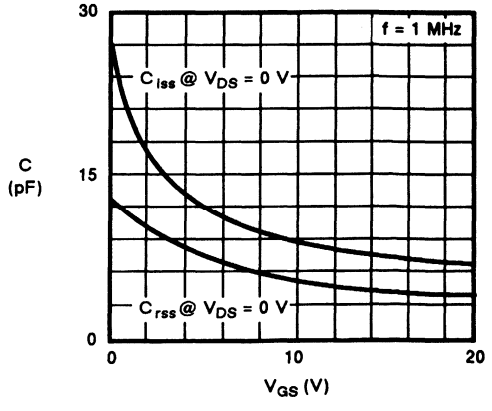
Turn-On Switching



Turn-Off Switching



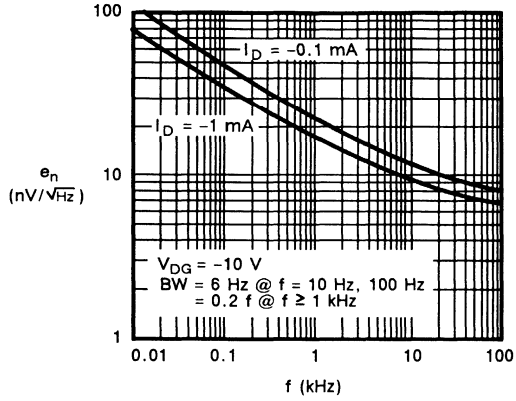
Capacitance vs. Gate-Source Voltage



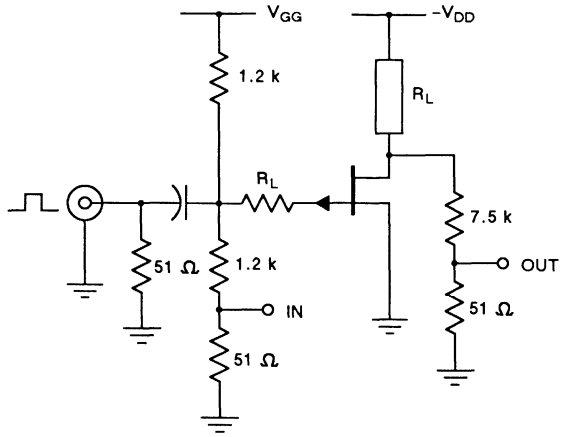
4

TYPICAL CHARACTERISTICS (Cont'd)

Noise Voltage vs. Frequency



SWITCHING CIRCUIT



DMOS 5

DMOS

INTRODUCTION

DMOS products from Siliconix utilize a lateral double-diffused MOS process to offer the ultimate low-cost yet highly reliable switches. The unique lateral construction affords all the benefits critical to small-signal switching applications. Ultra fast switching speed, exceptionally low capacitance, good off-isolation, and high operating frequency are all available to design engineers today.

Key applications which benefit from this technology include video switching and precision sample-and-hold applications. In fact, any high performance application which benefits from < 1 ns turn-on time, < 0.5 pF capacitance, and operating frequencies up to 450 MHz, should utilize Siliconix' lateral DMOS as an optimal design solution.

Packaging options are diversified and range from surface mount to hermetically sealed metal cans, and both single and quad array switches may be purchased. With our high reliability silicon gate process, full military processing is available per MIL-S-19500 on all hermetically sealed packages.

Siliconix incorporated

SD210DE SERIES
N-Channel Lateral DMOS FETs

The SD210DE Series of single-pole, single-throw analog switches is designed for high speed switchign in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. For long term reliability, this device also features a poly-silicon gate.

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
SD210DE	30	45	0.5	2
SD214DE	20	45	0.5	2

For additional design information please see performance curves DMCA/B.

TO-72 (TO-206AF) **BOTTOM VIEW**

1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE, CASE

SIMILAR PRODUCTS

- Quad Array, See SD5000 Series
- SO-14 Array, See SD5400 Series
- Zener Protection, See SD211DE Series
- SOT-143, See SST211 Series
- Chips, See DMCB Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		SD210DE	SD214DE	
Gate-Source, Gate-Drain Voltage	V_{GS}, V_{GD}	±40	±40	V
Gate-Substrate Voltage	V_{GB}	30	20	
Drain-Source Voltage	V_{DS}	30	20	
Source-Drain Voltage	V_{SD}	10	20	
Drain-Substrate Voltage	V_{DB}	30	25	
Source-Substrate Voltage	V_{SB}	15	25	
Drain Current	I_D	50	50	mA
Power Dissipation	P_D	300	300	mW
Power Derating		3	3	mW/°C
Operating Junction Temperature	T_J	-55 to 125		°C
Storage Temperature	T_{stg}	-65 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300		

5

SPECIFICATIONS[a]				LIMITS					
					SD210DE		SD214DE		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30				V
		$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ µA, Source OPEN		35	15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain OPEN		35	15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10			nA
			$V_{DS} = 20$ V	0.9				10	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10			
			$V_{SD} = 20$ V	1				10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = \pm 40$ V		0.001		0.1		0.1	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$ µA, $V_{SB} = 0$ V		0.7	0.5	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58		70		70	Ω
			$V_{GS} = 10$ V	38		45		45	
			$V_{GS} = 15$ V	30					
			$V_{GS} = 20$ V	26					
			$V_{GS} = 25$ V	24					
DYNAMIC									
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA		11	10		10		mS
Output Conductance	g_{os}	f = 1 kHz		0.9					
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5	
SWITCHING									
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω, $V_{IN} = 0$ to 5 V		0.5		1		1	ns
	t_r			0.6		1		1	
Turn-Off Time	$t_{d(OFF)}$			2					
	t_f			6					

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.

Siliconix incorporated

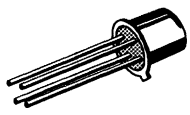
SD211DE SERIES
N-Channel Lateral DMOS FETs

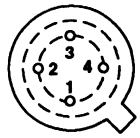
The SD211DE Series of single-pole, single-throw analog switches is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These devices also feature an integrated zener diode designed for overvoltage gate protection.

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
SD211DE	10	45	0.5	2
SD215DE	20	45	0.5	2

For additional design information please see performance curves DMCA/B.

TO-72 (TO-206AF) BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE, CASE

SIMILAR PRODUCTS

- Quad Array, See SD5000 Series
- SO-14 Array, See SD5400 Series
- SOT-143, See SST211 Series
- SD210DE, Non-Zener Protection
- Chips, See DMCB Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		SD211DE	SD215DE	
Gate-Source, Gate-Drain Voltage	V_{GS}, V_{GD}	-30/25	-25/30	V
Gate-Substrate Voltage	V_{GB}[1]	-0.3/25	-0.3/30	
Drain-Source Voltage	V_{DS}	30	20	
Source-Drain Voltage	V_{SD}	10	20	
Drain-Substrate Voltage	V_{DB}	30	25	
Source-Substrate Voltage	V_{SB}	15	25	
Drain Current	I_D	50	50	mA
Power Dissipation	P_D	300	300	mW
Power Derating		3	3	mW/°C
Operating Junction Temperature	T_J	-55 to 125		°C
Storage Temperature	T_{stg}	-65 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300		

[1]This series features an internal zener diode for gate protection

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SPECIFICATIONS[a]				LIMITS					
					SD211DE		SD215DE		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30				V
		$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ µA, Source OPEN		35	15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain OPEN		35	15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10			nA
			$V_{DS} = 20$ V	0.9				10	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10			
			$V_{SD} = 20$ V	1				10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V		10^{-5}		10		10	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$ µA, $V_{SB} = 0$ V		0.7	0.5	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58		70		70	Ω
			$V_{GS} = 10$ V	38		45		45	
			$V_{GS} = 15$ V	30					
			$V_{GS} = 20$ V	26					
			$V_{GS} = 25$ V	24					
DYNAMIC									
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA		11	10		10		mS
Output Conductance	g_{os}	f = 1 kHz		0.9					
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5	
SWITCHING									
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω, $V_{IN} = 0$ to 5 V		0.5		1		1	ns
	t_r			0.6		1		1	
Turn-Off Time	$t_{d(OFF)}$			2					
	t_f			6					

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.

Siliconix incorporated

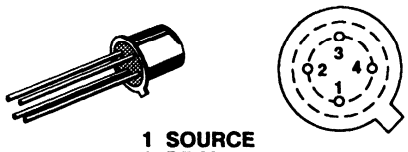
SD2100
N-Channel Depletion-Mode Lateral DMOS FET

The SD2100 is a depletion-mode MOSFET which utilizes our lateral DMOS process to provide low capacitance, fast switching, and high operating frequency. This DMOS process effectively bridges the operating frequency gap between JFETs and costly gallium-arsenide devices. The SD2100 is available in a TO-72 hermetically sealed can.

$V_{(BR)DS}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} TYP (ns)
15	50	2	1.1

For additional design information please see performance curves DMCD.

TO-72 (TO-206AF) **BOTTOM VIEW**



1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE & CASE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Source Voltage	V_{GS}	±25	V
Drain-Source Voltage	V_{DS}	25	
Drain Current	I_D	50	mA
Power Dissipation	P_D	300	mW
Power Derating		2.4	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

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SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 1$ µA		25	15		V
Gate Reverse Current	I_{GSS}	$V_{GS} = \pm 25$ V, $V_{DS} = V_{BS} = 0$ V		±0.05		±1	nA
Saturation Drain Current	I_{DSS}	$V_{DS} = 10$ V, $V_{GS} = V_{BS} = 0$ V		7	0.5	10	mA
Gate Source Cutoff	$V_{GS(OFF)}$	$V_{DS} = 10$ V, $I_D = 1$ µA, $V_{BS} = 0$ V		-1.5		-2	V
Gate-Source Voltage	V_{GS}	$V_{DG} = 10$ V, $V_{BS} = 0$ V	$I_D = 5$ mA	-0.3	-1	1	
			$I_D = 10$ mA	0.4	0	1.5	
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{BS} = 0$ V, $I_D = 1$ mA	$V_{GS} = 0$ V	120		200	Ω
			$V_{GS} = 5$ V	40		50	
DYNAMIC							
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{GS} = V_{SB} = 0$ V		8000	1000		µS
Output Conductance	g_{os}	$I_D = 20$ mA, f = 1 kHz		250		500	
Forward Transconductance	g_{fs}	$V_{DD} = 10$ V, $V_{BS} = 0$ V		10000	7000		
Output Conductance	g_{os}	$I_D = 10$ mA, f = 1 kHz		350		500	
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 10$ V, f = 1 MHz		5		6	pF
Reverse Transfer Capacitance	C_{rss}	$V_{GS} = V_{BS} = -5$ V		1		2	
SWITCHING							
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω		0.7			ns
	t_r	$V_{IN} = -4$ to -2 V		0.4			
Turn-Off Time	$t_{d(OFF)}$			5			

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.

Siliconix incorporated

SD5000 SERIES
N-Channel Lateral DMOS Quad FETs

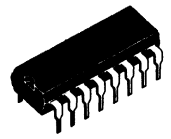
The Siliconix SD5000 Series is a monolithic array of single-pole, single-throw analog switches designed for high-speed switching in audio, video and high-frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the SD5000 is rated for analog signals of ± 10 V, while the SD5001 is rated for ± 5 V.

These bidirectional switches feature very low interelectrode capacitance and on-resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

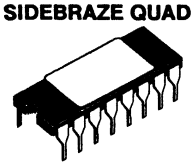
For additional design information please see performance curves DMCA/B.

PART NUMBER	$V_{GS(th)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	t_{ON} MAX (ns)	PACKAGE
SD5000N	2.0	70	2	Plastic
SD5001N	2.0	70	2	Plastic
SD5000I	2.0	70	2	Ceramic

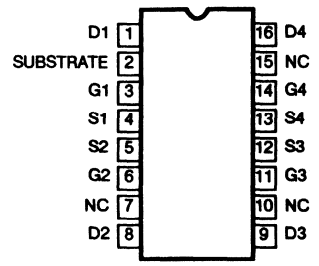
16-PIN DIP QUAD PLASTIC



16-PIN DIP SIDEBRAZE QUAD



TOP VIEW



SIMILAR PRODUCTS

- SO-14 Array, See SD5400 Series
- TO-72, See SD211DE Series
- SOT-143, See SST211 Series
- Chips, See DMCA1 Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SD5000	LIMITS SD5001	UNITS
Gate-Source, Gate-Drain Voltage		V_{GS}, V_{GD}	30/–25	25/–15	V
Drain-Substrate, Source-Substrate Voltage		V_{DB}, V_{SB}	25	15	
Drain-Source, Source-Drain Voltage		V_{DS}, V_{SD}	20	10	
Gate-Substrate Voltage[1]		V_{GB}[1]	30/–0.3	25/–0.3	
Drain Current		I_D	50		mA
Power Dissipation	Package	P_D	500		mW
	Each Device		300		
Power Derating			4		mW/°C
Operating Junction Temperature		T_J	–55 to 150		°C
Storage Temperature		T_{stg}	–65 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

[1]This series features an internal zener diode for gate protection

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SPECIFICATIONS[a]				LIMITS					
					SD5000		SD5001		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	20		10		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	20		10		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA Source OPEN		35	25		15		V
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA Drain OPEN		35	25		15		V
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4				10	nA
			$V_{DS} = 15$ V	0.7					
			$V_{DS} = 20$ V	0.9		10			
Source-Drain Leakage	$I_{DS(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{DS} = 10$ V	0.5				10	
			$V_{DS} = 15$ V	0.8					
			$V_{DS} = 20$ V	1		10			
Gate Leakage	I_{GBS}	$V_{DB} = V_{GS} = 0$ V, $V_{GB} = 30$ V		10^{-5}		1		1	µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$ µA $V_{SB} = 0$ V		0.7	0.1	2.0	0.1	2.0	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58		70		70	Ω
			$V_{GS} = 10$ V	38					
			$V_{GS} = 15$ V	30					
			$V_{GS} = 20$ V	26					
Resistance Match		$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V		1		5		5	
DYNAMIC									
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V $I_D = 20$ mA, $f = 1$ kHz		11	10		10		mS
Gate-Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5	pF
Drain-Node Capacitance	$C_{(GD+DB)}$			1.1		2.0		2.0	pF
Source-Node Capacitance	$C_{(GS+SB)}$			3.7		5		5	pF
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5	pF
Crosstalk[b]		f = 3 kHz, See Test Circuits in DMCA/B Performance Curves		-107					dB
SWITCHING									
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω $V_{IN} = 5$ V		0.5		1		1	ns
	t_r			0.6		1		1	ns
Turn-Off Time[b]	$t_{d(OFF)}$			2					ns
	t_f			6					ns

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.

Siliconix incorporated

SD5400 SERIES
N-Channel Lateral DMOS Quad FETs

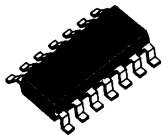
The Siliconix SD5400 series is a monolithic array of single-pole, single-throw analog switches designed for high-speed switching in audio, video and high frequency applications in communications, instrumentation, and process control. Designed with the Siliconix DMOS process, the SD5400 is rated for analog signals of ± 10 V, while the SD5401 is rated for ± 5 V.

These bidirectional switches feature very low interelectrode capacitance and on-resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

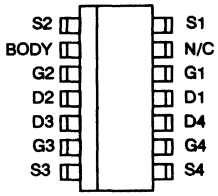
For additional design information please see performance curves DMCA/B.

PART NUMBER	$V_{(BR)DS}$ MIN (V)	$V_{GS(th)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	t_{ON} MAX (ns)
SD5400CY	20	2.0	75	2
SD5401CY	10	2.0	75	2

SO-14



TOP VIEW



SIMILAR PRODUCTS

- 16-Pin DIP, See SD5000 Series
- TO-72, See SD211DE Series
- SOT-143, See SST211 Series
- Chips, See DMCA1 Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNITS
			SD5400CY	SD5401CY	
Gate-Source, Gate-Drain Voltage		V_{GS}, V_{GD}	30/-25	25/-15	V
Drain-Substrate, Source-Substrate Voltage		V_{DB}, V_{SB}	25	15	
Drain-Source, Source-Drain Voltage		V_{DS}, V_{SD}	20	10	
Gate-Substrate Voltage[1]		V_{GB}[1]	30/-0.3	25/-0.3	
Drain Current		I_D	50		mA
Power Dissipation	Package	P_D	500		mW
	Each Device		300		
Power Derating			5		mW/°C
Operating Junction Temperature		T_J	-55 to 125		°C
Storage Temperature		T_{stg}	-55 to 125		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

[1]This series features an internal zener diode for gate protection

5

SPECIFICATIONS[a]				LIMITS					
					SD5400CY		SD5401CY		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	20		10		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	20		10		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA Source OPEN		35	25		15		V
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA Drain OPEN		35	25		15		V
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4				10	nA
			$V_{DS} = 20$ V	0.9		10			nA
Source-Drain Leakage	$I_{DS(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{DS} = 10$ V	0.5				10	nA
			$V_{DS} = 20$ V	1		10			nA
Gate Leakage	I_{GBS}	$V_{DB} = V_{GS} = 0$ V, $V_{GB} = 30$ V		10^{-5}		1		1	µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$ µA $V_{SB} = 0$ V		0.7	0.1	2.0	0.1	2.0	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58		75		75	Ω
			$V_{GS} = 10$ V	38					Ω
			$V_{GS} = 15$ V	30					Ω
			$V_{GS} = 20$ V	26					Ω
Resistance Match		$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V		1		5		5	
DYNAMIC									
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V $I_D = 20$ mA, $f = 1$ kHz		11	9		9		mS
Gate-Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5	pF
Drain-Node Capacitance	$C_{(GD+DB)}$			1.1		2		2	pF
Source-Node Capacitance	$C_{(GS+SB)}$			3.7		6		6	pF
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5	pF
Crosstalk[b]		$f = 3$ kHz		-107					dB
SWITCHING									
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω $V_{IN} = 5$ V		0.5		1		1	ns
	t_r			0.6		1		1	ns
Turn-Off Time[b]	$t_{d(OFF)}$			2					ns
	t_f			6					ns

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.

Siliconix incorporated

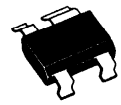
SST211 SERIES
N-Channel Lateral DMOS FETs

The SST211 Series single-pole, single-throw analog switches is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These devices also feature an integrated zener diode designed to protect the gate from electrical overvoltage.

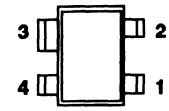
PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
SST211	30	75	0.5	2
SST215	20	75	0.5	2

For additional design information please see performance curves DMCA/B.

SOT-143



TOP VIEW



1 DRAIN
2 GATE
3 SUBSTRATE
4 SOURCE

SIMILAR PRODUCTS

- Quad Array, See SD5000 Series
- SO-14 Array, See SD5400 Series
- TO-72, See SD211DE Series
- Chips, See DMCB Series Die

PRODUCT MARKING	
SST211	D11
SST215	D15

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS SST211	LIMITS SST215	UNITS
Gate-Source, Gate-Drain Voltage	V_{GS}, V_{GD}	-30/25	-25/30	V
Gate-Substrate Voltage	V_{GB}[1]	-0.3/25	-0.3/30	
Drain-Source Voltage	V_{DS}	30	20	
Source-Drain Voltage	V_{SD}	10	20	
Drain-Substrate Voltage	V_{DB}	30	25	
Source-Substrate Voltage	V_{SB}	15	25	
Drain Current	I_D	50	50	mA
Power Dissipation	P_D	350	350	mW
Power Derating		3.5	3.5	mW/°C
Operating Junction Temperature	T_J	-55 to 125		°C
Storage Temperature	T_{stg}	-65 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300		

[1]This device features an internal zener diode for gate protection

5

SPECIFICATIONS[a]				LIMITS					
					SST211		SST215		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30				V
		$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ µA, Source OPEN		35	15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain OPEN		35	15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10			nA
			$V_{DS} = 20$ V	0.9				10	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10			
			$V_{SD} = 20$ V	1				10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V		10^{-5}		10		10	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$ µA, $V_{SB} = 0$ V		0.7	0.5	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58		75		75	Ω
			$V_{GS} = 10$ V	38		50		50	
			$V_{GS} = 15$ V	30					
			$V_{GS} = 20$ V	26					
			$V_{GS} = 25$ V	24					
DYNAMIC									
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA		11	9		9		mS
Output Conductance	g_{os}	f = 1 kHz		0.9					
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		6		6	
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5	
SWITCHING									
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\ \Omega$, $V_{IN} = 0$ to 5 V		0.5		1		1	ns
	t_r			0.6		1		1	
Turn-Off Time	$t_{d(OFF)}$			2					
	t_f			6					

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.

DMOS DIE

Siliconix incorporated

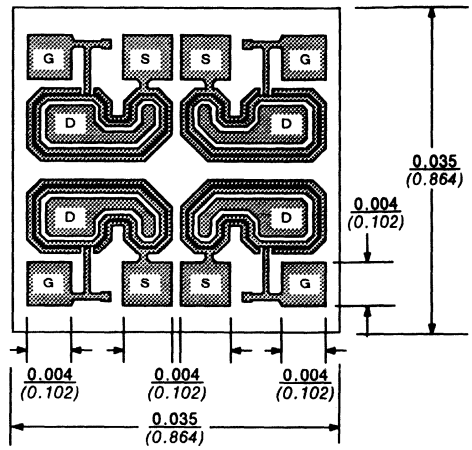
DMCA1 DIE
N-Channel Lateral DMOS Quad FETs

The Siliconix DMCA1 Die is a monolithic array of single-pole, single-throw analog switches designed for high-speed switching in audio, video and high-frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the product is rated for analog signals of ± 10 V.

These bidirectional switches feature very low interelectrode capacitance and on-resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage is 2 V maximum, simplifying driver requirements for low level signal applications.

For additional design information please consult the typical performance curves DMCA/B.

DMCA1CHP*
SD5000I SD5000N SD5001N SD5400CY SD5401CY
*Meets or exceeds specification for all part numbers listed below



Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Ultra-High Speed Switching
- High Gain Amplifiers

FEATURES

- < 1 ns Switching t_{ON}
  Ultra-Low Capacitance C_G < 3.5 pF
- g_{fs} (gain) > 10000 µmhos

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Source, Gate-Drain Voltage	V_{GS}, V_{GD}	30/–25	V
Drain-Substrate, Source-Substrate Voltage	V_{DB}, V_{SB}	25	
Drain-Source, Source-Drain Voltage	V_{DS}, V_{SD}	20	
Gate-Substrate Voltage	V_{GB}[1]	30/–0.3	
Drain Current	I_D	50	mA
Storage Temperature	T_{stg}	–65 to 150	°C

[1]This series features an internal zener diode for gate protection

5

DMCA1 DIE

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	20		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN		35	25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain OPEN		35	25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V, $V_{DS} = 20$ V		0.9			nA
Source-Drain Leakage	$I_{DS(OFF)}$	$V_{GD} = V_{BD} = -5$ V, $V_{DS} = 20$ V		1			
Gate Leakage	I_{GBS}	$V_{DB} = V_{GS} = 0$ V, $V_{GB} = 30$ V		10^{-5}			µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$ µA, $V_{SB} = 0$ V		0.7	0.1	2.0	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58			Ω
			$V_{GS} = 10$ V	38			
			$V_{GS} = 15$ V	30			
			$V_{GS} = 20$ V	26			
Resistance Match		$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V		1			
DYNAMIC							
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, $f = 1$ kHz		11			mS
Gate-Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz, $V_{GS} = V_{BS} = -15$ V		2.5			pF
Drain-Node Capacitance	$C_{(GD+DB)}$			1.1			
Source-Node Capacitance	$C_{(GS+SB)}$			3.7			
Reverse Transfer Capacitance	C_{rss}			0.2			
Crosstalk		f = 3 kHz, See Test Circuits in DMCA Performance Curves		-107			dB
SWITCHING							
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω, $V_{IN} = 5$ V		0.5			ns
	t_r			0.6			
Turn-Off Time	$t_{d(OFF)}$			2			
	t_f			6			

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.

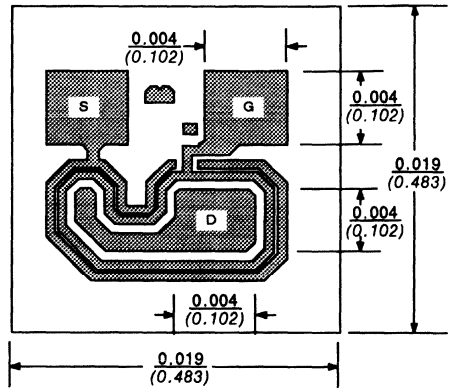
Siliconix incorporated

DMCB SERIES DIE
N-Channel Lateral DMOS FETs

The DMCB Series of single-pole, single-throw analog switches is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance of ultra-fast switching speeds. The DMCB Series also features an integrated zener diode designed to protect the gate from electrical "Spikes" or overstress.

DMCB1CHP*	DMCB2CHP*
SD210DE SD214DE	SD211DE SD215DE SST211 SST215
*Meets or exceeds specification for all part numbers listed below	

For additional design information please consult the typical performance curves DMCA/B.



Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Ultra-High Speed Switching
- High Gain Amplifiers

FEATURES

- < 1 ns Switching t_{ON}
  Ultra-Low Capacitance C_G < 3.5 pF
- g_{fs} (gain) > 10000 µmhos

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		DMCB1CHP	DMCB2CHP	
Gate-Source, Gate-Drain Voltage	V_{GS}, V_{GD}	±40	-30/25	V
Gate-Substrate Voltage	V_{GB}	±40	-0.3/25	
Drain-Source Voltage	V_{DS}	30		
Source-Drain Voltage	V_{SD}	10		
Drain-Substrate Voltage	V_{DB}	30		
Source-Substrate Voltage	V_{SB}	15		
Drain Current	I_D	50		mA
Storage Temperature	T_{stg}	-65 to 200		°C

5

DMCB SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS					
					DMCB1CHP		DMCB2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30		30		V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	20		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	20		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA Source OPEN		35	25		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA Drain OPEN		35	25		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4					nA
			$V_{DS} = 20$ V	0.9					
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{DS} = 10$ V	0.5					
			$V_{DS} = 20$ V	1					
Gate Leakage	I_{GBS}	$V_{DB} = V_{GS} = 0$ V, $V_{GB} = 30$ V		10^{-5}					µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$ µA $V_{SB} = 0$ V		0.7	0.5	2	0.5	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58					Ω
			$V_{GS} = 10$ V	38					
			$V_{GS} = 15$ V	30					
			$V_{GS} = 20$ V	26					
			$V_{GS} = 25$ V	24					
DYNAMIC									
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V		11					mS
Output Conductance	g_{os}	$I_D = 20$ mA, f = 1 kHz		0.9					
Gate-Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, f = 1 MHz $V_{GS} = V_{BS} = -15$ V		2.5					pF
Drain-Node Capacitance	$C_{(GD+DB)}$			1.1					
Source-Node Capacitance	$C_{(GS+SB)}$			3.7					
Reverse Transfer Capacitance	C_{rss}			0.2					
SWITCHING									
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω $V_{IN} = 0$ to 5 V		0.5					ns
	t_r			0.8					
Turn-Off Time	$t_{d(OFF)}$			2					
	t_f			6					

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.

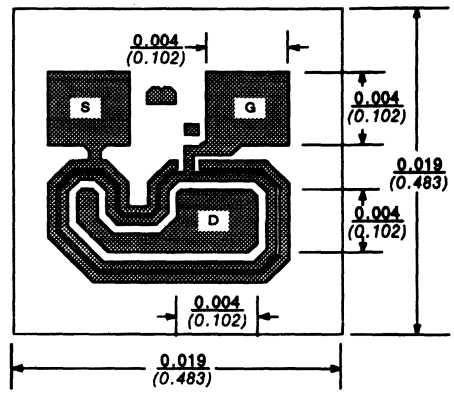
Siliconix incorporated

DMCD1 DIE
N-Channel Depletion-Mode Lateral DMOS FETs

The DMCD is a depletion-mode MOSFET which utilizes our lateral DMOS process to provide low capacitance, fast switching, and high operating frequency. This DMOS process effectively bridges the operating frequency gap between JFETs and costly gallium-arsenide devices.

DMCD1CHP*
SD2100
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves DMCD.



Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- High-Gain Amplification
- Analog Switching

FEATURES

- High g_{fs} > 10 mS (Typically)

5

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	±25	V
Gate-Source Voltage	V_{GS}	25	
Drain Current	I_D	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

DMCD1 DIE

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	V_{GS} = V_{BS} = -5 V, I_D = 1 µA		25	15		V
Gate Reverse Current	I_{GSS}	V_{GS} = ±25 V, V_{DS} = V_{BS} = 0 V		±0.05			nA
Saturation Drain Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = V_{BS} = 0 V		7	0.5	10	mA
Gate Source Cutoff	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 µA, V_{BS} = 0 V		-1.5		-2	V
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, V_{BS} = 0 V	I_D = 5 mA	-0.3			
			I_D = 10 mA	0.4			
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{BS} = 0 V, I_D = 100 µA	V_{GS} = 0 V	120		200	Ω
			V_{GS} = 5 V	40		50	
DYNAMIC							
Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = V_{SB} = 0 V		8000	1000		µS
Output Conductance	g_{os}	f = 1 kHz		250		500	
Forward Transconductance	g_{fs}	V_{DG} = 10 V, V_{BS} = 0 V		10000	7000		
Output Conductance	g_{os}	I_D = 10 mA, f = 1 kHz		350		500	
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, f = 1 MHz		5			pF
Reverse Transfer Capacitance	C_{rss}	V_{GS} = V_{BS} = -5 V		1			
SWITCHING							
Turn-On Time	$t_{d(ON)}$	V_{DD} = 5 V, R_L = 680 Ω		0.7			ns
	t_r	V_{IN} = -4 to -2 V		0.4			
Turn-Off Time	$t_{d(OFF)}$			5			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.

DMOS
PERFORMANCE CURVES

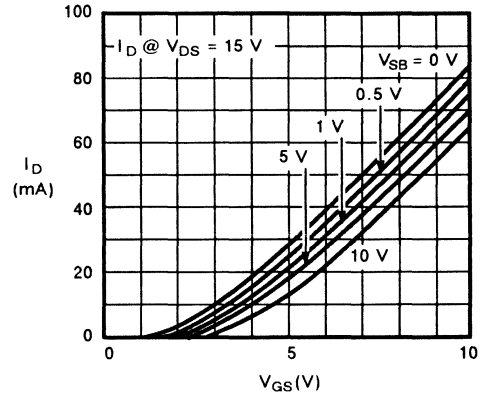
Siliconix incorporated

DMCA/B
N-Channel JFET
Enhancement-Mode DMOS FET

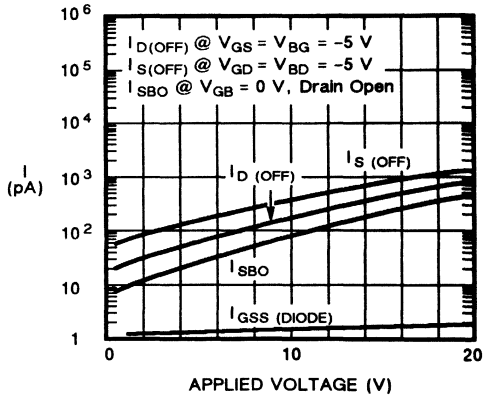
TYPE	PACKAGE	DEVICE
Single	TO-72 (TO-206AF)	• SD210DE, SD211DE, SD214DE, SD215DE
Single	SOT-143	• SST211, SST215
Quads	Dual-In-Line 16-Pin Sidebraze	• SD5000I
Quads	Dual-In-Line 16-Pin Plastic	• SD5000N, SD5001N
Quads	Surface Mount	• SD5400CY, SD5401CY,
Quads	Chip/Wafer	• Available as DMCA1CHP, DMCB1CHP, DMCB2CHP

TYPICAL CHARACTERISTICS

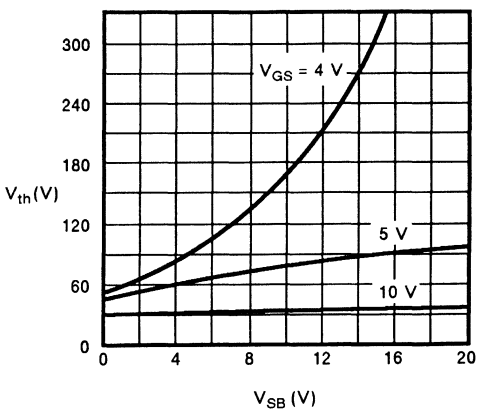
Drain Current vs. Gate-Source Voltage



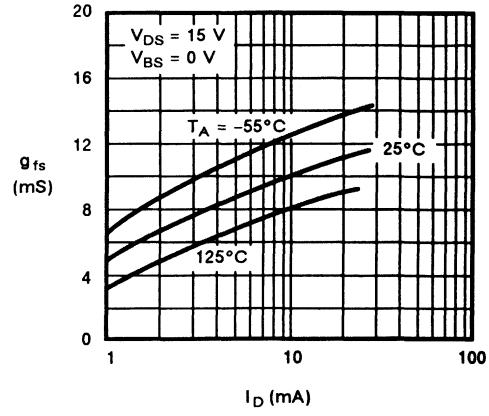
Leakage Current vs. Applied Voltage



On-Resistance vs. Gate-Source Voltage



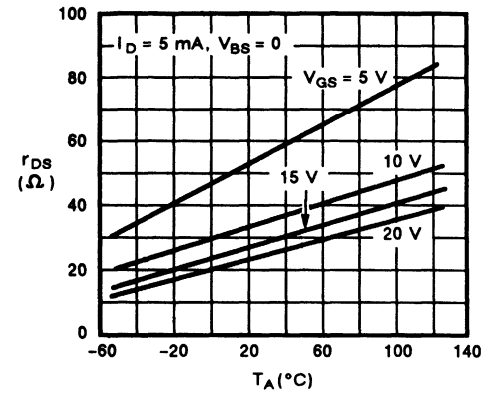
Common-Source Forward Transconductance vs. Drain Current



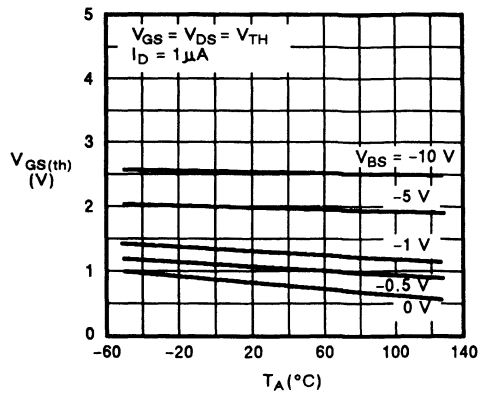
5

TYPICAL CHARACTERISTICS (Cont'd)

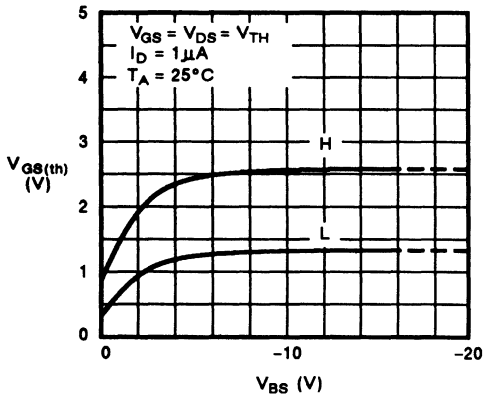
On-Resistance vs. Temperature



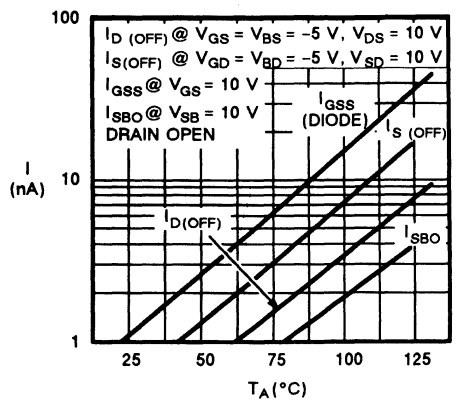
Threshold Voltage vs. Temperature



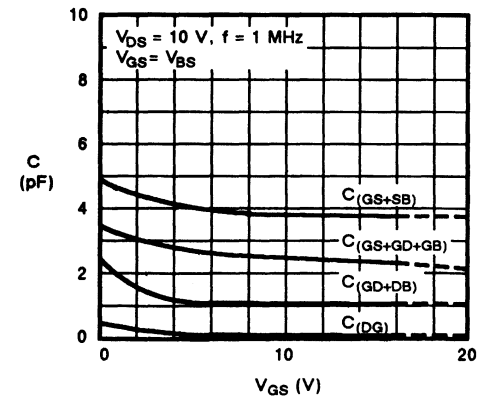
Threshold Voltage vs. Substrate-Source Voltage



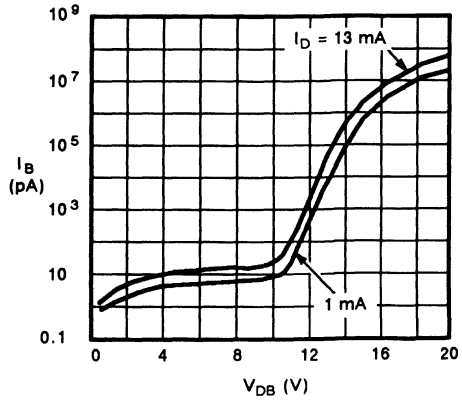
Leakage Currents vs. Temperature



Capacitance vs. Gate-Source Voltage

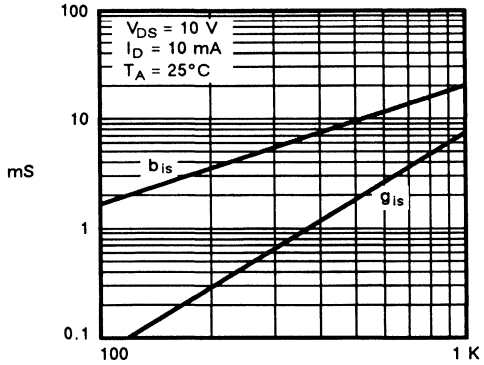


Body Leakage Current vs. Drain-Body Voltage

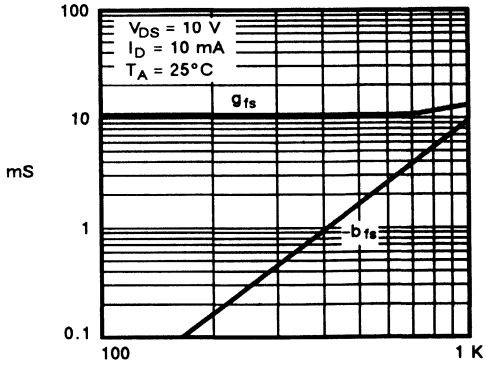


TYPICAL CHARACTERISTICS (Cont'd)

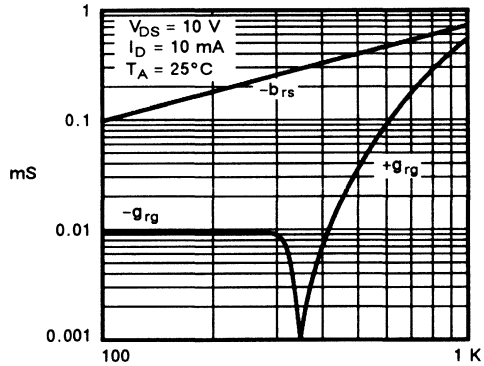
Input Admittance



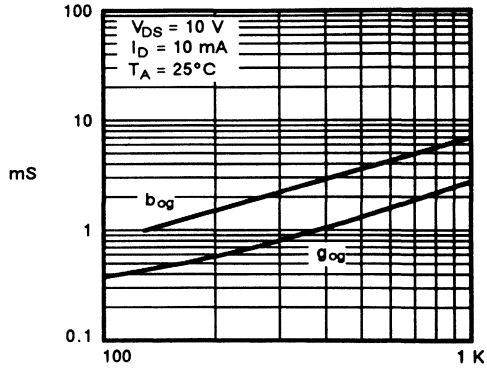
Forward Admittance



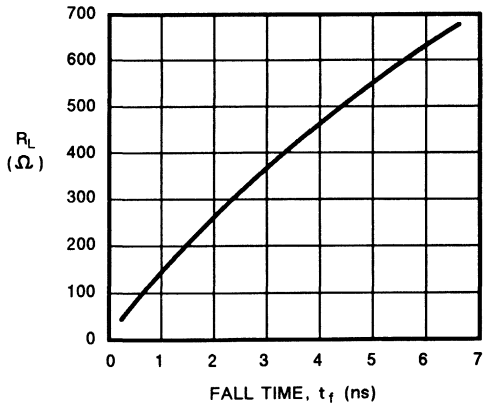
Reverse Admittance



Output Admittance



Switching Characteristics



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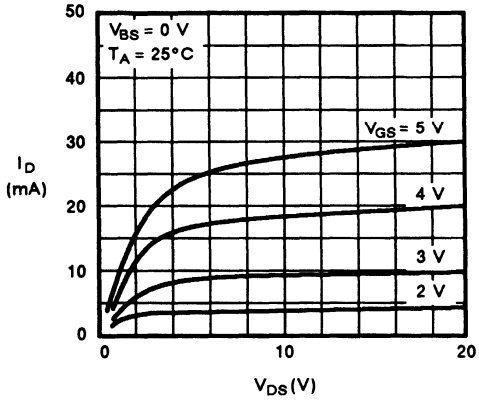
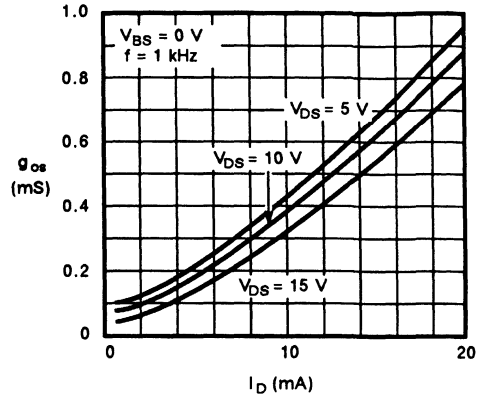
TYPICAL CHARACTERISTICS (Cont'd)

Output Characteristics



Output Conductance vs. Drain Current

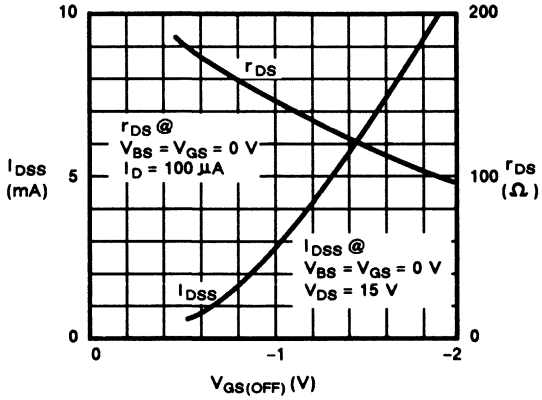


DMCD
N-Channel
Depletion-Mode MOSFET

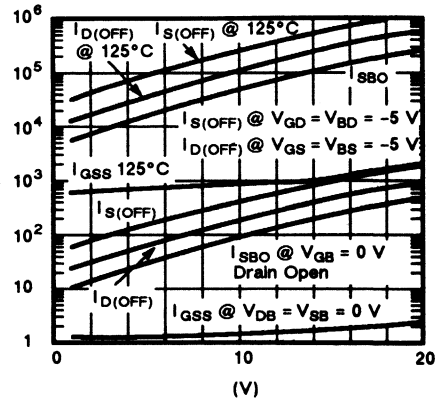
TYPE	PACKAGE	DEVICE
Single	TO-72 (TO-206AF)	• SD2100
Single	Chip	• Available as DMCD1CHP

TYPICAL CHARACTERISTICS

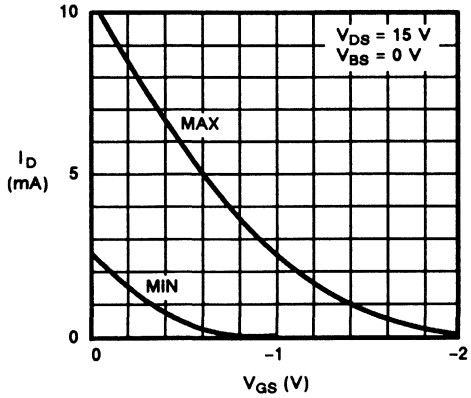
Depletion Mode - Drain Current & On-Resistance vs. Gate-Source Cutoff Voltage



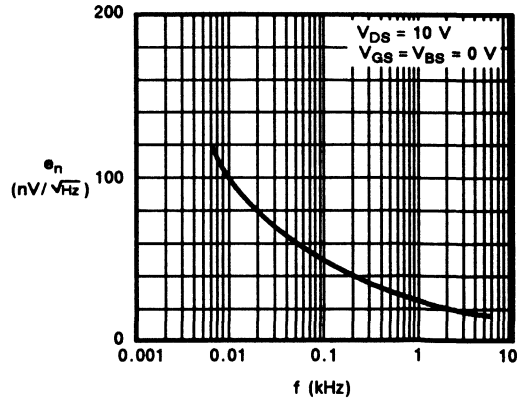
Leakage Currents vs. Applied Voltage



Transfer Characteristics



Equivalent Input Noise Voltage vs. Frequency



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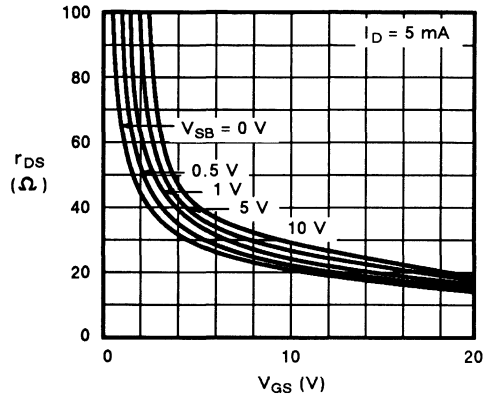
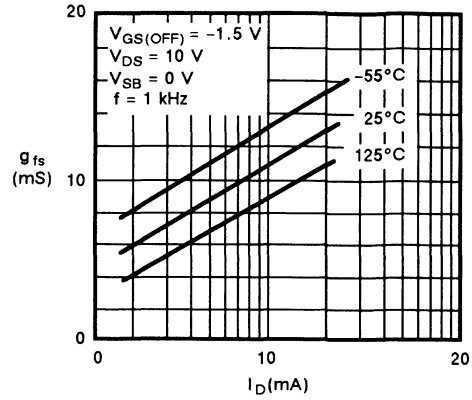
TYPICAL CHARACTERISTICS (Cont'd)

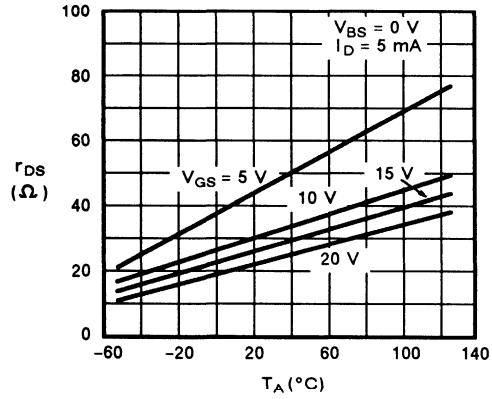
Drain-Source On-Resistance vs. Gate-Source Voltage



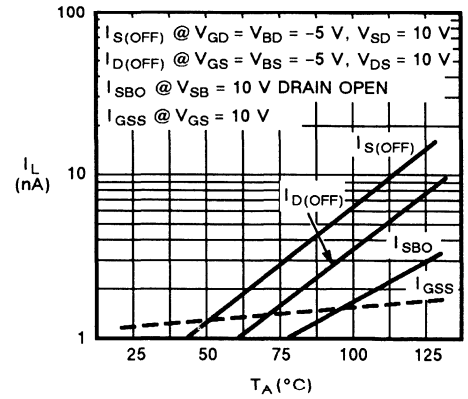
Common-Source Forward Transconductance vs. Drain Current



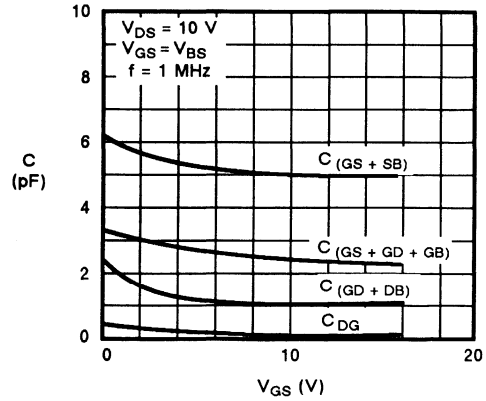
On-Resistance vs. Temperature



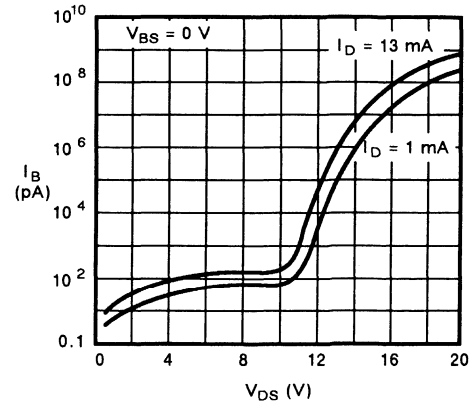
Leakage Current vs. Temperature



Capacitance vs. Gate-Source Voltage

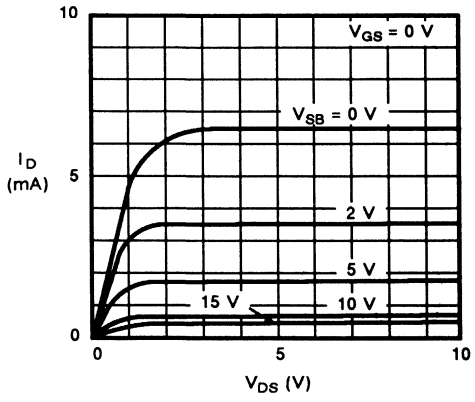


Body-Channel Leakage Current vs. Drain-Source Voltage

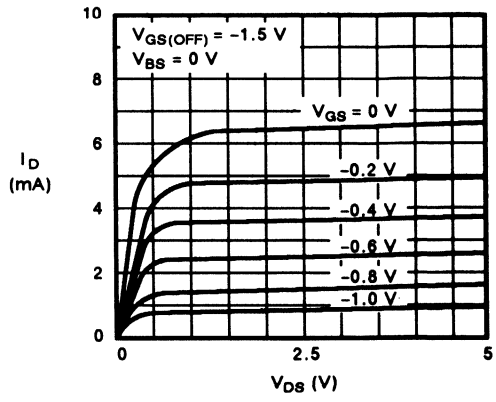


TYPICAL CHARACTERISTICS (Cont'd)

Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



Output Characteristics



5

General Information
Cross Reference
Selector Guide
JFETs
CMOS
Low Power MOS 6
Package Outlines
Applications
Publications Index
Worldwide Sales Offices and Distributors

LOW POWER MOS

INTRODUCTION

Low Power MOS products from Siliconix utilize a vertical DMOS process to offer a wide range of both n- and p-channel enhancement-mode and n-channel depletion-mode devices. The vertical structure allows high breakdown voltage, low on-resistance, low capacitance, and fast switching. Inherent in the MOS process, these devices also feature a high-impedance gate and freedom from the thermal runaway typically associated with bipolar devices.

To meet a wide range of applications, Siliconix Low Power MOS product line features n-channel enhancement-mode devices with breakdown voltages ranging from 30 – 500 volts, on-resistances as low as 1.2 Ω, and many devices with threshold voltages at 2 volts or less. P-channel devices designed to complement n-channel products are offered with breakdown voltage ranging from 30 – 240 volts, on-resistances as low as 1.8 Ω, and a family of low threshold devices again with threshold voltages less than 2.0 volts.

A recent unique addition to this product line was a family of high-voltage n-channel depletion-mode products. This series features normally "on" operation, breakdown voltages up to 240 volts, and on-resistances as low as 6 Ω. Depletion-mode performance is perfect for use in telecommunications and industrial process control applications.

Packaging options are diverse and include SOT-23, TO-92 (TO-226AA), TO-237, and 14-pin DIPs for commercial applications and TO-72 (TO-206AF), TO-52 (TO-206AC), and 14-pin ceramic packages for demanding industrial or military applications. Full military processing is available per MIL-S-19500 on all hermetically sealed packages.

For additional technical information please see "High-Side Switching" (LPD-4), and "Depletion-mode Applications" (LPD-5). These application notes are located in Section 8 and provide useful design tips and device information.

Siliconix incorporated

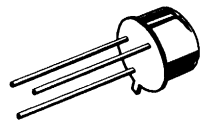
2N6659
N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

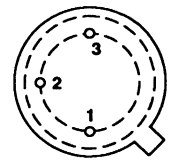
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
35	1.8	0.18

Performance Curves: VNDQ06

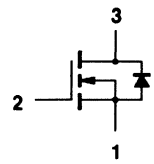
TO-39 (TO-205AD)



BOTTOM VIEW



1 SOURCE
2 GATE
3 & CASE-DRAIN



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	35	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[1]	T_C = 25°C	I_D	1.4	A
	T_C = 100°C		1	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_C = 100°C		2.5	
Operating Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range[2]		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient[2]	R_{thJA}	170	K/W
Junction-to-Case	R_{thJC}	20	

[1]Pulse width limited by maximum junction temperature
[2]This parameter not registered with JEDEC

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	70	35		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
		T_C = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 35 V, V_{GS} = 0 V			10	µA
		V_{DS} = 28 V, V_{GS} = 0 V, T_C = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	[d]V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		1.8	
		T_C = 125°C[d]	2.6		3.6	
Drain-Source On-Voltage[c]	$V_{DS(ON)}$	[d]V_{GS} = 5 V, I_D = 0.3 A	0.54		1.5	V
		V_{GS} = 10 V, I_D = 1 A	1.3		1.8	
		T_C = 125°C[d]	2.6		3.6	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[c, d]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Small Signal Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 10 V, I_D = 1 A, f = 1 kHz	1.3		1.8	Ω
Drain-Source Capacitance	C_{ds}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	30		40	pF
Input Capacitance	C_{iss}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	38		50	
Output Capacitance[d]	C_{oss}		28		40	
Reverse Transfer Capacitance	C_{rss}		8		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		10	nS
Turn-Off Time	t_{OFF}		9		10	

NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 80 µS, duty cycle ≤ 1%.
d. This parameter not registered with JEDEC.

Siliconix incorporated

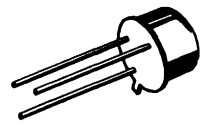
2N6660
N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

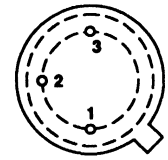
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	3	1.1

Performance Curves: VNDQ06

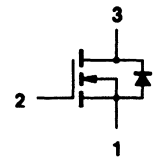
TO-39 (TO-205AD)



BOTTOM VIEW



1 SOURCE
2 GATE
3 & CASE-DRAIN



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	1.1	A
	T_C = 100°C		0.8	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_C = 100°C		2.5	
Operating Junction Temperature Range[2]		T_J	-55 to 150	°C
Storage Temperature Range		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient[2]	R_{thJA}	170	K/W
Junction-to-Case	R_{thJC}	20	

[1]Pulse width limited by maximum junction temperature
[2]This parameter not registered with JEDEC

6

Siliconix incorporated

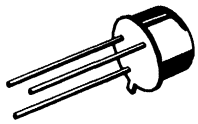
SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
		T_C = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_C = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	[d]V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3	
		T_C = 125°C[d]	2.6		4.2	
Drain-Source On-Voltage[c]	$V_{DS(ON)}$	[d]V_{GS} = 5 V, I_D = 0.3 A	0.54		1.5	V
		V_{GS} = 10 V, I_D = 1 A	1.3		3	
		T_C = 125°C[d]	2.6		4.2	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[c, d]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Small Signal Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 10 V, I_D = 1 A, f = 1 kHz	1.3		3	Ω
Drain-Source Capacitance	C_{ds}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	30		40	pF
Input Capacitance	C_{iss}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	38		50	
Output Capacitance[d]	C_{oss}		28		40	
Reverse Transfer Capacitance	C_{rss}		8		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	8		10	nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9		10	

NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 80 µS, duty cycle ≤ 1%.
d. This parameter not registered with JEDEC.

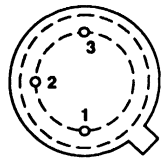
Siliconix incorporated

2N6660 JANTX, JANTXV
N-Channel Enhancement-Mode MOS Transistor

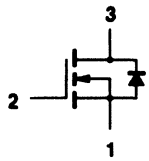
TO-39 (TO-205AD)



BOTTOM VIEW



1 SOURCE
2 GATE
3 & CASE-DRAIN



PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	3	1.1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	0.99	A
	T_C = 100°C		0.62	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_A = 25°C		0.725	
Operating Junction Temperature Range		T_J	-65 to 150	°C
Storage Temperature Range		T_{stg}	-65 to 175	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	170	K/W
Junction-to-Case	R_{thJC}	20	

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**TYP[b]**	**MIN**	**MAX**	**UNIT**
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	90	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2	
		T_C = -55°C	1.9		2.5	
		T_C = 125°C	1	0.3		
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
		T_C = 125°C			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		T_C = 125°C			100	
On-State Drain Current[c, d]	$I_{D(ON)}$	V_{DS} = 7.5 V, V_{GS} = 10 V	2			A
Drain-Source On-Resistance[c, e]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	3.5		5	Ω
		V_{GS} = 10 V, I_D = 1 A	2.25		3	
		T_C = 125°C	4		5.6	
Drain-Source On-Voltage[c]	$V_{DS(ON)}$	$^dV_{GS}$ = 5 V, I_D = 0.3 A	1.05		1.5	V
		V_{GS} = 10 V, I_D = 1 A	2.25		3	
		T_C = 125°C	4		5.6	
Forward Transconductance[c]	g_{FS}	V_{DS} = 7.5 V, I_D = 0.525 A	275	170		mS
Common Source Output Conductance[c, d]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	900			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	30		50	pF
Output Capacitance	C_{oss}		30		40	
Reverse Transfer Capacitance	C_{rss}		5		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 50 Ω	7		10	nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	6		10	
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS[a]						
Forward Voltage	V_{SD}	I_S = 0.99 A	0.8	0.7	1.6	V

NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 80 µS, duty cycle ≤ 1%.
d. This parameter not registered with MIL-S-19500/547A.
e. Not a measured value $r_{DS(ON)}$ = $V_{DS(ON)}/I_D$.

Siliconix incorporated

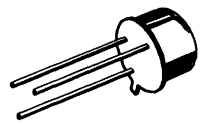
2N6661
N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

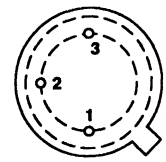
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
90	4	0.9

Performance Curves: VNDQ09

TO-39 (TO-205AD)



BOTTOM VIEW



1 SOURCE
2 GATE
3 & CASE-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	90	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	0.9	A
	T_C = 100°C		0.7	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_C = 100°C		2.5	
Operating Junction Temperature Range[2]		T_J	-55 to 150	°C
Storage Temperature Range		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	170	K/W

[1]Pulse width limited by maximum junction temperature
[2]This parameter not registered with JEDEC

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	120	90		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.6	0.8	2	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
		T_C = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 90 V, V_{GS} = 0 V			10	µA
		V_{DS} = 72 V, V_{GS} = 0 V, T_C = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 15 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	[d]V_{GS} = 5 V, I_D = 0.3 A	4.2		5.3	Ω
		V_{GS} = 10 V, I_D = 1 A	3.6		4	
		T_C = 125°C[d]	6.8		9	
Drain-Source On-Voltage[c]	$V_{DS(ON)}$	[d]V_{GS} = 5 V, I_D = 0.3 A	1.26		1.6	V
		V_{GS} = 10 V, I_D = 1 A	3.6		4	
		T_C = 125°C[d]	6.8		9	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[c, d]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	225			µS
DYNAMIC						
Small Signal Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 10 V, I_D = 1 A, f = 1 kHz	3.6		4	Ω
Drain-Source Capacitance	C_{ds}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	30		40	pF
Input Capacitance	C_{iss}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	35		50	
Output Capacitance[d]	C_{oss}		15		40	
Reverse Transfer Capacitance	C_{rss}		2		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	6		10	nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	8		10	

NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 80 µS, duty cycle ≤ 1%.
d. This parameter not registered with JEDEC.

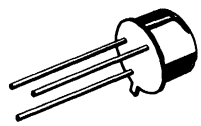
Siliconix incorporated

2N6661 JANTX, JANTXV
N-Channel Enhancement-Mode MOS Transistor

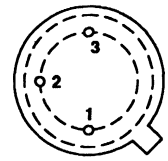
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
90	4	0.86

TO-39 (TO-205AD)



BOTTOM VIEW



1 SOURCE
2 GATE
3 & CASE-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	90	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	0.86	A
	T_C = 100°C		0.54	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_A = 25°C		0.725	
Operating Junction Temperature Range		T_J	-65 to 150	°C
Storage Temperature Range		T_{stg}	-65 to 175	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	170	K/W
Junction-to-Case	R_{thJC}	20	

[1]Pulse width limited by maximum junction temperature

6

2N6661 JANTX, JANTXV

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	130	90		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.8	2	
		T_C = -55°C			2.5	
		T_C = 125°C		0.3		
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
		T_C = 125°C			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 72 V, V_{GS} = 0 V	0.01		1	µA
		T_C = 125°C	30		100	
On-State Drain Current[c, d]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.7			A
Drain-Source On-Resistance[c, e]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	4.3		5.3	Ω
		V_{GS} = 10 V, I_D = 1 A	2.75		4	
		T_C = 125°C	5		7.5	
Drain-Source On-Voltage[c]	$V_{DS(ON)}$	[d]V_{GS} = 5 V, I_D = 0.3 A	1.3		1.6	V
		V_{GS} = 10 V, I_D = 1 A	2.75		4	
		T_C = 125°C	5		7.5	
Forward Transconductance[c]	g_{FS}	V_{DS} = 7.5 V, I_D = 0.475 A	250	170		mS
Common Source Output Conductance[c, d]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	425			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	30		50	pF
Output Capacitance	C_{oss}		30		40	
Reverse Transfer Capacitance	C_{rss}		5		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 50 Ω	8.5		10	nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9.6		10	
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS[a]						
Forward Voltage	V_{SD}	I_S = 0.86 A	0.9	0.7	1.4	V

NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 80 µS, duty cycle ≤ 1%.
d. This parameter not registered with MIL-S-19500/547A.
e. Not a measured value $r_{DS(ON)} = V_{DS(ON)}/I_D$.

Siliconix incorporated

2N7000
N-Channel Enhancement-Mode MOS Transistor

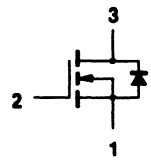
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	5	0.2

Performance Curves: VNDS06

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±40	
Continuous Drain Current	T_A = 25°C	I_D	±0.2	A
	T_A = 100°C		0.13	
Pulsed Drain Current[1]		I_{DM}	0.5	
Power Dissipation[1]	T_A = 25°C	P_D	0.4	W
	T_A = 100°C		0.16	
Operating Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	312.5	K/W

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	3	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		T_C = 125°C			1000	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	210	75		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	[d]V_{GS} = 4.5 V, I_D = 75 mA	4.8		5.3	Ω
		V_{GS} = 10 V, I_D = 0.5 A	2.5		5	
		T_C = 125°C	4.4		9	
Drain-Source On-Voltage[c]	$V_{DS(ON)}$	[d]V_{GS} = 4.5 V, I_D = 75 mA	0.36		0.4	V
		V_{GS} = 10 V, I_D = 0.5 A	1.25		2.5	
		T_C = 125°C[d]	2.2		4.5	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A	170	100		mS
Common Source Output Conductance[c, d]	g_{OS}	V_{DS} = 5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60	pF
Output Capacitance[d]	C_{oss}		11		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 25 Ω, I_D = 0.5 A V_{GEN} = 10 V, R_G = 25 Ω	7		10	nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	7		10	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

Siliconix incorporated

2N7002
N-Channel Enhancement-Mode MOS Transistor

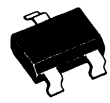
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	7.5	0.115

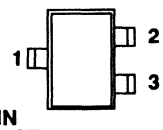
Performance Curves: VNDS06

PRODUCT MARKING	
2N7002	702

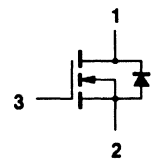
SOT-23



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±40	
Continuous Drain Current	T_A = 25°C	I_D	±0.115	A
	T_A = 100°C		±0.073	
Pulsed Drain Current[1]		I_{DM}	0.8	
Power Dissipation	T_A = 25°C	P_D	200	mW
	T_A = 100°C		80	
Operating Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	625	K/W

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA	2.15	1	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		T_C = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = ≥ 2 $V_{DS(ON)}$, V_{GS} = 10 V	1000	500		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 50 mA	5		7.5	Ω
		T_C = 125°C	9		13.5	
		V_{GS} = 10 V, I_D = 0.5 A	2.5		7.5	
		T_C = 125°C	4.4		13.5	
Drain-Source On-Voltage[c]	$V_{DS(ON)}$	V_{GS} = 5 V, I_D = 50 mA	0.25		0.375	V
		V_{GS} = 10 V, I_D = 0.5 A	1.25		3.75	
		T_C = 125°C[d]	2.2		6.75	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A	170	80		mS
Common Source Output Conductance[c, d]	g_{OS}	V_{DS} = 5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		50	pF
Output Capacitance[d]	C_{oss}		11		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 30 V, R_L = 150 Ω, I_D = 0.2 A V_{GEN} = 10 V, R_G = 25 Ω	7		20	nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	7		20	

NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 80 µS, duty cycle ≤ 1%.
d. This parameter not registered with JEDEC.

Siliconix incorporated

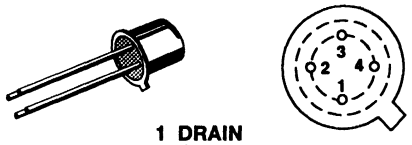
3N163 SERIES
P-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

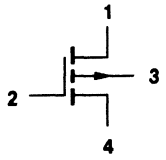
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
3N163	-40	250	-50
3N164	-30	300	-50

Performance Curves: MRA

TO-72 (TO-206AF) BOTTOM VIEW



1 DRAIN
2 GATE
3 SUBSTRATE, CASE
4 SOURCE



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS 3N163	LIMITS 3N164	UNITS
Drain-Source Voltage	V_{DS}	-40	-30	V
Gate-Source Voltage	V_{GS}	±40	±30	
Transient Gate-Source Voltage		±125		
Continuous Drain Current	I_D	-50		mA
Power Dissipation	P_D	375		mW
Power Derating		3		
Operating Junction Temperature	T_J	-55 to 150		°C
Storage Temperature	T_{stg}	-65 to 200		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300		

6

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				3N163		3N164		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{DS} = 0 V, I_D = -10 µA	-70	-40		-30		V
Source-Drain Breakdown Voltage	$V_{(BR)SDS}$	V_{GD} = V_{BD} = 0 V, I_S = -10 µA	-70	-40		-30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -10 µA	-2.5	-2	-5	-2	-5	V
Gate-Source Voltage	V_{GS}	V_{DS} = -15 V, I_D = -0.5 mA	-3.5	-3	-6.5	-2.5	-6.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 40 V	< -1		-10			pA
		T_A = 125°C[d]	-1					
		V_{DS} = 0 V, V_{GS} = 30 V	< -1				-10	pA
		T_A = 125°C[d]	-1					
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -15 V, V_{GS} = 0 V	-8		-200		-400	pA
		T_A = 125°C[d]	-20					nA
Zero-Gate Voltage Source Current	I_{SDS}	V_{GD} = V_{BD} = 0 V, V_{SD} = -20 V	-10		-400		-800	pA
		T_A = 125°C[d]	-25					nA
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -15 V, V_{GS} = -10 V	-10	-5	-30	-3	-30	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = -20 V, I_D = -100 µA	180		250		300	Ω
		T_A = 125°C[d]	270					
DYNAMIC								
Forward Transconductance[c]	g_{fs}	V_{DS} = -15 V, I_D = -10 mA, f = 1 kHz	2.7	2	4	1	4	mS
Common-Source Output Conductance[c]	g_{os}		150		250		250	µS
Input Capacitance	C_{iss}	V_{DS} = -15 V, I_D = -10 mA, f = 1 MHz	2.4		2.5		2.5	pF
Output Capacitance	C_{oss}		2.5		3		3	pF
Reverse Transfer Capacitance	C_{rss}		0.5		0.7		0.7	pF
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = -15 V, R_L = 1500 Ω	5		12		12	ns
	t_r	I_D = -10 mA, V_{GEN} = -12 V, R_G = 50 Ω	13		24		24	ns
Turn-Off Time	$t_{d(OFF)}$	Switching time is essentially independent of operating temperature.	25		50		50	ns

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
d. Not JEDEC registered

Siliconix incorporated

ND2012L, ND2020L
N-Channel Depletion-Mode MOS Transistors

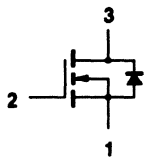
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
ND2012L	200	12	0.16
ND2020L	200	20	0.132

Performance Curves: VDDQ20

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS ND2012L	LIMITS ND2020L	UNITS
Drain-Source Voltage		V_{DS}	200	200	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.16	0.132	A
	T_A = 100°C		0.1	0.083	
Pulsed Drain Current[1]		I_{DM}	0.8	0.8	
Power Dissipation	T_A = 25°C	P_D	0.8	0.8	W
	T_A = 100°C		0.32	0.32	
Operating Junction Temperature Range		T_J	-55 to 150		°C
Storage Temperature Range		T_{stg}	-55 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS ND2012L	LIMITS ND2020L	UNITS
Junction-to-Ambient	R_{thJA}	156	156	K/W

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a]			LIMITS			
				ND2012L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	I_D = 10 µA , V_{GS} = -8 V	220	200		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA	-3	-1.5	-4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C			±50	
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 160 V, V_{GS} = -8 V			1	µA
		T_J = 125°C			200	
Drain-Saturation Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		30		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 20 mA	7			Ω
		V_{GS} = 0 V, I_D = 20 mA			12	
		T_J = 125°C			30	
Forward Transconductance[c]	g_{FS}	V_{DS} = 7.5 V, I_D = 20 mA	55			mS
Common Source Output Conductance[c]	g_{OS}		75			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	35		100	pF
Output Capacitance	C_{oss}		10		20	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 1250 Ω, I_D = 20 mA V_{GEN} = -5 V, R_G = 25 Ω	20			nS
	t_r		20			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	10			
	t_f		10			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

SPECIFICATIONS[a]			LIMITS			
				ND2020L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	I_D = 1 µA, V_{GS} = -5 V	220	200		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA	-1.8	-0.5	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C			±50	
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 160 V, V_{GS} = -5 V			1	µA
		T_J = 125°C			200	
Drain-Saturation Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		30		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 20 mA	7			Ω
		V_{GS} = 0 V, I_D = 20 mA			20	
		T_J = 125°C			50	
Forward Transconductance[c]	g_{FS}	V_{DS} = 7.5 V, I_D = 20 mA	55			mS
Common Source Output Conductance[c]	g_{OS}		75			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	35		100	pF
Output Capacitance	C_{oss}		10		20	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 1250 Ω, I_D = 20 mA V_{GEN} = -5 V, R_G = 25 Ω	20			nS
	t_r		20			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	10			
	t_f		10			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

ND2406L, ND2410L
N-Channel Depletion-Mode MOS Transistors

Siliconix incorporated

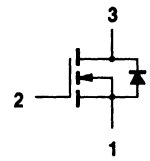
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
ND2406L	240	6	0.23
ND2410L	240	10	0.18

Performance Curves: VDDV24

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS ND2406L	LIMITS ND2410L	UNITS
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.23	0.18	A
	T_A = 100°C		0.14	0.12	
Pulsed Drain Current[1]		I_{DM}	0.9	0.9	
Power Dissipation	T_A = 25°C	P_D	0.8	0.8	W
	T_A = 100°C		0.32	0.32	
Operating Junction Temperature Range		T_J	-55 to 150		°C
Storage Temperature Range		T_{stg}	-55 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS ND2406L	LIMITS ND2410L	UNITS
Junction-to-Ambient	R_{thJA}	156	156	K/W

[1]Pulse width limited by maximum junction temperature

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS			
				ND2406L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	I_D = 10 µA , V_{GS} = -9 V	260	240		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA		-1.5	-4.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C			±50	
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 180 V, V_{GS} = -9 V			1	µA
		T_J = 125°C			200	
Drain-Saturation Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		40		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 30 mA				Ω
		V_{GS} = 0 V, I_D = 30 mA	3		6	
		T_J = 125°C			15	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 30 mA	110			mS
Common Source Output Conductance[c]	g_{OS}		70			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	70		120	pF
Output Capacitance	C_{oss}		20		30	
Reverse Transfer Capacitance	C_{rss}		10		15	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 830 Ω, I_D = 30 mA V_{GEN} = -5 V, R_G = 25 Ω	15			nS
	t_r		75			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	40			
	t_f		100			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

SPECIFICATIONS[a]			LIMITS			
				ND2410L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	I_D = 1 µA , V_{GS} = -5 V	260	240		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA		-0.5	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C			±50	
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 180 V, V_{GS} = -5 V			1	µA
		T_J = 125°C			200	
Drain-Saturation Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	120	40		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 30 mA	4.5			Ω
		V_{GS} = 0 V, I_D = 30 mA	5		10	
		T_J = 125°C	10		25	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 30 mA	110			mS
Common Source Output Conductance[c]	g_{OS}		70			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	70		120	pF
Output Capacitance	C_{oss}		20		30	
Reverse Transfer Capacitance	C_{rss}		10		15	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 830 Ω, I_D = 30 mA V_{GEN} = -5 V, R_G = 25 Ω	15			nS
	t_r		75			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	40			
	t_f		100			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

TD1001Y
Dual N-Channel Enhancement-Mode MOSFETs

PRODUCT SUMMARY

	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
Single MOSFET	30	1.2	0.49

FEATURES

- Electrically Isolated MOSFETs
- Surface Mount
- Low Thermal Resistance

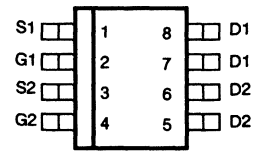
APPLICATIONS

- MOSFET Drivers
- Motor Drivers

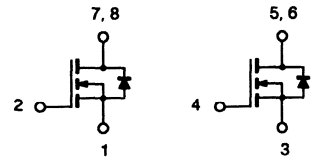
END PRODUCTS

- Disk/Tape Drives
- Printers/Plotters
- Instrumentation

SO-8 PACKAGE



Top View



Performance Curves: VNDQ03

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SINGLE MOSFET	UNITS
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.76	A
	T_A = 100°C		0.48	
Pulsed Drain Current[1]		I_{DM}	2	
Maximum Power Dissipation	T_A = 25°C	P_D	1.3	W
	T_A = 100°C		0.52	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	96	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	60	30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.5	0.8	2	
Gate-Body Lekage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			50	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.6	0.3		A
		V_{DS} = 10 V, V_{GS} = 10 V	2.5	1		
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 0.3 A	2.7		3.5	Ω
		T_J = 125°C	5.4		7	
		V_{GS} = 10 V, I_D = 1 A	1.2		1.5	
		T_J = 125°C	2.5		3	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	300		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz	40		60	pF
Output Capacitance	C_{oss}		30		40	
Reverse Transfer Capacitance	C_{rss}		8		15	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 24 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	10		20	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	15		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

TD1004Y
Dual N-Channel Enhancement-Mode MOSFETs

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	2	0.65

FEATURES

- Electrically Isolated MOSFETs
- Surface Mount
- Low Thermal Resistance

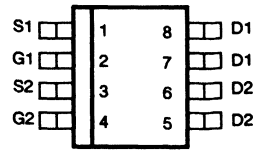
APPLICATIONS

- MOSFET Drivers
- Motor Drivers

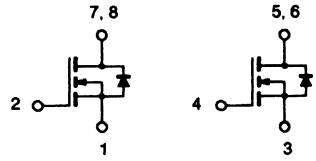
END PRODUCTS

- Disk/Tape Drives
- Printers/Plotters
- Instrumentation

SO-8 PACKAGE



Top View



Performance Curves: VNDQ06

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SINGLE MOSFET	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.55	A
	T_A = 100°C		0.35	
Pulsed Drain Current[1]		I_{DM}	2	
Maximum Power Dissipation	T_A = 25°C	P_D	1.3	W
	T_A = 100°C		0.52	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	62.5	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.5	0.8	2	
Gate-Body Lekage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			50	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.6	0.3		A
		V_{DS} = 10 V, V_{GS} = 10 V	1.5	1.25		
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 0.3 A	2.5		4	Ω
		T_J = 125°C	5		8	
		V_{GS} = 10 V, I_D = 1 A	1.3		2	
		T_J = 125°C	2.6		4	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	38		60	pF
Output Capacitance	C_{oss}		28		40	
Reverse Transfer Capacitance	C_{rss}		8		15	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	9		20	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	10		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

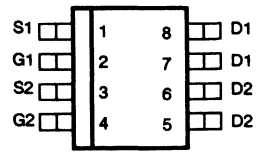
Siliconix incorporated

TD2001Y
Dual P-Channel Enhancement-Mode MOSFETs

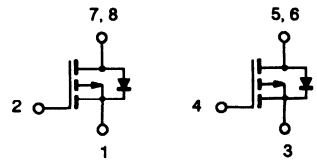
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-30	2	-0.5

SO-8 PACKAGE



Top View



FEATURES

- Electrically Isolated MOSFETs
- Surface Mount
- Low Thermal Resistance

APPLICATIONS

- MOSFET Drivers
- Motor Drivers

END PRODUCTS

- Disk/Tape Drives
- Printers/Plotters
- Instrumentation

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SINGLE MOSFET	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.65	A
	T_A = 100°C		-0.41	
Pulsed Drain Current[1]		I_{DM}	2	
Maximum Power Dissipation	T_A = 25°C	P_D	1.5	W
	T_A = 100°C		0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	83.3	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-55	-30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.6	-0.8	-4.5	
Gate-Body Lekage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V			-10	µA
		T_J = 125°C			-500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-1.5	-1		A
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -200 mA	1.7		2	Ω
		T_J = 125°C	3		4	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	290	200		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -15 V, f = 1 MHz	130		150	pF
Output Capacitance	C_{oss}		75		100	
Reverse Transfer Capacitance	C_{rss}		20		60	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = -25 V, R_L = 23 Ω, I_D = -1 A V_{GEN} = -10 V, R_G = 25 Ω	16		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	13		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

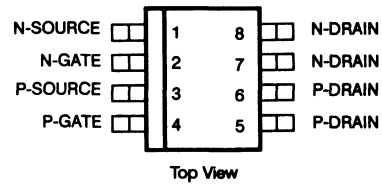
Siliconix incorporated

TD3001Y
N- and P-Channel Half-Bridge MOSFETs

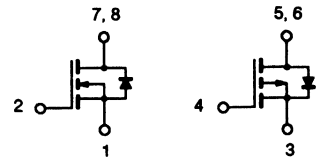
PRODUCT SUMMARY

	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
N-Channel	30	1.5	0.61
P-Channel	-30	2	0.39

SO PACKAGE



Top View



FEATURES

- Electrically Isolated MOSFETs
- Surface Mount
- Low Thermal Resistance

APPLICATIONS

- MOSFET Drivers
- Motor Drivers

END PRODUCTS

- Disk/Tape Drives
- Printers/Plotters
- Instrumentation

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS N-CHANNEL	LIMITS P-CHANNEL	UNITS
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current	T_A = 25°C	I_D	0.61	-0.54	A
	T_A = 100°C		0.39	-0.34	
Pulsed Drain Current[1]		I_{DM}	±2		
Maximum Power Dissipation	T_A = 25°C	P_D	1.2		W
	T_A = 100°C		0.48		
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	104	K/W

[1]Pulse width limited by maximum junction temperature.

6

TD3001Y

Siliconix incorporated

SPECIFICATIONS[a]			N-CHANNEL LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA		30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.5	0.8	2.0	
Gate-Body Lekage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1.0	µA
		T_J = 125°C			50	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.6	0.30		mA
		V_{DS} = 10 V, V_{GS} = 10 V	2.5	1		
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 0.3 A	2.7		3.5	Ω
		T_J = 125°C	5.4		7	
		V_{GS} = 10 V, I_D = 1 A	0.90		1.5	
		T_J = 125°C	2.0		3.0	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	300		mS
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz	40		60	pF
Output Capacitance	C_{oss}		30		40	
Reverse Transfer Capacitance	C_{rss}		8		15	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 24 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	10		20	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	15		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

SPECIFICATIONS[a]			P-CHANNEL LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA		-30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA		-1	-4	
Gate-Body Lekage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-50	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = -10 V	-1.5	-0.80		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -200 m A			2	Ω
		T_J = 125°C			7	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	290	200		mS
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = -15 V, f = 1 MHz	130		150	pF
Output Capacitance	C_{oss}		75		100	
Reverse Transfer Capacitance	C_{rss}		20		60	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = -25 V, R_L = 24 Ω, I_D = -1 A, V_{GEN} = -10 V, R_G = 25 Ω	16		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	13		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

6

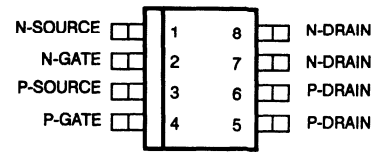
TD3002Y
N- and P-Channel Half-Bridge MOSFETs

Siliconix incorporated

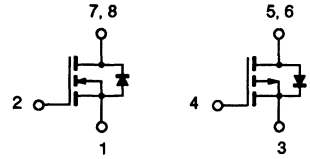
PRODUCT SUMMARY

	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
N-Channel	60	5	0.41
P-Channel	-60	10	0.29

SO PACKAGE



Top View



FEATURES

- Electrically Isolated MOSFETs
- Surface Mount
- Low Thermal Resistance

APPLICATIONS

- MOSFET Drivers
- Motor Drivers

END PRODUCTS

- Disk/Tape Drives
- Printers/Plotters
- Instrumentation

Performance Curves: N-Channel - VNDS06
P-Channel - VPDS06

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS N-CHANNEL	LIMITS P-CHANNEL	UNITS
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current	T_A = 25°C	I_D	0.36	-0.24	A
	T_A = 100°C		0.22	-0.15	
Pulsed Drain Current[1]		I_{DM}	±0.75		
Maximum Power Dissipation	T_A = 25°C	P_D	1.2		W
	T_A = 100°C		0.38		
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	104	K/W

[1]Pulse width limited by maximum junction temperature.

SPECIFICATIONS[a]			N-CHANNEL LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.5	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			200	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	500	200		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 50 mA	4		7.5	Ω
		V_{GS} = 10 V, I_D = 0.2 A	2.3		5	
		T_J = 125°C	4.6		10	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A	170	100		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	16		25	pF
Output Capacitance	C_{oss}		11		20	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 15 Ω, I_D = 0.25 A V_{GEN} = 10 V, R_G = 25 Ω	10		20	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	10		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

6

SPECIFICATIONS[a]			P-CHANNEL LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-1.5	-0.8	-2.5	
Gate-Body Lekage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-200	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-300	-200		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -50 mA	10		15	Ω
		V_{GS} = -10 V, I_D = -0.2 A	7		10	
		T_J = 125°C	14		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.2 A	110	50		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz	15		25	pF
Output Capacitance	C_{oss}		10		20	
Reverse Transfer Capacitance	C_{rss}		3		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A V_{GEN} = -10 V, R_G = 25 Ω	16		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	15		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

TN0201L, TN0401L
N-Channel Enhancement-Mode MOS Transistors

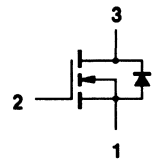
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TN0201L	20	1.2	0.64
TN0401L	40	1.2	0.64

Performance Curves: VNDQ03

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TN0201L	LIMITS TN0401L	UNITS
Drain-Source Voltage		V_{DS}	20	40	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	±0.64	±0.64	A
	T_A = 100°C		±0.38	±0.38	
Pulsed Drain Current[1]		I_{DM}	±1.5	±1.5	
Maximum Power Dissipation	T_A = 25°C	P_D	0.8	0.8	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	TN0201L	40	20		V
		I_D = 10 µA	TN0401L	50	40		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.7	0.5	2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x rated $V_{(BR)DSS}$, V_{GS} = 0 V				1	µA
			T_J = 125°C			100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V		0.8	0.25		A
		V_{DS} = 10 V, V_{GS} = 10 V		1.5	1.0		
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 50 mA		2.5		4	Ω
		V_{GS} = 4.5 V, I_D = 250 mA		1.4		2.0	
			T_J = 125°C	2.8		4.0	
		V_{GS} = 10 V, I_D = 1 A		0.85		1.2	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A		500	200		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		40		60	pF
Output Capacitance	C_{oss}			35		50	
Reverse Transfer Capacitance	C_{rss}			10		15	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω		10		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		15		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

TN0601L
N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

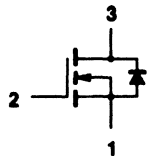
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	1.8	0.47

Performance Curves: VNDQ06

TO-92 (TO-226AA)

BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.47	A
	T_A = 100°C		0.29	
Pulsed Drain Current[1]		I_{DM}	1.5	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	W
	T_A = 100°C		0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, ID = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.7	0.5	2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			100	
On-State Drain Current [c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.5	0.25		A
		V_{DS} = 10 V, V_{GS} = 10 V	1.5	1		
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 250 mA	2		3	Ω
		T_J = 125°C	4		6	
		V_{GS} = 3.5 V, I_D = 40 mA	4		5	
		V_{GS} = 10 V, I_D = 1 A	1.3		1.8	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 500 mA	350	200		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	40		60	pF
Output Capacitance	C_{oss}		30		50	
Reverse Transfer Capacitance	C_{rss}		5		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1.0 A V_{GEN} = 10 V, R_G = 25 Ω	8		15	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9		15	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec. Duty Cycle ≤ 2%.

Siliconix incorporated

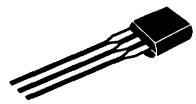
TN1206L
N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

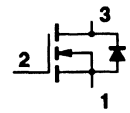
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
120	6	0.18

Performance Curves: See VNDQ12

TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	120	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	±0.18	A
	T_A = 100°C		±0.11	
Pulsed Drain Current[1]		I_{DM}	±1	
Maximum Power Dissipation	T_A = 25°C	P_D	0.8	W
	T_A = 100°C		0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, ID = 100 µA	145	120		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.4	0.5	2.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 96 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current [c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.6	0.2		A
		V_{DS} = 10 V, V_{GS} = 10 V	0.8	0.5		
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 100 mA	4.5		8	Ω
		V_{GS} = 4.5 V, I_D = 2 mA	3.8		6	
		T_J = 125°C	7.6		12	
		V_{GS} = 10 V, I_D = 300 mA	3.3		6	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 200 mA	400	250		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		15		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0. 4 A V_{GEN} = 10 V, R_G = 25 Ω	8		15	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	10		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

TN2010L, TN2410L
N-Channel Enhancement-Mode MOS Transistors

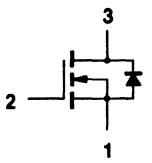
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TN2010L	200	10	0.18
TN2410L	240	10	0.18

Performance Curves: VNDB24

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TN2010L	LIMITS TN2410L	UNITS
Drain-Source Voltage		V_{DS}	200	240	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	±0.18	±0.18	A
	T_A = 100°C		±0.11	±0.11	
Pulsed Drain Current[1]		I_{DM}	±1	±1	
Maximum Power Dissipation	T_A = 25°C	P_D	0.8	0.8	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	TN2410L	260	240		V
		I_D = 100 µA	TN2010L	240	200		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		1.4	0.5	1.8	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V		±1		±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x rated $V_{(BR)DSS}$, V_{GS} = 0 V		0.01		1	µA
			T_J = 125°C	1.0		100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V		0.8	0.25		A
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 50 mA		6		15	Ω
		V_{GS} = 4.5 V, I_D = 200 mA		5		10	
			T_J = 125°C	10		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A		500	100		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		110		135	pF
Output Capacitance	C_{oss}			30		50	
Reverse Transfer Capacitance	C_{rss}			5		20	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0. 4 A V_{GEN} = 10 V, R_G = 25 Ω		15		35	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		30		60	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

TN2460 SERIES
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (mA)	PACKAGE
TN2460L	240	60	76	TO-92
TN2460T	240	60	51	SOT-23

Performance Curves: VNDN24

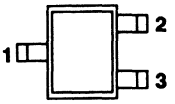
PRODUCT MARKING	
TN2460T	TO3

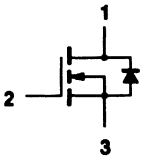
TO-92 (TO-226AA)

BOTTOM VIEW

SOT-23

BOTTOM VIEW





1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TN2460L	LIMITS TN2460T	UNITS
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current[1]	T_A = 25°C	I_D	±76	±51	mA
	T_A = 100°C		±48	±32	
Pulsed Drain Current[1]		I_{DM}	±0.8	±0.40	
Power Dissipation	T_A = 25°C	P_D	0.80	0.36	W
	T_A = 100°C		0.32	0.14	
Operating Junction Temperature		T_J	-55 to 150		°C
Storage Temperature		T_{stg}	-55 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS TN2460L	LIMITS TN2460T	UNITS
Junction-to-Ambient	R_{thJA}	156	350	K/W

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	260	240		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.40	0.5	1.8	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V			0.1	µA
		T_J = 125°C			5.0	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	140	20		mA
		V_{DS} = 10 V, V_{GS} = 10 V	170	75		
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 20 mA	55		60	Ω
		T_J = 125°C	110		120	
		V_{GS} = 10 V, I_D = 50 mA			60	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 50 mA		30		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	15		30	pF
Output Capacitance	C_{oss}		4		15	
Reverse Transfer Capacitance	C_{rss}		1		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 500 Ω, I_D = 50 mA V_{GEN} = 10 V, R_G = 25 Ω	10		20	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	20		35	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 80 µsec, Duty Cycle ≤ 1%.

Siliconix incorporated

TN3512L, TN4012L
N-Channel Enhancement-Mode MOS Transistors

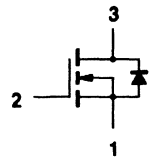
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TN3512L	350	12	0.16
TN4012L	400	12	0.16

Performance Curves: VNDV40

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TN3512L	LIMITS TN4012L	UNITS
Drain-Source Voltage		V_{DS}	350	400	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	±0.16	±0.16	A
	T_A = 100°C		±0.10	±0.10	
Pulsed Drain Current[1]		I_{DM}	±0.65	±0.65	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	0.80	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	TN4012L	420	400		V
		I_D = 10 µA	TN3512L	400	350		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		1.3	0.6	1.8	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V		±1		±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x rated $V_{(BR)DSS}$, V_{GS} = 0 V				1	µA
			T_J = 125°C			100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V		300	150		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 50 mA		10		15	Ω
		V_{GS} = 4.5 V, I_D = 150 mA		9		12	
			T_J = 125°C	17		30	
Forward Transconductance[c]	g_{FS}	V_{DS} = 15 V, I_D = 100 mA		350	125		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		90		110	pF
Output Capacitance	C_{oss}			20		30	
Reverse Transfer Capacitance	C_{rss}			5		10	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 250 Ω, I_D = 0.1 A V_{GEN} = 10 V, R_G = 25 Ω		5.5		15	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		40		60	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

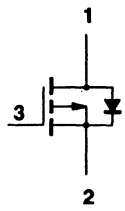
TP0610 SERIES
P-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
TP0610L	-60	10	-0.18	TO-92
TP0610T	-60	10	-0.12	SOT-23

Performance Curves: VPDS06

PRODUCT MARKING	
TP0610T	T50

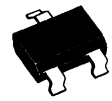


TO-92 (TO-226AA)

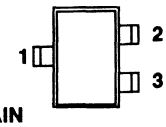
BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

SOT-23



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TP0610L	LIMITS TP0610T	UNITS
Drain-Source Voltage		V_{DS}	-60	-60	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	-0.18	-0.12	A
	T_A = 100°C		-0.11	-0.07	
Pulsed Drain Current[1]		I_{DM}	-0.8	-0.4	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	0.36	W
	T_A = 100°C		0.32	0.14	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS TP0610L	LIMITS TP0610T	UNITS
Junction-to-Ambient	R_{thJA}	156	350	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]			LIMITS			
				TP0610L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.7	-1	-2.4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C			±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-200	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-80	-50		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -25 mA	11		25	Ω
		V_{GS} = -10 V, I_D = -0.5 A	8		10	
		T_J = 125°C	15		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	135	80		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -10 V, I_D = -0.1 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz	15		60	pF
Output Capacitance	C_{oss}		10		25	
Reverse Transfer Capacitance	C_{rss}		3		5	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A V_{GEN} = -10 V, R_G = 25 Ω	6		10	ns
	t_r		10		15	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	7		15	
	t_f		8		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

SPECIFICATIONS[a]			LIMITS			
				TP0610T		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.7	-1	-2.4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C			±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-200	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-80	-50		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -25 mA	11		25	Ω
		V_{GS} = -10 V, I_D = -0.2 A	6		10	
		T_J = 125°C	12		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.1 A	90	60		mS
Common Source Output Conductance[c]	g_{OS}		400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz	15		60	pF
Output Capacitance	C_{oss}		10		25	
Reverse Transfer Capacitance	C_{rss}		3		5	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A V_{GEN} = -10 V, R_G = 25 Ω	6		10	ns
	t_r		10		15	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	7		15	
	t_f		8		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

6

TP1220L, TP2020L
P-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

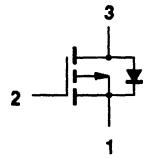
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TP1220L	-120	20	-0.12
TP2020L	-200	20	-0.12

Performance Curves: VPDQ20

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TP1220L	LIMITS TP2020L	UNITS
Drain-Source Voltage		V_{DS}	-120	-200	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.12	-0.12	A
	T_A = 100°C		-0.08	-0.08	
Pulsed Drain Current[1]		I_{DM}	-0.48	-0.48	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	0.80	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	TP1220L	-200	-120		V
		I_D = -10 µA	TP2020L	-220	-200		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA		-1.9	-1	-2.4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±10	nA
			T_J = 125°C			±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V				-1	µA
			T_J = 125°C			-100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V		-250	-50		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -50 mA		15		20	Ω
			T_J = 125°C	30		40	
		V_{GS} = -10 V, I_D = -100 mA		15		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA		100	60		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz		30		60	pF
Output Capacitance	C_{oss}			10		20	
Reverse Transfer Capacitance	C_{rss}			2		10	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = -25 V, R_L = 250 Ω, I_D = -0.1 A V_{GEN} = -10 V, R_G = 25 Ω		15		25	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		35		55	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

6

TP2010L, TP2410L
P-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

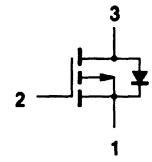
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TP2010L	-200	10	-0.18
TP2410L	-240	10	-0.18

Performance Curves: VPDV24

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TP2010L	LIMITS TP2410L	UNITS
Drain-Source Voltage		V_{DS}	-200	-240	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.18	-0.18	A
	T_A = 100°C		-0.11	-0.11	
Pulsed Drain Current[1]		I_{DM}	-0.72	-0.72	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	0.80	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	TP2010L	-220	-200		V
		I_D = -10 µA	TP2410L	-255	-240		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA		-1.9	-1	-2.4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±10	nA
			T_J = 125°C			±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V				-1	µA
			T_J = 125°C			-100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V		-300	-100		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -100 mA		8.5		10	Ω
			T_J = 125°C	15.5		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA		175	125		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz		90		110	pF
Output Capacitance	C_{oss}			30		50	
Reverse Transfer Capacitance	C_{rss}			10		15	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = -25 V, R_L = 250 Ω, I_D = -100 mA V_{GEN} = -10 V, R_G = 25 Ω		25		45	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		90		130	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

6

TQ1001J
N-Channel Enhancement-Mode MOS Transistor Arrays

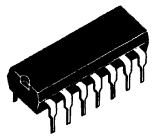
Siliconix incorporated

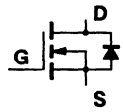
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
30	1.2	0.56

Performance Curves: VNDQ03

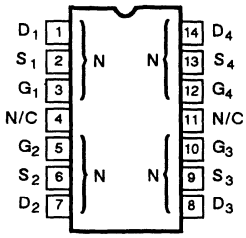
14-PIN PLASTIC





TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current – Single	T_A = 25°C	I_D	0.56	A
	T_A = 100°C		0.36	
Pulsed Drain Current[1]		I_{DM}	1.5	
Maximum Power Dissipation – Single	T_A = 25°C	P_D	1.3	W
	T_A = 100°C		0.52	
Maximum Power Dissipation – Quad	T_A = 25°C		2	
	T_A = 100°C		0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	K/W
Junction-to-Ambient – Quad		62.5	

[1]Pulse width limited by maximum junction temperature.

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	50	30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.4	0.5	2.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C				
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.8	0.25		A
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 40 mA	4.0		5	Ω
		V_{GS} = 4.5 V, I_D = 250 mA	1.6		2.2	
		T_J = 125°C	3.0		4.5	
		V_{GS} = 10 V, I_D = 0.5 A	1.0		1.2	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	200		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz	40		60	pF
Output Capacitance	C_{oss}		35		50	
Reverse Transfer Capacitance	C_{rss}		10		15	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0. 6 A V_{GEN} = 10 V, R_G = 25 Ω	10		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	15		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

6

TQ1004J

N-Channel Enhancement-Mode MOS Transistor Arrays

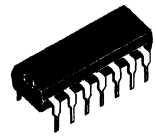
Siliconix incorporated

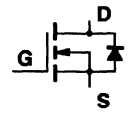
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	2	0.45

Performance Curves: VNDQ06

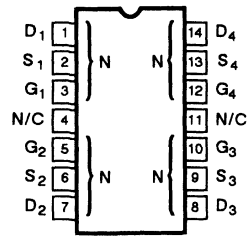
14-PIN PLASTIC





TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current - Single	T_A = 25°C	I_D	0.45	A
	T_A = 100°C		0.28	
Pulsed Drain Current[1]		I_{DM}	1.5	
Maximum Power Dissipation - Single	T_A = 25°C	P_D	1.3	W
	T_A = 100°C		0.52	
Maximum Power Dissipation - Quad	T_A = 25°C		2.0	
	T_A = 100°C		0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	K/W
Junction-to-Ambient - Quad		62.5	

[1]Pulse width limited by maximum junction temperature.

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.7	0.5	2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
		T_J = 125°C	±5		±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			100	
On-State Drain Current [c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	500	250		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 40 mA			5	Ω
		V_{GS} = 4.5 V, I_D = 250 mA	2.4		3	
		T_J = 125°C	4.8		6	
		V_{GS} = 10 V, I_D = 1 A	1.3		2	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	200		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	40		60	pF
Output Capacitance	C_{oss}		30		50	
Reverse Transfer Capacitance	C_{rss}		5		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	8		15	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9		15	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

6

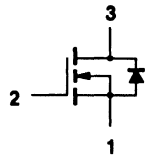
VN46AFD
N-Channel Enhancement-Mode MOS Transistor

Siliconix incorporated

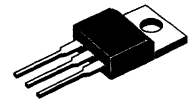
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
40	3	1.46

Performance Curves: VNDQ06

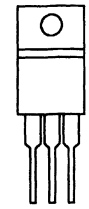


TO-220SD



1 SOURCE
2 GATE
3 & TAB - DRAIN

FRONT VIEW



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_C = 25°C	I_D	1.46	A
	T_C = 100°C		0.92	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	15	W
	T_C = 100°C		6	
Operating Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Case	R_{thJC}	8.3	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	70	40		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			10	µA
		V_{DS} = 32 V, V_{GS} = 0 V, T_C = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3	
		T_C = 125°C	2.6		6	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		25		65	
Reverse Transfer Capacitance	C_{rss}		5		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 32 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		15	nS
Turn-Off Time	t_{OFF}		9.5		15	

NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

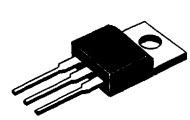
VN66AFD
N-Channel Enhancement-Mode MOS Transistor

Siliconix incorporated

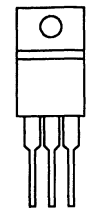
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	3	1.46

TO-220SD

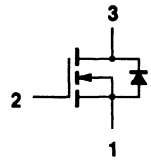


FRONT VIEW



1 SOURCE
2 GATE
3 & TAB - DRAIN

Performance Curves: VNDQ06



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_C = 25°C	I_D	1.46	A
	T_C = 100°C		0.92	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	15	W
	T_C = 100°C		6	
Operating Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Case	R_{thJC}	8.3	K/W

[1]Pulse width limited by maximum junction temperature

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
		T_C = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		T_C = 125°C			10	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3	
		T_C = 125°C	2.6		6	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		15		40	
Reverse Transfer Capacitance	C_{rss}		2		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω	8		15	nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9.5		15	

NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

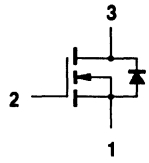
VN88AFD
N-Channel Enhancement-Mode MOS Transistor

Siliconix incorporated

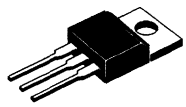
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
80	4	1.29

Performance Curves: VNDQ09

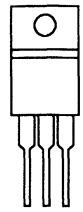


TO-220SD



1 SOURCE
2 GATE
3 & TAB - DRAIN

FRONT VIEW



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_C = 25°C	I_D	1.29	A
	T_C = 100°C		0.81	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	15	W
	T_C = 100°C		6	
Operating Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Case	R_{thJC}	8.3	K/W

[1]Pulse width limited by maximum junction temperature

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	120	80		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.6	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
		T_C = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			10	µA
		V_{DS} = 64 V, V_{GS} = 0 V, T_C = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	4.2		5.6	Ω
		V_{GS} = 10 V, I_D = 1 A	3.6		4	
		T_C = 125°C	6.8		6	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	225			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		15		40	
Reverse Transfer Capacitance	C_{rss}		2		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω	6		15	nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	8		15	

NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

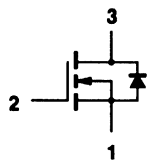
VN0300 SERIES
N-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

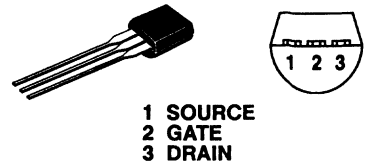
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN0300L	30	1.2	0.64	TO-92
VN0300M	30	1.2	0.67	TO-237

Performance Curves: VNDQ03

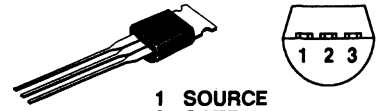


TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW



1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN0300L	LIMITS VN0300M	UNITS
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.64	0.67	A
	T_A = 100°C		0.38	0.43	
Pulsed Drain Current[1]		I_{DM}	3	3	
Power Dissipation	T_A = 25°C	P_D	0.8	1	W
	T_A = 100°C		0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN0300L	LIMITS VN0300M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	65	30		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	3	1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.4		3.3	Ω
		V_{GS} = 5 V, I_D = 1 A	0.85		1.2	
		T_J = 125°C	1.8		2.40	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	200		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	38		100	pF
Output Capacitance	C_{oss}		28		95	
Reverse Transfer Capacitance	C_{rss}		8		25	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 24 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	9		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	13		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

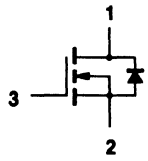
VN0605T
N-Channel Enhancement-Mode MOS Transistor

Siliconix incorporated

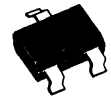
PRODUCT SUMMARY

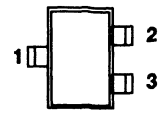
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	5	0.18

Performance Curves: VNDS06



SOT-23 TOP VIEW





1 DRAIN
2 SOURCE
3 GATE

PRODUCT MARKING	
VN0605T	V02

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.18	A
	T_A = 100°C		0.11	
Pulsed Drain Current[1]		I_{DM}	0.72	
Power Dissipation	T_A = 25°C	P_D	0.36	W
	T_A = 100°C		0.14	
Operating Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range		T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	350	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS			
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**TYP[b]**	**MIN**	**MAX**	**UNIT**
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	3.0	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	700	500		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 50 mA	4.5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3		5	
		T_J = 125°C	5.5		10	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A	180	80		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 50 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60	pF
Output Capacitance	C_{oss}		11		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 30 V, R_L = 150 Ω, I_D = 0.2 A V_{GEN} = 10 V, R_G = 25 Ω	7		20	nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	11		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

VN0606M, VN0808M
N-Channel Enhancement-Mode MOS Transistors

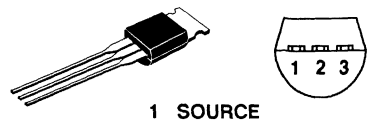
Siliconix incorporated

PRODUCT SUMMARY

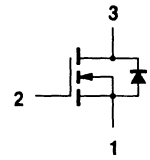
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
VN0606M	60	3	0.39
VN0808M	80	4	0.33

Performance Curves: VNDQ06 . . . . . VN0606M
VNDQ09 . . . . . VN0808M

TO-237 BOTTOM VIEW



1 SOURCE
2 GATE
3 & TAB-DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN0606M	LIMITS VN0808M	UNITS
Drain-Source Voltage		V_{DS}	60	80	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.39	0.33	A
	T_A = 100°C		0.25	0.21	
Pulsed Drain Current[1]		I_{DM}	2.0	1.9	
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.4	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	125	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS					
				VN0606M		VN0808M		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	120	60		80		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.6	0.8	2	0.8	2	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			10		10	µA
		T_J = 125°C			500		500	
On-State Drain Current[d]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	4.2					Ω
		V_{GS} = 10 V, I_D = 0.5 A			3		4	
		T_J = 125°C			6		8	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		170		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	225					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz	35		50		50	pF
Output Capacitance	C_{oss}		15		40		40	
Reverse Transfer Capacitance	C_{rss}		2		10		10	
SWITCHING								
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	6		10		10	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	8		10		10	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.
d. Pulse width limited by maximum junction temperature.

6

VN0610L, VN10KE, VN10KM
N-Channel Enhancement-Mode MOS Transistors, Zener Gate Protected

Siliconix incorporated

PRODUCT SUMMARY

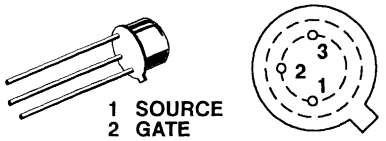
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN0610L	60	5	0.27	TO-92
VN10KE	60	5	0.17	TO-52
VN10KM	60	5	0.31	TO-237

Performance Curves: VNDS06

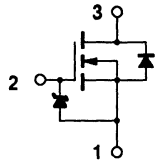
TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-52 (TO-206AC) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE



TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN0610L	LIMITS VN010KE	LIMITS VN10KM	UNITS
Drain-Source Voltage		V_{DS}	60	60	60	V
Gate-Source Voltage[2]		V_{GS}	15/–0.3	15/–0.3	15/–0.3	
Continuous Drain Current	T_A = 25°C	I_D	0.27	0.17	0.31	A
	T_A = 100°C		0.17	0.11	0.20	
Pulsed Drain Current[1]		I_{DM}	1	1	1	
Power Dissipation	T_A = 25°C	P_D	0.8	1.5	1	W
	T_A = 100°C		0.32	0.12	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	–55 to 150			°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300			

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN0610L	LIMITS VN10KE	LIMITS VN10KM	UNITS
Junction-to-Ambient	R_{thJA}	156	400	125	K/W

[1]Pulse width limited by maximum junction temperature
[2]Features internal gate-source Zener diode

VN0610L, VN10KE, VN10KM

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	120	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = 15 V, V_{DS} = 0 V	1		100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V	0.7		10	µA
		T_J = 125°C	3		500	
On-State Drain Current	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	4		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3		5	
		T_J = 125°C	5.6		9	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	300	100		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 50 mA	200			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz	38		60	pF
Output Capacitance	C_{oss}		16		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A V_{GEN} = 10 V, R_G = 25 Ω	7		10	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9		10	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

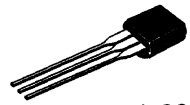
VN0610LL, VN10LM
N-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

PRODUCT SUMMARY

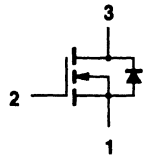
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN0610LL	60	5	0.28	TO-92
VN10LM	60	5	0.32	TO-237

TO-92 (TO-226AA) BOTTOM VIEW

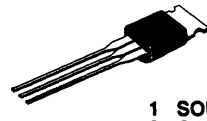


1 SOURCE
2 GATE
3 DRAIN

Performance Curves: VNDS06



TO-237 BOTTOM VIEW



1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN0610LL	LIMITS VN10LM	UNITS
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.28	0.32	A
	T_A = 100°C		0.17	0.2	
Pulsed Drain Current[1]		I_{DM}	1.3	1.4	
Power Dissipation	T_A = 25°C	P_D	0.8	1.0	W
	T_A = 100°C		0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN0610LL	LIMITS VN10LM	UNITS
Junction-to-Ambient	R_{thJA}	156	125	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current[d]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	2.5		5	
		T_J = 125°C	4.4		9	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	230	100		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz	16		60	pF
Output Capacitance	C_{oss}		11		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A V_{GEN} = 10 V, R_G = 25 Ω	7		10	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	7		10	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.
d. Pulse width limited by maximum junction temperature.

6

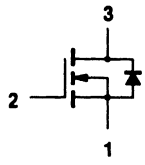
VN1206 SERIES
N-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

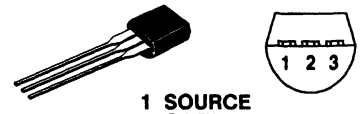
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN1206L	120	6	0.23	TO-92
VN1206M	120	6	0.26	TO-237

Performance Curves: VNDQ12

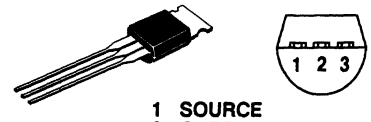


TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW



1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN1206L	LIMITS VN1206M	UNITS
Drain-Source Voltage		V_{DS}	120	120	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.23	0.26	A
	T_A = 100°C		0.15	0.16	
Pulsed Drain Current[1]		I_{DM}	2	2	
Power Dissipation	T_A = 25°C	P_D	0.8	1.0	W
	T_A = 100°C		0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN1206L	LIMITS VN1206M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	145	120		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.6	1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	6		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3.4		6	
		T_J = 125°C	7		14.8	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	425	300		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		125	pF
Output Capacitance	C_{oss}		15		50	
Reverse Transfer Capacitance	C_{rss}		2		20	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω	3		8	ns
	t_r	(Switching time is essentially independent of operating temperature)	2.5		8	
Turn-Off Time	$t_{d(OFF)}$		7		18	
	t_f		2.5		12	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

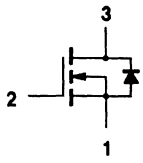
VN1210 SERIES
N-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

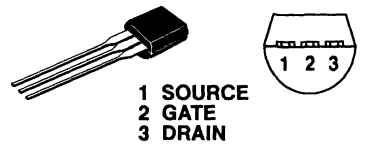
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN1210L	120	10	0.18	TO-92
VN1210M	120	10	0.20	TO-237

Performance Curves: VNDQ12

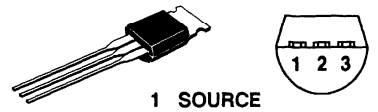


TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW



1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN1210L	LIMITS VN1210M	UNITS
Drain-Source Voltage		V_{DS}	120	120	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.18	0.20	A
	T_A = 100°C		0.11	0.13	
Pulsed Drain Current[1]		I_{DM}	2	2	
Power Dissipation	T_A = 25°C	P_D	0.8	1.0	W
	T_A = 100°C		0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN1210L	LIMITS VN1210M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	145	120		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.0	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.6	1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	6		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3.4		10	
		T_J = 125°C	7		24.7	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	425	300		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz	35		125	pF
Output Capacitance	C_{oss}		15		50	
Reverse Transfer Capacitance	C_{rss}		2		20	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A V_{GEN} = 10 V, R_G = 25 Ω	3		8	ns
	t_r		2.5		8	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	7		18	
	t_f		2.5		12	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

VN2010L
N-Channel Enhancement-Mode MOS Transistor

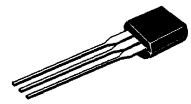
Siliconix incorporated

PRODUCT SUMMARY

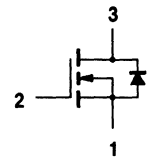
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
200	10	0.19

Performance Curves: VNDQ20

TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.19	A
	T_A = 100°C		0.12	
Pulsed Drain Current[1]		I_{DM}	0.8	
Power Dissipation	T_A = 25°C	P_D	0.8	W
	T_A = 100°C		0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS			
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**TYP[b]**	**MIN**	**MAX**	**UNIT**
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	220	200		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.8	1.8	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	700	100		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 50 mA	7		10	Ω
		T_J = 125°C	12.5		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = 15 V, I_D = 100 mA	180	125		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 15 V, I_D = 50 mA	150			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		60	pF
Output Capacitance	C_{oss}		9		30	
Reverse Transfer Capacitance	C_{rss}		1		15	
SWITCHING[d]						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 250 Ω, I_D = 100 mA V_{GEN} = 10 V, R_G = 25 Ω	5		20	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	21		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.
d. Switching time is essentially independent of operating temperature.

6

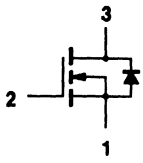
VN2222 SERIES
N-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2222LL	60	7.5	0.23	TO-92
VN2222LM	60	7.5	0.26	TO-237

Performance Curves: VNDS06



TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN2222LL	LIMITS VN2222LM	UNITS
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.23	0.26	A
	T_A = 100°C		0.14	0.16	
Pulsed Drain Current[1]		I_{DM}	1	1	
Power Dissipation	T_A = 25°C	P_D	0.8	1	W
	T_A = 100°C		0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN2222LL	LIMITS VN2222LM	UNITS
Junction-to-Ambient	R_{thJA}	156	125	K/W

[1]Pulse width limited by maximum junction temperature

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.6	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	2.5		7.5	
		T_J = 125°C	4.4		13.5	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	230	100		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 0.2 A	1200			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60	pF
Output Capacitance	C_{oss}		11		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A V_{GEN} = 10 V, R_G = 25 Ω	7		10	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	7		10	

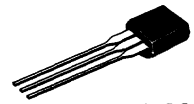
NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

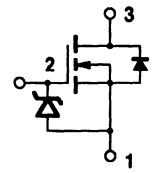
VN2222L
N-Channel Enhancement-Mode MOS Transistor

Siliconix incorporated

TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN



PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	7.5	0.23

Performance Curves: VNDP06

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage[2]		V_{GS}	+15, -0.3	
Continuous Drain Current	T_A = 25°C	I_D	0.23	A
	T_A = 100°C		0.14	
Pulsed Drain Current[1]		I_{DM}	1	
Power Dissipation	T_A = 25°C	P_D	0.8	W
	T_A = 100°C		0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature
[2]Features internal gate-source zener diode

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	120	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.6	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = 15 V, V_{DS} = 0 V			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	4		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3		7.5	
		T_J = 125°C	5.6		13.5	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	300	100		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 50 mA	200			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	38		60	pF
Output Capacitance	C_{oss}		16		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A V_{GEN} = 10 V, R_G = 25 Ω	7		10	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9		10	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

VN2406 SERIES
N-Channel Enhancement-Mode MOS Transistors

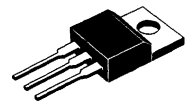
Siliconix incorporated

PRODUCT SUMMARY

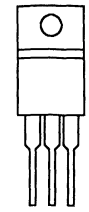
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2406D	240	6	1.12	TO-220
VN2406L	240	6	0.22	TO-92
VN2406M	240	6	0.25	TO-237

Performance Curves: VNDB24

TO-220

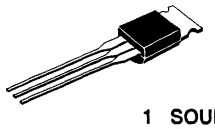


FRONT VIEW



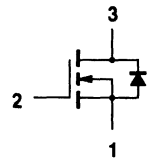
1 GATE
2 & TAB-DRAIN
3 SOURCE

TO-237

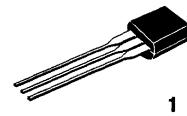


BOTTOM VIEW

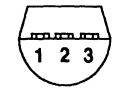
1 SOURCE
2 GATE
3 & TAB-DRAIN



TO-92 (TO-226AA)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN2406D	LIMITS VN2406L	LIMITS VN2406M	UNITS
Drain-Source Voltage		V_{DS}	240	240	240	V
Gate-Source Voltage		V_{GS}	±30	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	1.12	0.17	0.19	A
	T_A = 100°C		0.7	0.11	0.12	
Pulsed Drain Current[1]		I_{DM}	3	1.7	2	
Power Dissipation	T_A = 25°C	P_D	20	0.8	1	W
	T_A = 100°C		8	0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300			

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN2406D	LIMITS VN2406L	LIMITS VN2406M	UNITS
Junction-to-Ambient	R_{thJA}	6.25	156	125	K/W

[1]Pulse width limited by maximum junction temperature

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	270	240		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.0	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.5	1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	7.5		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	5		6	
		T_J = 125°C	10.8		14.8	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530	300		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	110		125	pF
Output Capacitance	C_{oss}		30		50	
Reverse Transfer Capacitance	C_{rss}		5		20	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A V_{GEN} = 10 V, R_G = 25 Ω	3		8	ns
	t_r		2		8	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	13		18	
	t_f		9		12	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

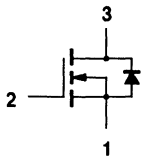
VN2410 SERIES
N-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

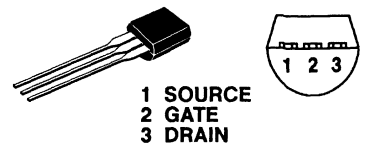
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2410L	240	10	0.17	TO-92
VN2410M	240	10	0.19	TO-237

Performance Curves: VNDB24

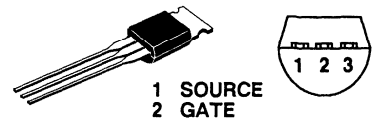


TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW



1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN2410L	LIMITS VN2410M	UNITS
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.17	0.19	A
	T_A = 100°C		0.11	0.12	
Pulsed Drain Current[1]		I_{DM}	1.7	2	
Power Dissipation	T_A = 25°C	P_D	0.8	1.0	W
	T_A = 100°C		0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN2410L	LIMITS VN2410M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS			
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**TYP[b]**	**MIN**	**MAX**	**UNIT**
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	270	240		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.0	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 15 V, V_{GS} = 10 V	1.2	1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	8.5		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	6.5		10	
		T_J = 125°C	14		24.7	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530	300		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	110		125	pF
Output Capacitance	C_{oss}		30		50	
Reverse Transfer Capacitance	C_{rss}		5		20	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A V_{GEN} = 10 V, R_G = 25 Ω	3		8	ns
	t_r		2		8	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	13		23	
	t_f		9		34	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

VN4012L, VN3515L
N-Channel Enhancement-Mode MOS Transistors

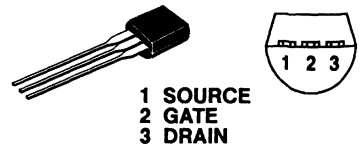
Siliconix incorporated

PRODUCT SUMMARY

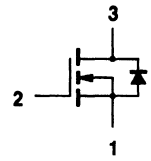
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
VN4012L	400	12	0.16
VN3515L	350	15	0.15

Performance Curves: VNDV40

TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN4012L	LIMITS VN3515L	UNITS
Drain-Source Voltage		V_{DS}	400	350	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.16	0.15	A
	T_A = 100°C		0.10	0.09	
Pulsed Drain Current[1]		I_{DM}	0.65	0.60	
Power Dissipation	T_A = 25°C	P_D	0.80	0.80	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN4012L	LIMITS VN3515L	UNITS
Junction-to-Ambient	R_{thJA}	156	156	K/W

[1]Pulse width limited by maximum junction temperature

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS					
				VN4012L		VN3515L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	420	400		350		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.6	1.8	0.6	1.8	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10		±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			1		1	µA
		T_J = 125°C			100		100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	300	150		150		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 100 mA	9					Ω
		V_{GS} = 4.5 V, I_D = 100 mA	9.5		12		15	
		T_J = 125°C	17		30		35	
Forward Transconductance[c]	g_{FS}	V_{DS} = 15 V, I_D = 100 mA	350	125		125		mS
Common Source Output Conductance[c]	g_{OS}		17					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	80		90		90	pF
Output Capacitance	C_{oss}		10		20		20	
Reverse Transfer Capacitance	C_{rss}		2		5		5	
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 250 Ω, I_D = 0.1 A, V_{GEN} = 10 V, R_G = 25 Ω	3.5		20		20	ns
	t_r		2		20		20	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	25		65		65	
	t_f		15		65		65	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

VN50300 SERIES
N-Channel Enhancement-Mode MOS Transistors

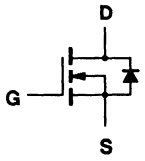
Siliconix incorporated

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN50300L	500	300	0.033	TO-92
VN50300T	500	300	0.022	SOT-23

Performance Curves: VNDO50

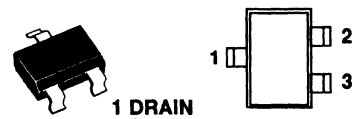
PRODUCT MARKING	
VN50300T	V01



TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

SOT-23 TOP VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VN50300L	LIMITS VN50300T	UNITS
Drain-Source Voltage		V_{DS}	500	500	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.033	0.022	A
	T_A = 100°C		0.021	0.013	
Pulsed Drain Current[1]		I_{DM}	0.13	0.08	
Power Dissipation	T_A = 25°C	P_D	0.8	0.35	W
	T_A = 100°C		0.32	0.14	
Operating Junction Temperature Range		T_J	-55 to 150		°C
Storage Temperature Range		T_{stg}	-55 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VN50300L	LIMITS VN50300T	UNITS
Junction-to-Ambient	R_{thJA}	156	350	K/W

[1]Pulse width limited by maximum junction temperature

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	520	500		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10 µA	3.5	1	4.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V			50	
		T_J = 125°C			5	µA
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	30	15		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 10 mA	250		300	Ω
		V_{GS} = 10 V, I_D = 5 mA	240			
		T_J = 125°C	525		700	
Forward Transconductance[c]	g_{FS}	V_{DS} = 15 V, I_D = 10 mA	14	5		mS
Common Source Output Conductance[c]	g_{OS}		4.5			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	5		20	pF
Output Capacitance	C_{oss}		1.8		10	
Reverse Transfer Capacitance	C_{rss}		0.5		5	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 2500 Ω, I_D = 10 mA V_{GEN} = 10 V, R_G = 25 Ω	4.5		8	nS
	t_r		8		12	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	15		20	
	t_f		60		90	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

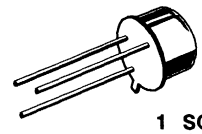
VP0300 SERIES
P-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

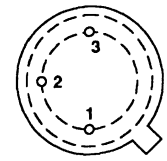
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP0300B	-30	2.5	-1.25	TO-39
VP0300L	-30	2.5	-0.32	TO-92
VP0300M	-30	2.5	-0.5	TO-237

TO-39 (TO-205AD)



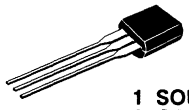
BOTTOM VIEW



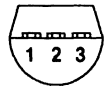
1 SOURCE
2 GATE
3 & CASE-DRAIN

Performance Curves: VPMH03

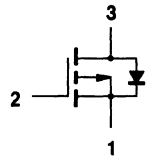
TO-92 (TO-226AA)



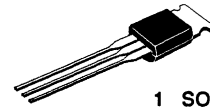
BOTTOM VIEW



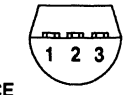
1 SOURCE
2 GATE
3 DRAIN



TO-237



BOTTOM VIEW



1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VP0300B[2]	LIMITS VP0300L	LIMITS VP0300M	UNITS
Drain-Source Voltage		V_{DS}	-30	-30	-30	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	-1.25	-0.32	-0.5	A
	T_A = 100°C		-0.79	-0.2	-0.32	
Pulsed Drain Current[1]		I_{DM}	-3	-2.4	-3	
Power Dissipation	T_A = 25°C	P_D	6.25	0.8	1	W
	T_A = 100°C		2.5	0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300			

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VP0300B[2]	LIMITS VP0300L	LIMITS VP0300M	UNITS
Junction-to-Ambient	R_{thJA}	20	156	125	K/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case temperature for all tests

Rev. A (02/11/91)

SPECIFICATIONS[a]			LIMITS[d]			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	-55	-30		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.6	-2.8	-4.5	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -25 V, V_{GS} = 0 V			-10	µA
		T_J = 125°C			-500	
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -12 V	-1.6	1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -12 V, I_D = -1 A	1.8		2.5	Ω
		T_J = 125°C	3.1		3.63	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	290			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.05 A	800			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	130		150	pF
Output Capacitance	C_{oss}		75		100	
Reverse Transfer Capacitance	C_{rss}		20		60	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = -25 V, R_L = 23 Ω, I_D = -1 A V_{GEN} = -10 V, R_G = 25 Ω	16		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	13		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.
d. Reference case temperature for VP0300B.

6

VP0610 SERIES
P-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP0610L	-60	10	-0.18	TO-92
VP0610T	-60	10	-0.12	SOT-23

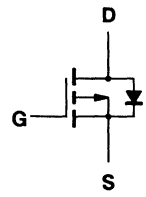
TO-92 (TO-226AA)

BOTTOM VIEW

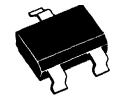
1 SOURCE
2 GATE
3 DRAIN

Performance Curves: VPDS06

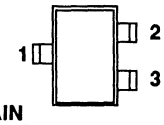
PRODUCT MARKING	
VP0610T	V50



SOT-23



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VP0610L	LIMITS VP0610T	UNITS
Drain-Source Voltage		V_{DS}	-60	-60	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	-0.18	-0.12	A
	T_A = 100°C		-0.11	-0.07	
Pulsed Drain Current[1]		I_{DM}	-0.8	-0.4	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	0.36	W
	T_A = 100°C		0.32	0.14	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VP0610L	LIMITS VP0610T	UNITS
Junction-to-Ambient	R_{thJA}	156	350	K/W

[1]Pulse width limited by maximum junction temperature.

Rev. A (2/11/91)

SPECIFICATIONS[a]			LIMITS			
				VP0610L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-2	-1	-3.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-200	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-700	-600		mA
Drain-Source ON-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -0.5 A	8		10	Ω
		T_J = 125°C	15		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	135	80		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -10 V, I_D = -0.2 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz	15		60	pF
Output Capacitance	C_{oss}		10		25	
Reverse Transfer Capacitance	C_{rss}		3		5	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A V_{GEN} = -10 V, R_G = 25 Ω	6		10	ns
	t_r		10		15	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	7		15	
	t_f		8		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

6

SPECIFICATIONS[a]			LIMITS			
				VP0610T		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-2	-1	-3.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-200	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-300	-220		mA
Drain-Source ON-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -0.2 A	6		10	Ω
		T_J = 125°C	12		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.1 A	90	70		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -10 V, I_D = -0.2 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz	15		60	pF
Output Capacitance	C_{oss}		10		25	
Reverse Transfer Capacitance	C_{rss}		3		5	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A V_{GEN} = -10 V, R_G = 25 Ω	6		10	ns
	t_r		10		15	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	7		15	
	t_f		8		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

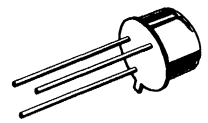
VP0808 SERIES
P-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

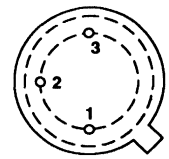
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP0808B	-80	5	-0.88	TO-39
VP0808L	-80	5	-0.28	TO-92
VP0808M	-80	5	-0.31	TO-237

Performance Curves: VPDV10

TO-39 (TO-205AD)

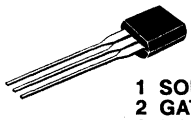


BOTTOM VIEW



1 SOURCE
2 GATE
3 & CASE-DRAIN

TO-92 (TO-226AA)



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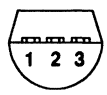
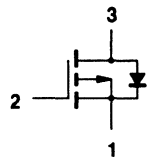
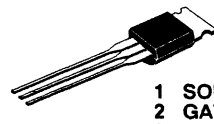


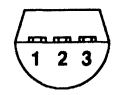
1 SOURCE
2 GATE
3 DRAIN



TO-237



BOTTOM VIEW



1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VP0808B[2]	LIMITS VP0808L	LIMITS VP0808M	UNITS
Drain-Source Voltage		V_{DS}	-80	-80	-80	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	-0.88	-0.28	-0.31	A
	T_A = 100°C		-0.53	-0.17	-0.20	
Pulsed Drain Current[1]		I_{DM}	-3	-3	-3	
Power Dissipation	T_A = 25°C	P_D	6.25	0.8	1	W
	T_A = 100°C		2.5	0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300			

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VP0808B[2]	LIMITS VP0808L	LIMITS VP0808M	UNITS
Junction-to-Ambient	R_{thJA}	20	156	125	K/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case temperature for all tests

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**TYP[b]**	**MIN**	**MAX**	**UNIT**
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -10 µA , V_{GS} = 0 V	-110	-80		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.4	-2	-4.5	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V, V_{GS} = 0 V			-10	µA
		T_J = 125°C			-500	
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -15 V, V_{GS} = -10 V	-2	-1.1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -1 A	2.5		5	Ω
		T_J = 125°C	4.3		8	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	325	200		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.1 A	450			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	75		150	pF
Output Capacitance	C_{oss}		40		60	
Reverse Transfer Capacitance	C_{rss}		18		25	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 47 Ω, I_D = -0.5 A V_{GEN} = -10 V, R_G = 25 Ω	11		15	ns
	t_r		30		40	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	20		30	
	t_f		20		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

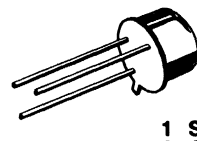
Siliconix incorporated

VP1008 SERIES
P-Channel Enhancement-Mode MOS Transistors

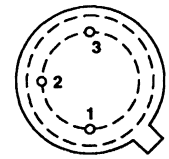
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP1008B	-100	5	-0.79	TO-39
VP1008L	-100	5	-0.28	TO-92
VP1008M	-100	5	-0.31	TO-237

TO-39 (TO-205AD)



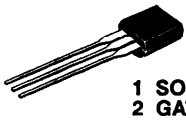
BOTTOM VIEW



1 SOURCE
2 GATE
3 & CASE-DRAIN

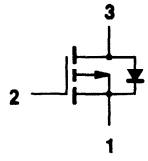
Performance Curves: VPDV10

TO-92 (TO-226AA)

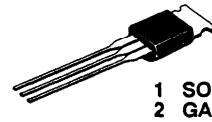


BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



TO-237



BOTTOM VIEW

1 SOURCE
2 GATE
3 & TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VP1008B[2]	LIMITS VP1008L	LIMITS VP1008M	UNITS
Drain-Source Voltage		V_{DS}	-100	-100	-100	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	-0.79	-0.28	-0.31	A
	T_A = 100°C		-0.53	-0.17	-0.20	
Pulsed Drain Current[1]		I_{DM}	-3	-3	-3	
Power Dissipation	T_A = 25°C	P_D	6.25	0.8	1	W
	T_A = 100°C		2.5	0.32	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300			

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS VP1008B[2]	LIMITS VP1008L	LIMITS VP1008M	UNITS
Junction-to-Ambient	R_{thJA}	20	156	125	K/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case temperature for all tests

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -10 µA , V_{GS} = 0 V	-110	-100		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.4	-2	-4.5	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V, V_{GS} = 0 V			-10	µA
		T_J = 125°C			-500	
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -15 V, V_{GS} = -10 V	-2	-1.1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -1 A	2.5		5	Ω
		T_J = 125°C	4.3		8	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	325	200		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.1 A	450			µS
DYNAMIC						
Input Capacitance	C_{lss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	75		150	pF
Output Capacitance	C_{oss}		40		60	
Reverse Transfer Capacitance	C_{rss}		18		25	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 47 Ω, I_D = -0.5 A V_{GEN} = -10 V, R_G = 25 Ω	11		15	ns
	t_r		30		40	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	20		30	
	t_f		20		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

VP2020L
P-Channel Enhancement-Mode MOS Transistor

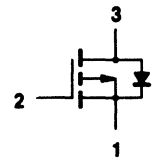
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	20	-0.12

Performance Curves: VPDQ20

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-200	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_A = 25°C	I_D	-0.12	A
	T_A = 100°C		-0.08	
Pulsed Drain Current[1]		I_{DM}	-0.48	
Power Dissipation	T_A = 25°C	P_D	0.80	W
	T_A = 100°C		0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

6

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -10 µA , V_{GS} = 0 V	-220	-200		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.9	-0.8	-2.5	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	nA
		T_J = 125°C			±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -160 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-100	
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-270	-100		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -100 mA	15		20	Ω
		T_J = 125°C	27		40	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA	150	100		mS
Common Source Output Conductance[c]	g_{OS}		300			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	30		70	pF
Output Capacitance	C_{oss}		10		20	
Reverse Transfer Capacitance	C_{rss}		2		10	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 250 Ω, I_D = -100 mA V_{GEN} = -10 V, R_G = 25 Ω	6		10	ns
	t_r		8		15	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	18		30	
	t_f		17		25	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

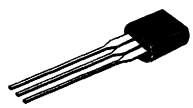
VP2410L
P-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

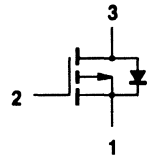
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-240	10	-0.18

Performance Curves: VPDV24

TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-240	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_A = 25°C	I_D	-0.18	A
	T_A = 100°C		-0.11	
Pulsed Drain Current[1]		I_{DM}	-0.72	
Power Dissipation	T_A = 25°C	P_D	0.80	W
	T_A = 100°C		0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

6

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -5 µA , V_{GS} = 0 V	-255	-240		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -2.5 mA	-2.25	-0.8	-2.5	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	nA
		T_J = 125°C			±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -180 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-100	
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-300	-150		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -100 mA	7			Ω
		V_{GS} = -4.5 V, I_D = -150 mA	8.5		10	
		T_J = 125°C	15.5		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA	175	125		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -10 V, I_D = -50 mA	125			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	65		95	pF
Output Capacitance	C_{oss}		20		30	
Reverse Transfer Capacitance	C_{rss}		8		15	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 250 Ω, I_D = -100 mA V_{GEN} = -10 V, R_G = 25 Ω	7		15	ns
	t_r		18		30	
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	45		70	
	t_f		45		60	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

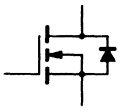
Siliconix incorporated

VQ1000 SERIES
N-Channel Enhancement-Mode MOS Transistor Arrays

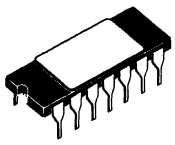
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ1000J	60	5.5	0.225	Plastic
VQ1000P	60	5.5	0.225	Sidebraze

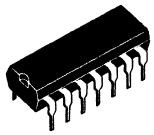
Performance Curves: VNDS06



14-PIN DIP SIDEBRAZE

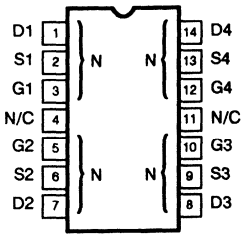


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VQ1000J	LIMITS VQ1000P	UNITS
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current - Single	T_A = 25°C	I_D	0.225	0.225	A
	T_A = 100°C		0.14	0.14	
Pulsed Drain Current[1]		I_{DM}	±1	±1	
Power Dissipation - Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation - Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	K/W
Junction-to-Ambient - Quad		62.5	

[1]Pulse width limited by maximum junction temperature

6

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	500		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.3 A	2.5		5.5	
		T_J = 125°C	4.4		7.6	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	230	100		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60	pF
Output Capacitance	C_{oss}		11		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A V_{GEN} = 10 V, R_G = 25 Ω	7		10	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	7		10	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

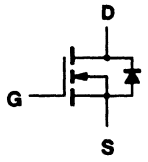
Siliconix incorporated

VQ1001 SERIES
N-Channel Enhancement-Mode MOS Transistor Arrays

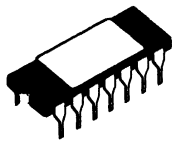
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ1001J	30	1	0.83	Plastic
VQ1001P	30	1	0.83	Sidebraze

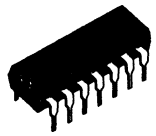
Performance Curves: VNDQ03



14-PIN DIP SIDEBRAZE

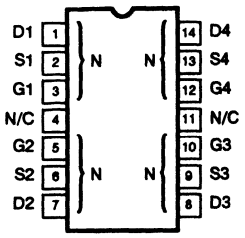


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VQ1001J	LIMITS VQ1001P	UNITS
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current - Single	T_A = 25°C	I_D	0.83	0.83	A
	T_A = 100°C		0.53	0.53	
Pulsed Drain Current[1]		I_{DM}	±3	±3	
Power Dissipation - Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation - Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	K/W
Junction-to-Ambient - Quad		62.5	

[1]Pulse width limited by maximum junction temperature

6

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	65	30		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 12 V	3	2		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	1.4		1.75	Ω
		V_{GS} = 12 V, I_D = 1 A	0.85		1	
		T_J = 125°C	1.65		2	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	200		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	38		110	pF
Output Capacitance	C_{oss}		28		110	
Reverse Transfer Capacitance	C_{rss}		8		35	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A V_{GEN} = 10 V, R_G = 25 Ω	9		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	13		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

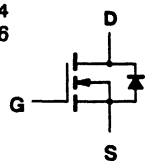
Siliconix incorporated

VQ1004 SERIES
N-Channel Enhancement-Mode MOS Transistor Arrays

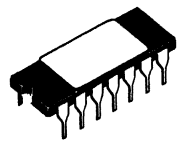
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ1004	60	3.5	0.46	All
VQ1006	90	3.5	0.40	All

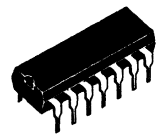
Performance Curves: VNDQ06 .. VQ1004
VNDQ09 .. VQ1006



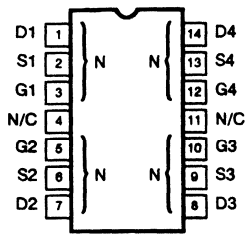
14-PIN DIP SIDEBRAZE



14-PIN PLASTIC



TOP VIEW
Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VQ1004	LIMITS VQ1006	UNITS
Drain-Source Voltage		V_{DS}	60	90	V
Gate-Source Voltage	Plastic	V_{GS}	±30	±30	
	Sidebraze		±20	±20	
Continuous Drain Current - Single	T_A = 25°C	I_D	0.46	0.40	A
	T_A = 100°C		0.26	0.23	
Pulsed Drain Current[1]		I_{DM}	±2	±2	
Power Dissipation - Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation - Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	K/W
Junction-to-Ambient - Quad		62.5	

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a]			LIMITS					
				VQ1004		VQ1006		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	70	60		90		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±15 V, V_{DS} = 0 V			±100		±100	nA
		T_J = 125°C			±500		±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1		1	µA
		T_J = 125°C			500		500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.8		5		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3.5		3.5	
		T_J = 125°C	2.6		4.9		4.9	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		170		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		60		60	pF
Output Capacitance	C_{oss}		25		50		50	
Reverse Transfer Capacitance	C_{rss}		5		10		10	
SWITCHING								
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω	8		10		10	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9		10		10	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

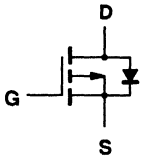
Siliconix incorporated

VQ2001 SERIES
P-Channel Enhancement-Mode MOS Transistor Arrays

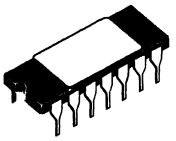
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ2001J	-30	2	-0.6	Plastic
VQ2001P	-30	2	-0.6	Sidebraze

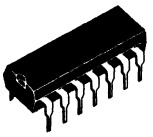
Performance Curves: VPMH03



14-PIN DIP SIDEBRAZE

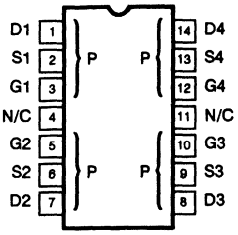


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VQ2001J	LIMITS VQ2001P	UNITS
Drain-Source Voltage		V_{DS}	-30	-30	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.6	-0.6	A
	T_A = 100°C		-0.12	-0.12	
Pulsed Drain Current[1]		I_{DM}	±2	±2	
Power Dissipation - Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation - Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($1/16$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	K/W
Junction-to-Ambient - Quad		62.5	

[1]Pulse width limited by maximum junction temperature

6

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -10 µA, V_{GS} = 0 V	-55	-30		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.6	-2	-4.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V			-10	µA
		V_{DS} = -24 V, V_{GS} = 0 V, T_J = 125°C			-500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -12 V	-1.6	-1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -12 V, I_D = -1 A	1.8		2	Ω
		T_J = 125°C	3.1		3.6	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	290	200		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.05 A	800			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	130		150	pF
Output Capacitance	C_{oss}		75		100	
Reverse Transfer Capacitance	C_{rss}		20		60	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = -15 V, R_L = 23 Ω, I_D = -0.6 A, V_{GEN} = -10 V, R_G = 25 Ω	18		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	13		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

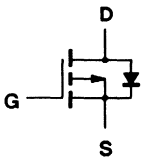
Siliconix incorporated

VQ2004 SERIES
P-Channel Enhancement-Mode MOS Transistor Arrays

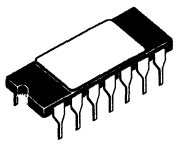
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ2004	-60	5	-0.41	All
VQ2006	-90	5	-0.41	All

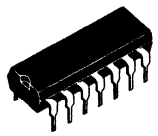
Performance Curves: VPDV10



14-PIN DIP SIDEBRAZE

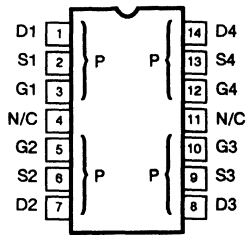


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VQ2004	LIMITS VQ2006	UNITS
Drain-Source Voltage		V_{DS}	-60	-90	V
Gate-Source Voltage	Plastic	V_{GS}	±30	±30	
	Sidebraze		±20	±20	
Continuous Drain Current - Single	T_A = 25°C	I_D	-0.41	-0.41	A
	T_A = 100°C		-0.23	-0.23	
Pulsed Drain Current[1]		I_{DM}	±3	±3	
Power Dissipation - Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation - Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	K/W
Junction-to-Ambient - Quad		62.5	

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a]			LIMITS					
				VQ2004		VQ2006		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -10 µA , V_{GS} = 0 V	-110	60		90		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.4	-2	-4.5	-2	-4.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100		±100	nA
		T_J = 125°C			±500		±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -60 V, V_{GS} = 0 V			-10		-10	µA
		V_{DS} = -24 V, V_{GS} = 0 V, T_J = 125°C			-500		-500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-2	-1		-1		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -1 A	2.5		5		5	Ω
		T_J = 125°C	4.3		8		8	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	325	200		200		mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.1 A	450					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	75		150		150	pF
Output Capacitance	C_{oss}		40		60		60	
Reverse Transfer Capacitance	C_{rss}		18		25		25	
SWITCHING								
Turn-On Time	t_{ON}	V_{DD} = -25 V, R_L = 47 Ω, I_D = -0.5 A, V_{GEN} = -10 V, R_G = 25 Ω	11		15		15	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	20		30		30	

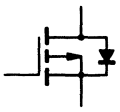
NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

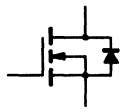
VQ3001 SERIES
N- and P- Channel Enhancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ3001J	30/–30	N = 1 P = 2	N = 0.85 P = 0.6	Plastic
VQ3001P	30/–30	N = 1 P = 2	N = 0.85 P = 0.6	Sidebraze

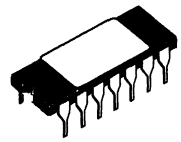


P-Channel

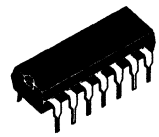


N-Channel

14-PIN DIP SIDEBRAZE

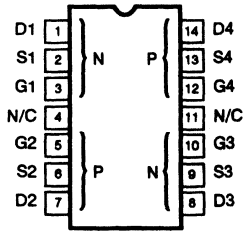


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS VQ3001J N-CH	LIMITS VQ3001J P-CH	LIMITS VQ3001P N-CH	LIMITS VQ3001P P-CH	UNITS
Drain-Source Voltage		V_{DS}	30	–30	30	–30	V
Gate-Source Voltage		V_{GS}	±30	±30	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	±0.85	±0.6	±0.85	±0.6	
	T_A = 100°C		±0.52	±0.37	±0.52	±0.37	A
Pulsed Drain Current[1]		I_{DM}	±3	±2	±3	±2	
Power Dissipation – Single	T_A = 25°C	P_D	1.3	1.3	1.3	1.3	
	T_A = 100°C		0.52	0.52	0.52	0.52	W
Power Dissipation – Quad	T_A = 25°C		2	2	2	2	
	T_A = 100°C		0.8	0.8	0.8	0.8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	–55 to 150				°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	K/W
Junction-to-Ambient – Quad		62.5	

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a] (N-Channel)			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 mA , V_{GS} = 0 V	55	30		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	3.6	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			10	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C			500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 12 V	3	2		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 12 V, I_D = 1 A	1.8		1	Ω
		T_J = 125°C	1.4		1.75	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	360	250		mS
DYNAMIC						
Input Capacitance	C_{lss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	85		110	pF
Output Capacitance	C_{oss}		83		110	
Reverse Transfer Capacitance	C_{rss}		20		35	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω I_D = 0.6 A, V_{GEN} = -0 V, R_G = 25 Ω	10		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	13.5		30	

SPECIFICATIONS[a] (P-Channel)			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -10 mA , V_{GS} = 0 V	-55	-30		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.5	-2	-4.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±100	nA
		T_J = 125°C			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V			-10	µA
		V_{DS} = -24 V, V_{GS} = 0 V, T_J = 125°C			-500	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -12 V	-2	-1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -12 V, I_D = -1 A	1.8		2	Ω
		T_J = 125°C	3.1		3.5	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	280	200		mS
DYNAMIC						
Input Capacitance	C_{lss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	130		150	pF
Output Capacitance	C_{oss}		75		100	
Reverse Transfer Capacitance	C_{rss}		20		60	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = -15 V, R_L = 23 Ω I_D = -0.6 A, V_{GEN} = -10 V, R_G = 25 Ω	18		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	26		30	

NOTES: a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

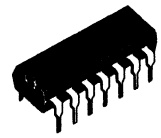
VQ7254J

N- and P- Channel Enhancement-Mode MOS Transistor Array

PRODUCT SUMMARY

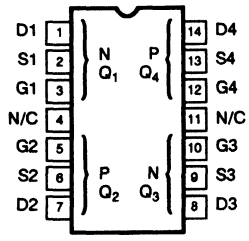
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ $Q_1 + Q_2$ or $Q_3 + Q_4$ (Ω)	I_D (A)
20/-20	3	2

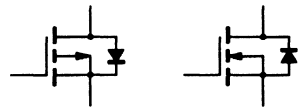
14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package





P-Channel N-Channel

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS N-CHANNEL	LIMITS P-CHANNEL	UNITS
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current		I_D	2	-2	A
Pulsed Drain Current[1]		I_{DM}	±3	±3	
Power Dissipation - Single	T_A = 25°C	P_D	1.75	1.75	W
	T_A = 80°C		1.05	1.05	
Operating Junction Temperature Range		T_J	-40 to 100		°C
Storage Temperature Range		T_{stg}	-40 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		
Thermal Coupling Factor - Single (K) - Q_1 - Q_4 or Q_2 - Q_3			60		%
Thermal Coupling Factor - Single (K) - Q_1 - Q_2 -Q_3 - Q_4, Q_1 - Q_3 or Q_2 - Q_4			50		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	K/W
Junction-to-Ambient - Quad		62.5	

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS[f]	TYP[b]	MIN	MAX	UNIT
STATIC[d]						
Drain-Source On Voltage	$V_{DS(ON)}$	V_{GS} = 11.4 V, I_D = 1 A	2.5	2	3	V
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	$(Q_1 + Q_2)$ or $(Q_3 + Q_4)$	2.5	2	3	Ω

SPECIFICATIONS[a]			LIMITS						
			N-CHANNEL			P-CHANNEL			
PARAMETER	SYMBOL	TEST CONDITIONS[f]	TYP[b]	MIN	MAX	TYP[b]	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	40	20		-55	-20		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8		-3.6	-0.8		
		T_J = 85°C	1.2	0.65		-3.3	-0.65		
Gate-Body Leakage	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V	±1		±100	±1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	0.1		500	-0.1		-500	µA
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8			-1.6			A
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	200		290	200		mS
DYNAMIC									
Input Capacitance	C_{iss}	V_{DS} = 12 V, V_{GS} = 0 V f = 1 MHz	85		175	130		190	pF
Output Capacitance	C_{oss}		80		95	75		100	
Reverse Transfer Capacitance	C_{rss}		18		25	20		60	
SWITCHING[e]									
Turn-On Time	t_{ON}	V_{DD} = 17 V, R_L = 15 Ω I_D = 1.1 A, V_{GEN} = 10 V	12		20	20		30	ns
Turn-Off Time	t_{OFF}	R_G = 25 Ω	14		20	20		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.
d. $r_{DS(ON)}$ and $V_{DS(ON)}$ limits are not specified for individual transistors but are measured as the sum of a n- and p-channel pair.
e. Switching time is essentially independent of operating temperature.
f. Reverse polarity for p-channel devices.

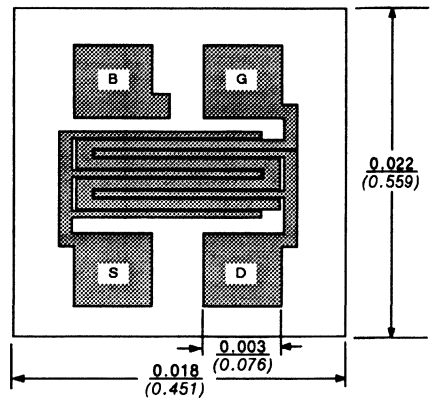
LOW POWER MOS DIE

Siliconix incorporated

MRA1 DIE
P-Channel Enhancement-Mode MOS Transistors

MRA1CHP*
3N163 3N164
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves MRA.



Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Analog and Digital Switching
- General Purpose Amplifiers
- Smoke Detectors

FEATURES

- High Gate Transient Voltage Breakdown Eliminates need for Gate Protective Diode
- Ultra-High Input Impedance
- Normally Off

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±40	
Transient Gate-Source Voltage		±125	
Operating and Storage Temperature	T_J, T_{stg}	-55 to 150	°C

6

MRA1 DIE

Siliconix incorporated

SPECIFICATIONS[1]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{DS} = 0 V, I_D = 10 µA	-70	-40		V
Source-Drain Breakdown Voltage	$V_{(BR)SDS}$	V_{GD} = V_{BD} = 0 V, I_S = -10 µA	-70	-40		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -10 µA	-2.5	-2	-5	V
Gate-Source Voltage	V_{GS}	V_{DS} = -15 V, I_D = -0.5 mA	-3.5	-3	-6.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = -40 V	<-1			pA
		T_J = 125°C	<-1			pA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	-8			pA
Zero-Gate Voltage Source Current	I_{SDS}	V_{GD} = V_{BD} = 0 V, V_{SD} = -20 V	-10			pA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -15 V, V_{GS} = -10 V	-10	-5	-30	mA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = -20 V, I_D = -100 µA	180		250	Ω
DYNAMIC						
Forward Transconductance[3]	g_{fs}	V_{DS} = -15 V, I_D = -10 mA, f = 1 kHz	2.7			mS
Common-Source Output Conductance[3]	g_{os}		150			µS
Input Capacitance	C_{iss}		2.4			pF
Output Capacitance	C_{oss}		2.5			pF
Reverse Transfer Capacitance	C_{rss}		0.5			pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -15 V, R_L = 1500 Ω	5			ns
	t_r	I_D = -10 mA, V_{GEN} = 12 V, R_G = 50 Ω	13			ns
Turn-Off Time	t_{OFF}	Switching time is essentially independent of operating temperature.	25			ns

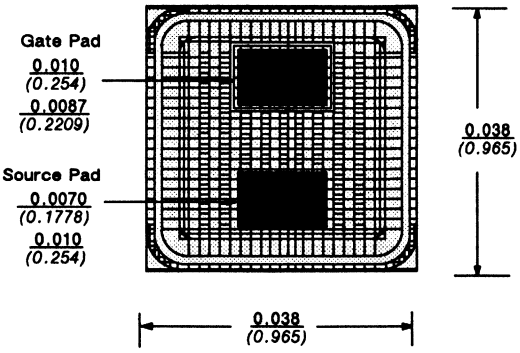
NOTES:
1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

VDDQ SERIES DIE
N-Channel Depletion-Mode MOS Transistors

VDDQ1CHP*	VDDQ2CHP*
ND2012L	ND2020L
*Meets or exceeds specification for all part numbers listed below	

For additional design information please consult the typical performance curves VDDQ20.



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- High Breakdown Voltage > 200 V
- Low $r_{DS(ON)}$ < 10 Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		VDDQ1CHP	VDDQ2CHP	
Drain-Source Voltage	V_{DS}	200	200	V
Gate-Source Voltage	V_{GS}	±30	±20	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150		°C

6

VDDQ SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				VDDQ1CHP		VDDQ2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	I_D = 10 µA , V_{GS} = -8 V	220	200		200		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA		-1.5	-4	-0.5	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1					nA
		T_J = 125°C	±5					
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 160 V, V_{GS} = -8 V	0.2					µA
		T_J = 125°C	5					
Drain-Saturation Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	400					mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 20 mA	9					Ω
		V_{GS} = 0 V, I_D = 20 mA	10		12		20	
		T_J = 125°C	18					
Forward Transconductance[c]	g_{FS}	V_{DS} = 7.5 V, I_D = 20 mA	55					mS
Common Source Output Conductance[c]	g_{OS}		75					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V f = 1 MHz	35					pF
Output Capacitance	C_{oss}		10					
Reverse Transfer Capacitance	C_{rss}		2					
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 1250 Ω I_D = 20 mA V_{GEN} = -5 V	20					nS
	t_r	R_G = 25 Ω	20					
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	10					
	t_f		10					

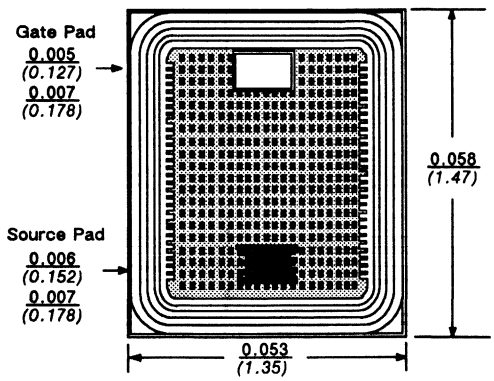
NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

VDDV SERIES DIE
N-Channel Depletion-Mode MOS Transistors

VDDV1CHP*	VDDV2CHP*
ND2406L	ND2410L
*Meets or exceeds specification for all part numbers listed below	

For additional design information please consult the typical performance curves VDDV24.



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- High Breakdown > 240 V
- Low $r_{DS(ON)}$ < 3 Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	240	V
Gate-Source Voltage	V_{GS}	±30	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

6

VDDV SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS					
				VDDV1CHP		VDDV2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	I_D = 10 µA, V_{GS} = -9 V	260	240		240		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA		-1.5	-4.5	-0.5	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1					nA
		T_J = 125°C	±5					
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 180 V, V_{GS} = -9 V	0.04					µA
		T_J = 125°C	15					
Drain-Saturation Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	500					mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 30 mA	3.5		6		10	Ω
		T_J = 125°C	6.4					
Forward Transconductance[c]	g_{FS}	V_{DS} = 7.5 V, I_D = 30 mA	110					mS
Common Source Output Conductance[c]	g_{OS}		70					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V f = 1 MHz	70					pF
Output Capacitance	C_{oss}		20					
Reverse Transfer Capacitance	C_{rss}		10					
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 30 Ω I_D = 30 mA V_{GEN} = -5 V	15					nS
	t_r	R_G = 25 Ω	75					
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	40					
	t_f		100					

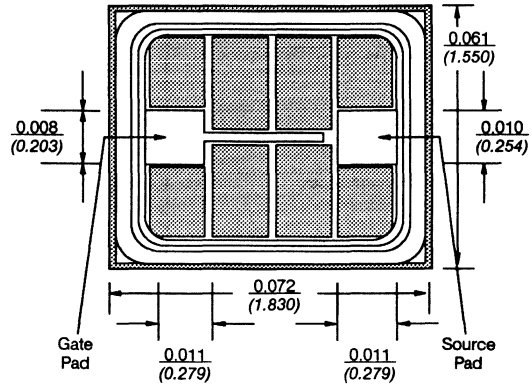
NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

VNDB1 DIE
N-Channel Enhancement-Mode MOS Transistor

VNDB1CHP*
TN2010L TN2410L VN2406D/L/M VN2410L/M
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves VNDB24.



Backside is Drain

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- High Breakdown > 240 V
- Low $r_{DS(ON)}$ < 6 Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	240	V
Gate-Source Voltage	V_{GS}	±30	
Operating and Storage Temperature	T_J, T_{stg}	-55 to 150	°C

6

VNDB1 DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	270	240		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	1.8	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	±1			nA
		T_J = 125°C	±0.5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.01			µA
		T_J = 125°C	1			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	1.5	0.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	7.5		10	Ω
		V_{GS} = 4.5 V, I_D = 200 mA	5		6	
		T_J = 125°C	10.8			
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz	110			pF
Output Capacitance	C_{oss}		30			
Reverse Transfer Capacitance	C_{rss}		5			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A V_{GEN} = 10 V, R_G = 25 Ω	3			ns
	t_r		2			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	13			
	t_f		9			

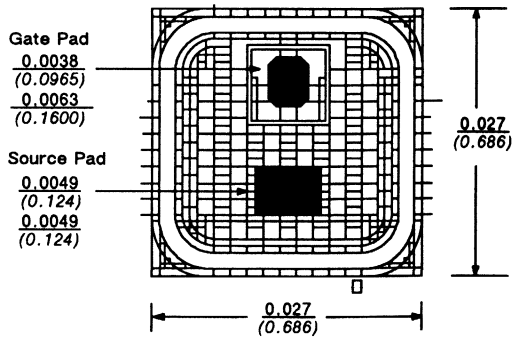
NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

VNDN1 DIE
N-Channel Enhancement-Mode MOS Transistor

VNDN1CHP*
TN2460L TN2460T
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves VNDN24.



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- High Breakdown > 240 V

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±40	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

6

VNDN1 DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	270	240		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA	1.85		2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	±1			nA
		T_C = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.001			µA
		T_C = 125°C	0.5			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 20 V, V_{GS} = 4.5 V	100	50		mA
		V_{GS} = 10 V	170	150		
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 20 mA	40		60	Ω
		T_C = 125°C	80			
		V_{GS} = 10 V, I_D = 50 mA	35		60	
		T_C = 125°C	75			
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 50 mA, f = 1 kHz	50			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 50 mA	10			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	15			pF
Output Capacitance	C_{oss}		4			
Reverse Transfer Capacitance	C_{rss}		1			
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 60 V, R_L = 1.2 kΩ, I_D = 50 mA, V_{GEN} = 10 V, R_G = 25 Ω	7			nS
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	18			

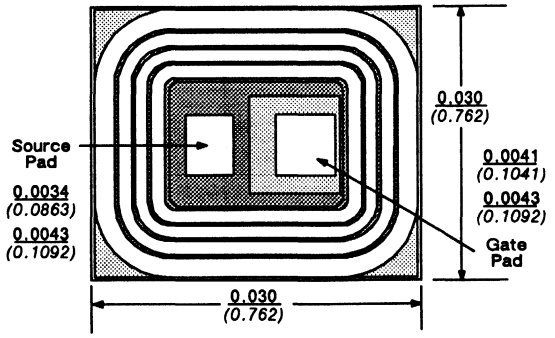
NOTES:
a. T_C = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 80 µS, duty cycle ≤ 1%.

Siliconix incorporated

VNDO1 DIE
N-Channel Enhancement-Mode MOS Transistor

VNDO1CHP*
VN50300L VN50300T
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves VNDO50.



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Switching
- Spike Protection

FEATURES

- High Breakdown 500 V

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	±30	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

6

VNDO1 DIE

Siliconix incorporated

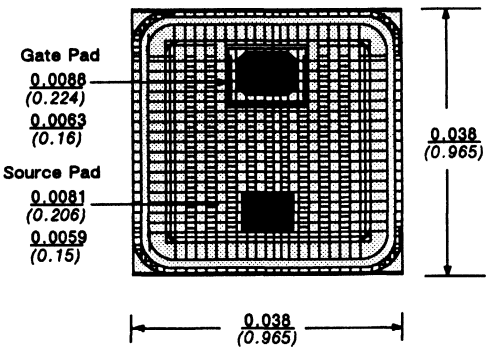
SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA , V_{GS} = 0 V	520	500		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10 µA	3.5	1	4.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V	3			µA
		T_J = 125°C	2			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	30	15		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 10 mA	250		300	Ω
		V_{GS} = 10 V, I_D = 5 mA	240			
		T_J = 125°C	525			
Forward Transconductance[c]	g_{FS}	V_{DS} = 15 V, I_D = 10 mA	14			mS
Common Source Output Conductance[c]	g_{OS}		4.5			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	5			pF
Output Capacitance	C_{oss}		1.8			
Reverse Transfer Capacitance	C_{rss}		0.5			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 2500 Ω, I_D = 10 mA V_{GEN} = 10 V, R_G = 25 Ω	4.5			nS
	t_r		8			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	15			
	t_f		60			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

VNDP1 DIE
N-Channel Enhancement-Mode MOS Transistor

VNDP1CHP*
VN0610L VN10KE VN10KM VN2222L
*Meets or exceeds specification for all part numbers listed below



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

For additional design information please consult the typical performance curves VNDP06.

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- Protection Diode
- Low $r_{DS(ON)} < 5\ \Omega$

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	15/–0.3	
Operating and Storage Temperature	T_J, T_{stg}	–55 to 150	°C

6

VNDP1 DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	120	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = 15 V, V_{DS} = 0 V	1			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V				µA
		T_J = 125°C				
On-State Drain Current	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	4		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3		5	
		T_J = 125°C	5.8			
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	300			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 50 mA	200			µS
DYNAMIC						
Input Capacitance	C_{lss}	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz	35			pF
Output Capacitance	C_{oss}		16			
Reverse Transfer Capacitance	C_{rss}		2			
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A V_{GEN} = 10 V, R_G = 25 Ω	7			ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

VNDQ SERIES DIE
N-Channel Enhancement-Mode MOS Transistors

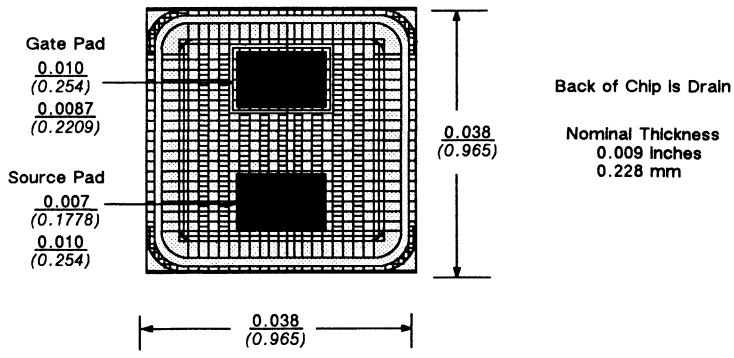
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	DEVICES	PERFORMANCE CURVES
VNDQ1CHP	30	1.2	• TN0201L, TN0401L • VN0300L, VN0300M • VQ1001J/P (VNDQ03 x 4) • TD1001Y (VNDQ03 x 2) • TQ1001J (VNDQ03 x 4)	VNDQ03
VNDQ2CHP	60	1.8	• 2N6659, 2N6660 • TN0601L • VN46AFD, VN66AFD, VN0606M, • TD1004Y (VNDQ06 x 2) • TQ1004J, VQ1004J/P (VNDQ06 x 4)	VNDQ06
VNDQ3CHP	90	4.0	• 2N6661 • VN88AFD, VN0808M • VQ1006J/P (VNDQ09 x 4)	VNDQ09
VNDQ4CHP	120	6.0	• TN1206L • VN1206L/M, VN1210L/M	VNDQ12
VNDQ5CHP	200	10.0	• VN2010L	VNDQ20

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- Low $r_{DS(ON)}$



6

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS					UNITS
		VNDQ1	VNDQ2	VNDQ3	VNDQ4	VNDQ5	
Drain-Source Voltage	V_{DS}	30	60	90	120	200	V
Gate-Source Voltage	V_{GS}	±30	±20	±20	±30	±30	
Operating and Storage Temperature	T_J, T_{stg}	-55 to 150					°C

VNDQ SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
				VNDQ1CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	65	30		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.5	0.8	2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	0.0001			µA
		T_J = 125°C	0.2			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.8	0.25		A
		V_{DS} = 10 V, V_{GS} = 10 V	3	1		
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 50 mA	2.5		4	Ω
		V_{GS} = 4.5 V, I_D = 250 mA	1.4		2	
		V_{GS} = 12 V, I_D = 1 A	0.85		1.2	
		T_J = 125°C	1.8			
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	38			pF
Output Capacitance	C_{oss}		28			
Reverse Transfer Capacitance	C_{rss}		8			
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 24 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	9			ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	13			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

VNDQ SERIES DIE

SPECIFICATIONS[a]			LIMITS			
				VNDQ2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2	
Gate-Body Leakage	I_{GSS}	V_{DS} = ±15 V, V_{GS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	0.05			µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C	0.3			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.5	0.25		A
		V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 40 mA	4		5	Ω
		V_{GS} = 4.5 V, I_D = 250 mA	2		3	
		V_{GS} = 10 V, I_D = 1 A	1.3		1.8	
		T_J = 125°C	2.6			
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Small Signal Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 10 V, I_D = 1 A, f = 1 kHz	1.3		1.8	Ω
Drain-Source Capacitance	C_{OS}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	30			pF
Input Capacitance	C_{iss}		38			
Output Capacitance	C_{oss}		28			
Reverse Transfer Capacitance	C_{rss}		8			
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω	8			ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

VNDQ SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
				VNDQ3CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	120	90		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2	
Gate-Body Leakage	I_{GSS}	V_{DS} = ±15 V, V_{GS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 90 V, V_{GS} = 0 V	0.03			µA
		V_{DS} = 72 V, V_{GS} = 0 V, T_J = 125°C	0.3			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 15 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	4.2		5.3	Ω
		V_{GS} = 10 V, I_D = 1 A	3.6		4	
		T_J = 125°C	6.8			
Drain-Source On-Resistance[c]	$V_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.26			V
		V_{GS} = 10 V, I_D = 1 A	3.6			
		T_J = 125°C	6.8			
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	225			µS
DYNAMIC						
Small Signal Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 10 V, I_D = 1 A, f = 1 kHz	3.8			Ω
Drain-Source Capacitance	C_{OS}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	30			pF
Input Capacitance	C_{iss}		35			
Output Capacitance	C_{oss}		15			
Reverse Transfer Capacitance	C_{rss}		2			
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A V_{GEN} = 10 V, R_G = 25 Ω	6			ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	8			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

VNDQ SERIES DIE

SPECIFICATIONS[a]			LIMITS			
				VNDQ4CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	145	120		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2	
Gate-Body Leakage	I_{GSS}	V_{DS} = ±20 V, V_{GS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.001			µA
		T_J = 125°C	0.5			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.9	0.2		A
		V_{DS} = 10 V, V_{GS} = 10 V	1.8	0.1		
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	8		10	Ω
		V_{GS} = 4.5 V, I_D = 200 mA	3.4		6	
		T_J = 125°C	7			
		V_{GS} = 10 V, I_D = 200 mA	3.3		5	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A	425			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35			pF
Output Capacitance	C_{oss}		15			
Reverse Transfer Capacitance	C_{rss}		2			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω	3			ns
	t_r	(Switching time is essentially independent of operating temperature)	2.5			
Turn-Off Time	$t_{d(OFF)}$		7			
	t_f		2.5			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

VNDQ SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
				VNDQ5CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	220	200		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.8	1.8	
Gate-Body Leakage	I_{GSS}	V_{DS} = ±20 V, V_{GS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V	0.001			µA
		T_J = 125°C	1			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	700	100		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 2.8 V, I_D = 20 mA	8		28	Ω
		V_{GS} = 4.5 V, I_D = 50 mA	7		10	
		T_J = 125°C	12.5			
Forward Transconductance[c]	g_{FS}	V_{DS} = 15 V, I_D = 100 mA	180			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 15 V, I_D = 50 mA	150			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35			pF
Output Capacitance	C_{oss}		9			
Reverse Transfer Capacitance	C_{rss}		1			
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 250 Ω, I_D = 100 mA V_{GEN} = 10 V, R_G = 25 Ω	5			ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	21			

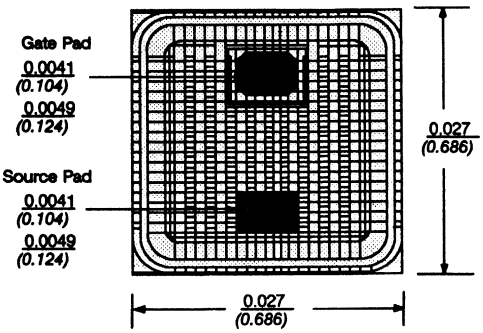
NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

VNDS1 DIE
N-Channel Enhancement-Mode MOS Transistor

VNDS1CHP*
2N7000 2N7002 BS170 VN10LM VN0605T VN0610LL VN2222LL VN2222LM VQ1000J/P (VNDS06 x 4)
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves VNDS06.



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- Low $r_{DS(ON)} < 5\ \Omega$
- Low Cost

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±30	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

6

VNDS1 DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA , V_{GS} = 0 V	70	60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	±1			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V	0.02			µA
		T_J = 125°C	1			
On-State Drain Current[d]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 75 mA	5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.2 A	2.5		5	
		T_J = 125°C	4.4			
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	230			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = 5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz	16			pF
Output Capacitance	C_{oss}		11			
Reverse Transfer Capacitance	C_{rss}		2			
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7			ns
Turn-Off Time	t_{OFF}		7			

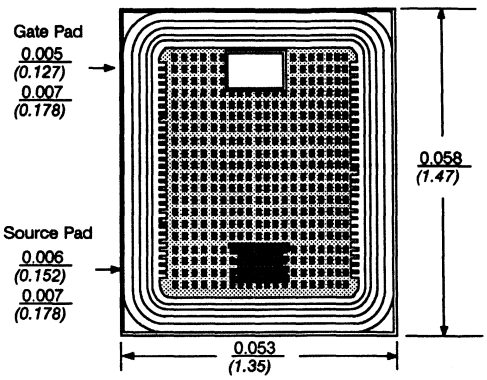
NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.
d. Pulse width limited by maximum junction temperature.

Siliconix incorporated

VNDV1 DIE
N-Channel Enhancement-Mode MOS Transistor

VNDV1CHP*
TN3512L TN4012L VN3515L VN4012L
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves VNDV40.



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- High Breakdown > 400 V
- Low $r_{DS(ON)}$ < 12 Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	±30	
Power Dissipation	T_A = 25°C	P_D	0.80	W
	T_A = 100°C		0.32	
Operating and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

6

VNDV1 DIE

Siliconix incorporated

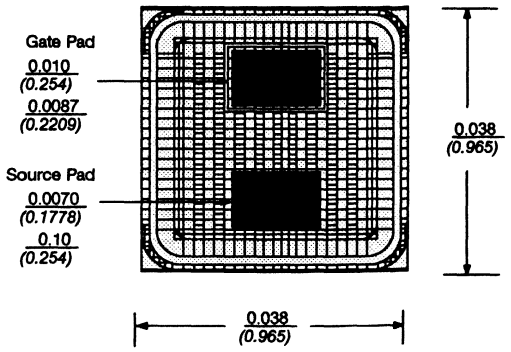
SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	420	400		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.6	1.8	
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V	0.002			µA
		T_J = 125°C	0.8			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	300	150		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 50 mA	9		15	Ω
		V_{GS} = 4.5 V, I_D = 100 mA	9.5		12	
		T_J = 125°C	17			
Forward Transconductance[c]	g_{FS}	V_{DS} = 15 V, I_D = 100 mA	350			mS
Common Source Output Conductance[c]	g_{OS}		17			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	80			pF
Output Capacitance	C_{oss}		10			
Reverse Transfer Capacitance	C_{rss}		2			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 250 Ω, I_D = 0.1 A, V_{GEN} = 10 V, R_G = 25 Ω	3.5			ns
	t_r	(Switching time is essentially independent of operating temperature)	2			
Turn-Off Time	$t_{d(OFF)}$		25			
	t_f		15			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

VPDQ1 DIE
P-Channel Enhancement-Mode MOS Transistor

VPDQ1CHP*
BSS92 TP2020L TP1220L VP2020L
*Meets or exceeds specification for all part numbers listed below



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

For additional design information please consult the typical performance curves VPDQ20.

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- High Breakdown > 200 V
- Low $r_{DS(ON)}$ < 20 Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-200	V
Gate-Source Voltage		V_{GS}	±30	
Power Dissipation	T_A = 25°C	P_D	0.80	W
	T_A = 100°C		0.32	
Operating and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

6

VPDQ1 DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -10 µA , V_{GS} = 0 V	-220	-200		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.9	-1.0	-2.4	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V				nA
		T_J = 125°C				
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V				µA
		T_J = 125°C				
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-270	-100		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -50 mA	15		20	Ω
		T_J = 125°C	27			
		V_{GS} = -10 V, I_D = -100 mA	15		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA	150			mS
Common Source Output Conductance[c]	g_{OS}		300			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	30			pF
Output Capacitance	C_{oss}		10			
Reverse Transfer Capacitance	C_{rss}		2			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 250 Ω, I_D = -100 mA V_{GEN} = -10 V, R_G = 25 Ω	6			ns
	t_r		8			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	18			
	t_f		17			

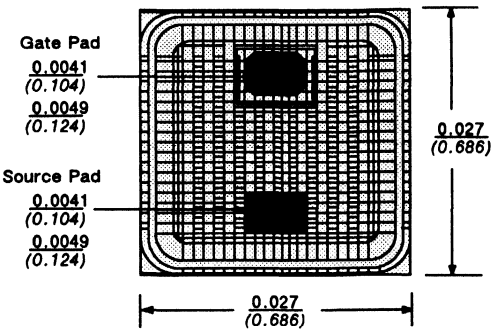
NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

Siliconix incorporated

VPDS1 DIE
P-Channel Enhancement-Mode MOS Transistor

VPDS1CHP*
BS250 TP0610L/T VP0610L/T
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves VPDS06.



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Switching (p-Channel Complement to 2N7000)

FEATURES

- Low $r_{DS(ON)} < 10\ \Omega$

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±30	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	W
	T_A = 100°C		0.32	
Operating and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

6

VPDS1 DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.7	-1	-2.4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V	-0.02			µA
		T_J = 125°C	-0.2			
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-80	-50		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -25 mA	11		25	Ω
		V_{GS} = -10 V, I_D = -0.2 A	6		10	
		T_J = 125°C	12			
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.1 A	90			mS
Common Source Output Conductance[c]	g_{OS}		400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz	15			pF
Output Capacitance	C_{oss}		10			
Reverse Transfer Capacitance	C_{rss}		3			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A V_{GEN} = -10 V, R_G = 25 Ω	6			ns
	t_r		10			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	7			
	t_f		8			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

VPDV SERIES DIE
P-Channel Enhancement-Mode MOS Transistors

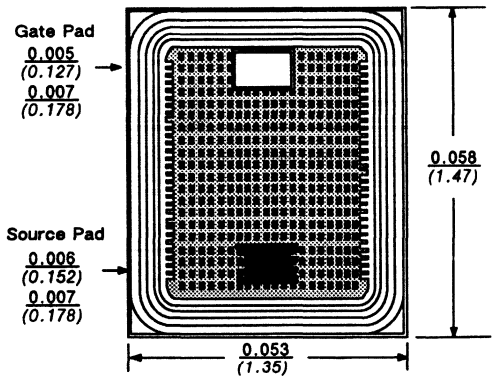
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	DEVICES	PERFORMANCE CURVES
VPDV1CHP	100	5	• VP0808B/L/M • VP1008B/L/M • VQ2004J (VPDV10 x 4) • VQ2006J (VPDV10 x 4)	VPDV10
VPDV2CHP	240	10	• TP2010L • TP2410L • VP2410L	VPDV24

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- Low $r_{DS(ON)}$



Back of Chip is Drain

Nominal Thickness
0.009 inches
0.228 mm

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		VPDV1CHP	VPDV2CHP	
Drain-Source Voltage	V_{DS}	-100	-240	V
Gate-Source Voltage	V_{GS}	±20	±30	
Operating and Storage Temperature	T_J, T_{stg}	-55 to 150		°C

6

VPDV SERIES DIE

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
				VPDV1CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -10 µA , V_{GS} = 0 V	-110	-100		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.4	-2	-4.5	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V, V_{GS} = 0 V	-0.001			µA
		T_J = 125°C	-0.40			
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -15 V, V_{GS} = -12 V	-2	-1.1		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -1 A	2.5		5	Ω
		T_J = 125°C	4.3			
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	325			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.1 A	450			µS
DYNAMIC						
Input Capacitance	C_{lss}	V_{DS} = -25 V, V_{GS} = 0 V f = 1 MHz	75			pF
Output Capacitance	C_{oss}		40			
Reverse Transfer Capacitance	C_{rss}		18			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 47 Ω I_D = -0.5 A, V_{GEN} = -10 V R_G = 25 Ω	11			ns
	t_r		30			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	20			
	t_f		20			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 3%.

SPECIFICATIONS[a]			LIMITS			
				VPDV2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -5 µA , V_{GS} = 0 V	-255	-240		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -2.5 mA	-2.25	-1.0	-2.4	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -180 V, V_{GS} = 0 V	-0.001			µA
		T_J = 125°C	-0.40			
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-300	-150		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -100 mA	7		10	Ω
		V_{GS} = -4.5 V, I_D = -100 mA	8.5		10	
		T_J = 125°C	15.5			
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA	175			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -10 V, I_D = -50 mA	125			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V f = 1 MHz	65			pF
Output Capacitance	C_{oss}		20			
Reverse Transfer Capacitance	C_{rss}		8			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 250 Ω I_D = -100 mA, V_{GEN} = -10 V R_G = 25 Ω	7			ns
	t_r		18			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	45			
	t_f		45			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%.

6

LOW POWER MOS PERFORMANCE CURVES

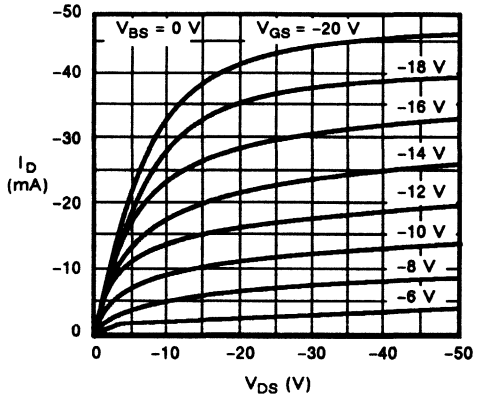
Siliconix incorporated

MRA
P-Channel
Enhancement-Mode MOSFET

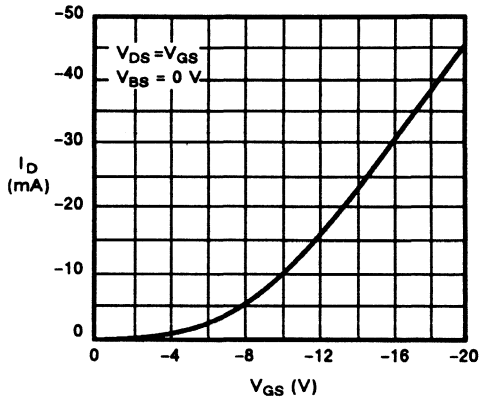
TYPE	PACKAGE	DEVICE
Single	TO-72 (TO-206AF)	• 3N163, 3N164
Single	Chip	• Available as MRA1CHP

TYPICAL CHARACTERISTICS

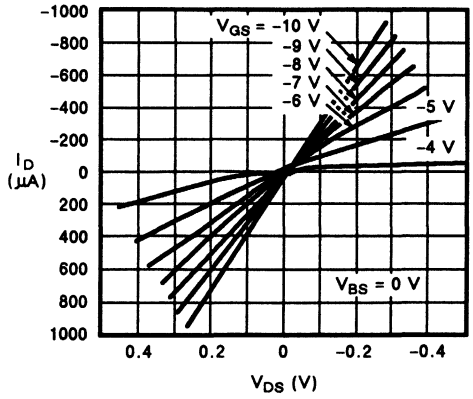
Output Characteristics



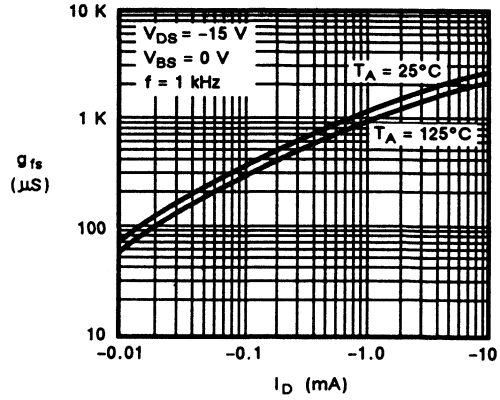
Transfer Characteristics



Low-Level Output Characteristics



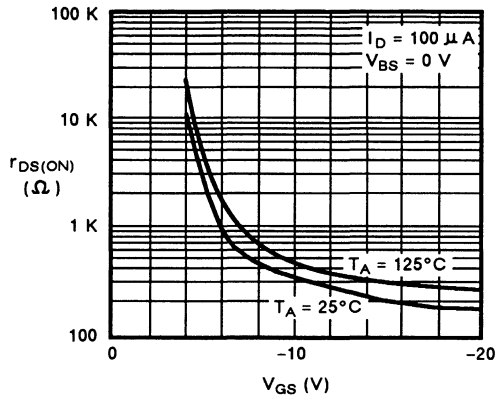
Common-Source Forward Transconductance vs Drain Current



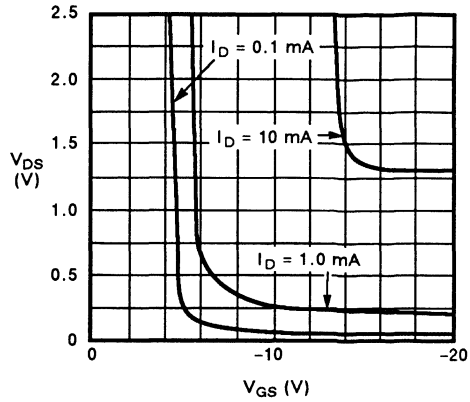
6

TYPICAL CHARACTERISTICS (Cont'd)

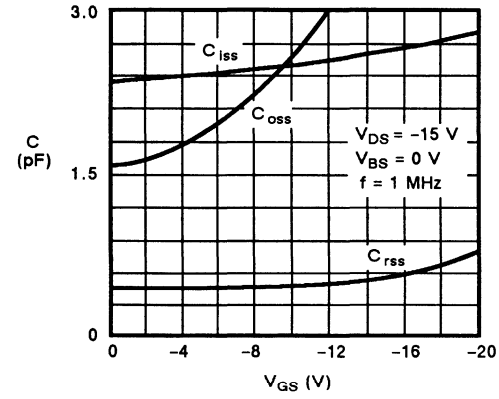
Drain Source On-Resistance vs. Gate-Source Voltage



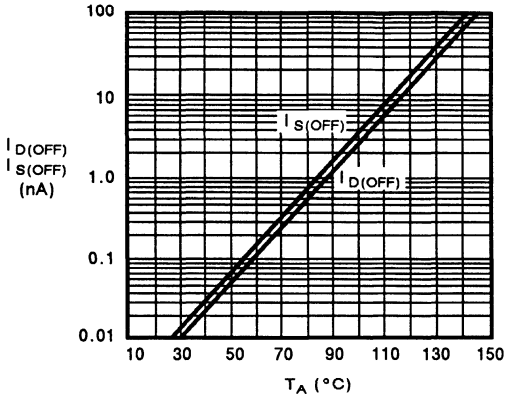
Low-Level Drain-Source ON Voltage vs. Gate-Source Voltage



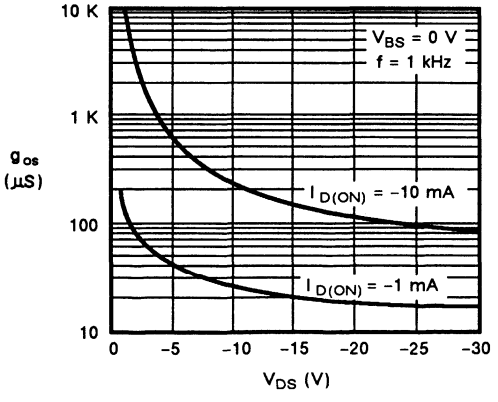
Capacitance vs. Gate-Source Voltage



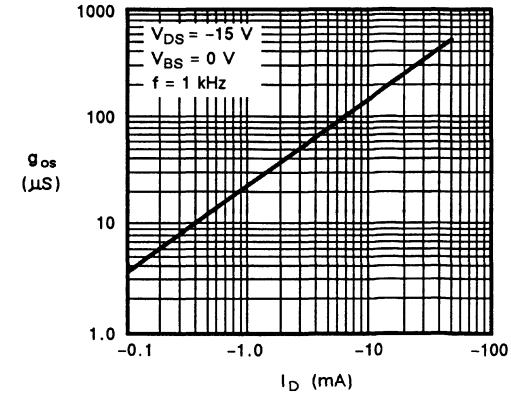
Drain-Source Leakage Current vs. Temperature



Common-Source Output Conductance vs Drain Voltage



Common-Source Output Conductance vs Drain Current



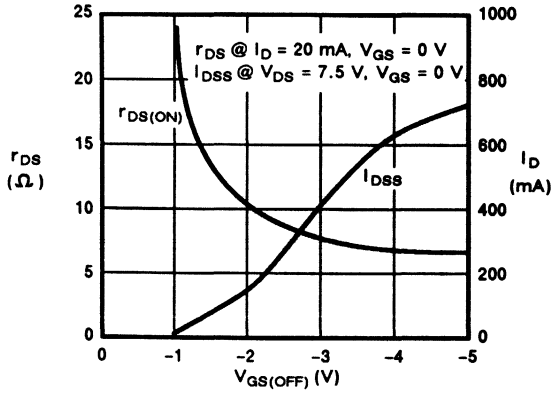
Siliconix incorporated

VDDQ20
N-Channel
Depletion-Mode MOSFET

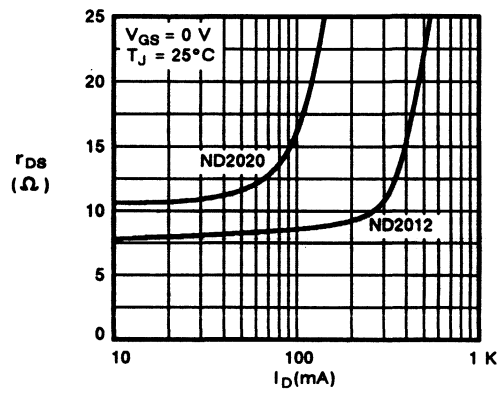
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• ND2012L, ND2020L
Single	Chip	• Available as VDDQ1CHP, VDDQ2CHP

TYPICAL CHARACTERISTICS

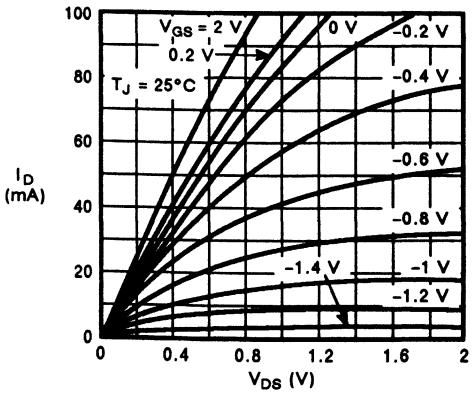
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



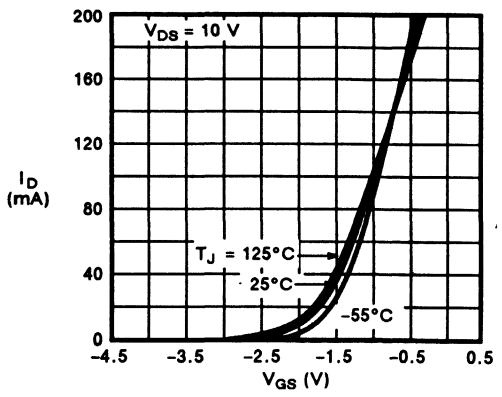
On-Resistance vs. Drain Current



Output Characteristics (ND2020)



Transfer Characteristics (ND2020)



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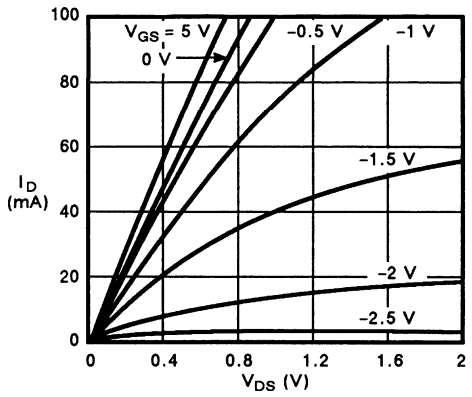
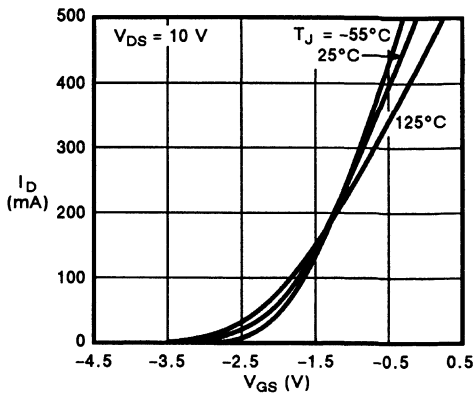
TYPICAL CHARACTERISTICS (Cont'd)

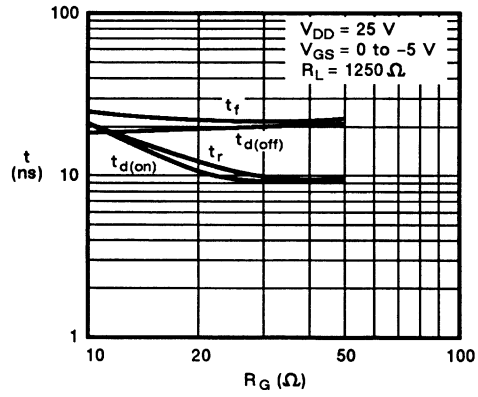
Output Characteristics (ND2012)



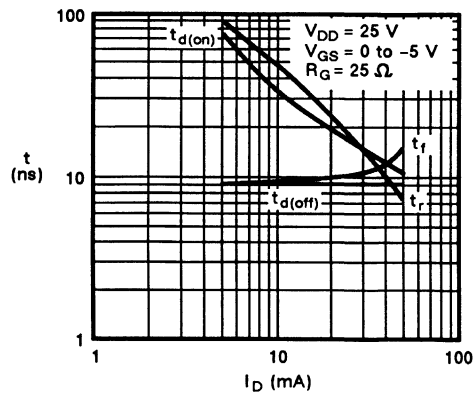
Transfer Characteristics (ND2012)



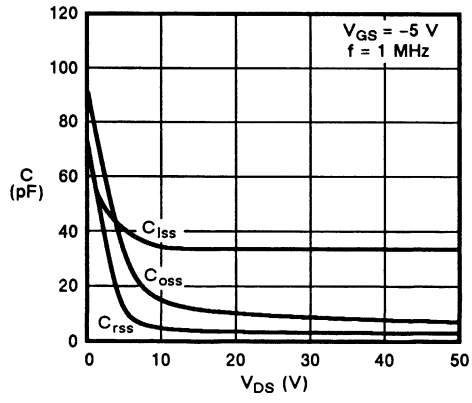
Effects of Drive Resistance



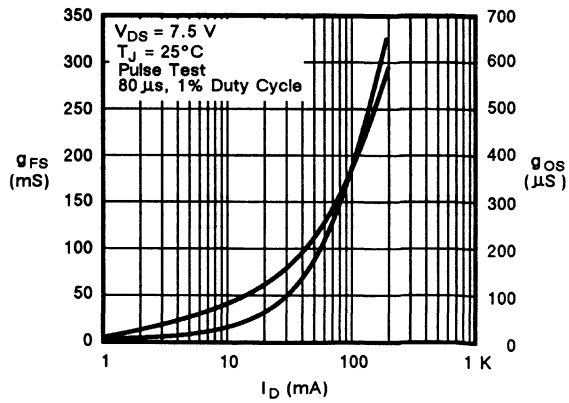
Effects on Load Conditions



Capacitance

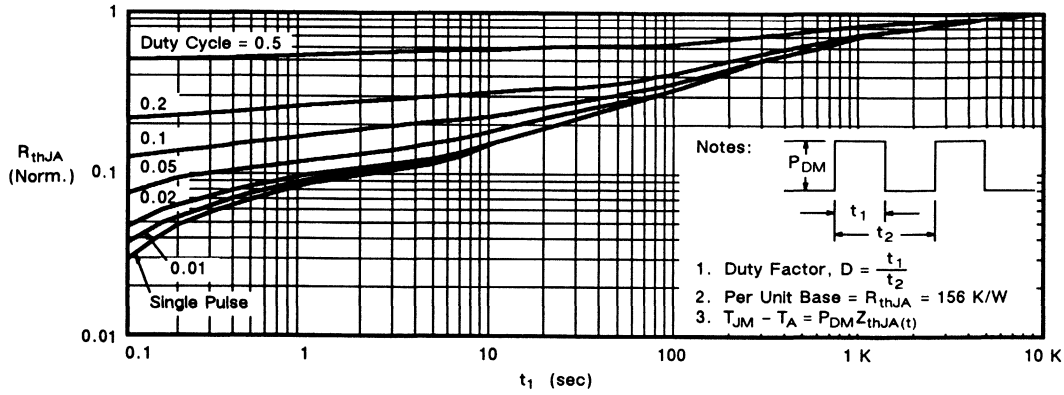


Forward Transconductance vs. Drain Current

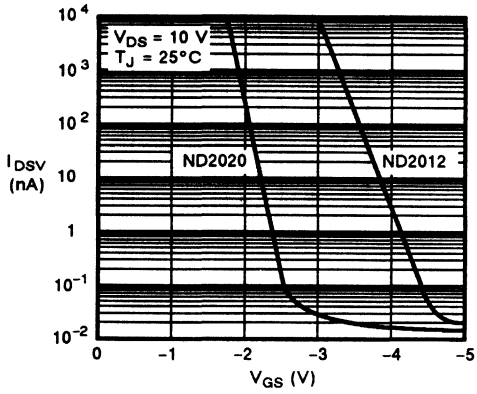


TYPICAL CHARACTERISTICS (Cont'd)

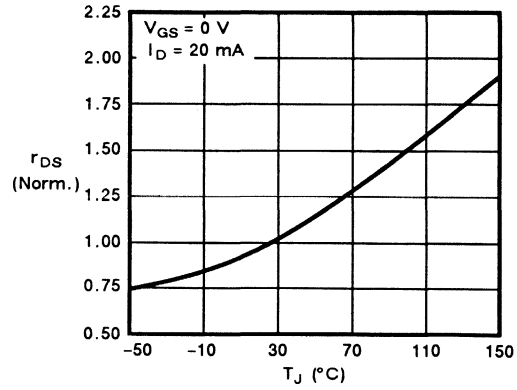
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



Body-Drain Leakage Current



Normalized On-Resistance vs. Junction Temperature



6

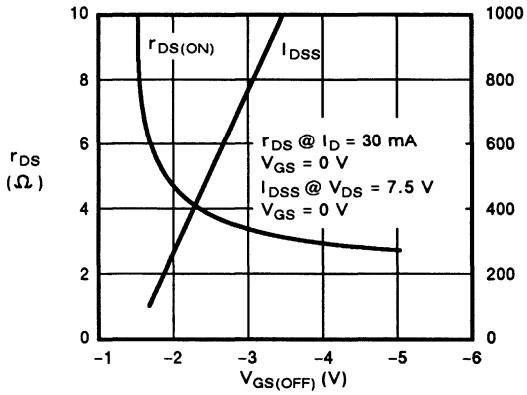
VDDV24
N-Channel
Depletion-Mode MOSFET

Siliconix incorporated

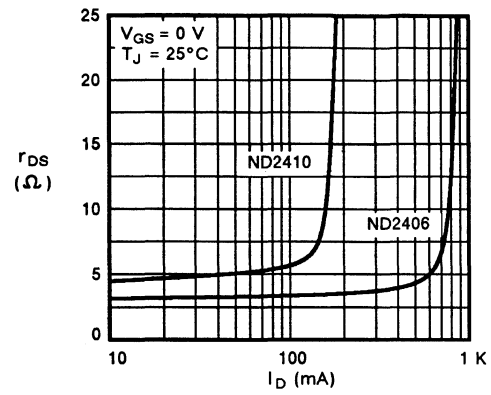
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• ND2406L, ND2410L
Single	Chip	• Available as VDDV1CHP, VDDV2CHP

TYPICAL CHARACTERISTICS

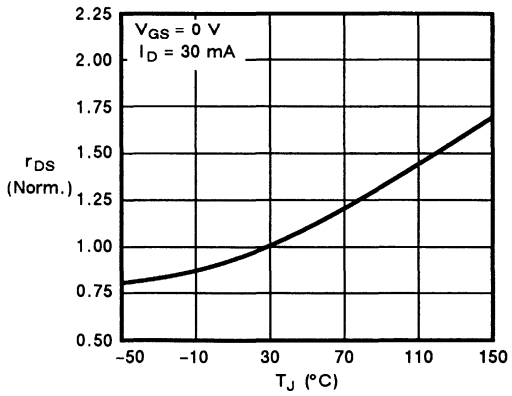
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



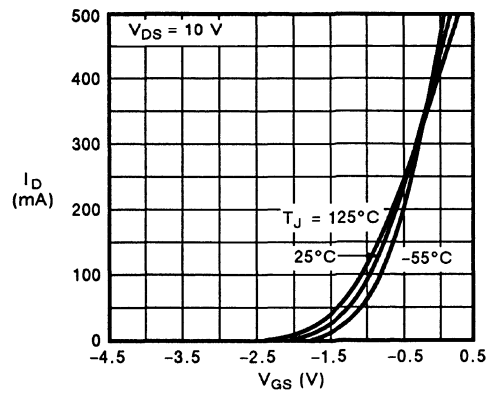
On-Resistance vs. Drain Current



Normalized On-Resistance vs. Junction Temperature



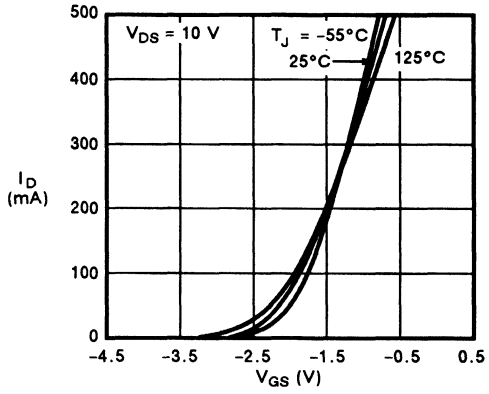
Transfer Characteristics (ND2410)



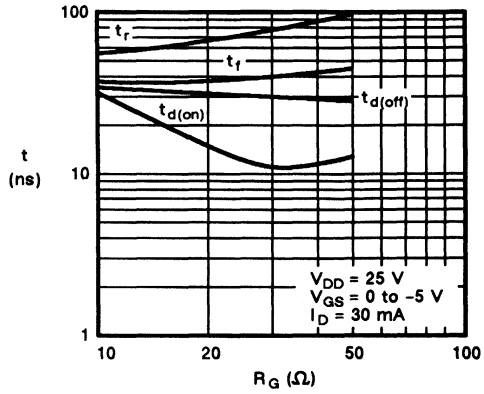
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

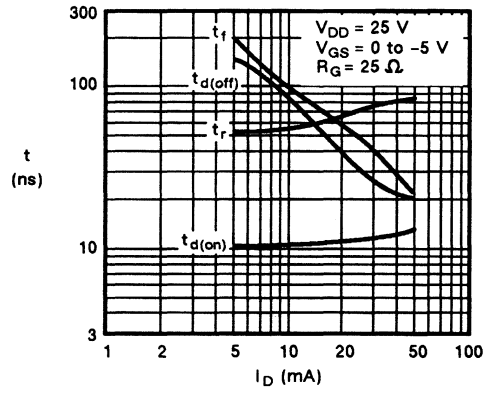
Transfer Characteristics (ND2406)



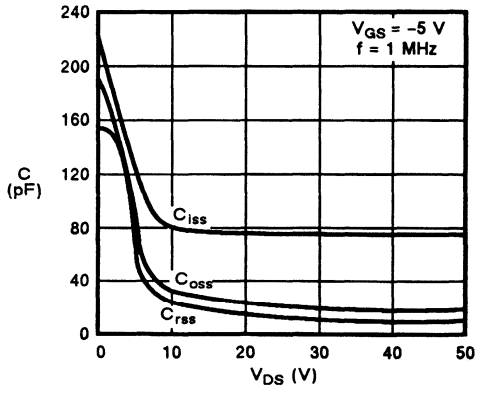
Effects of Drive Resistance



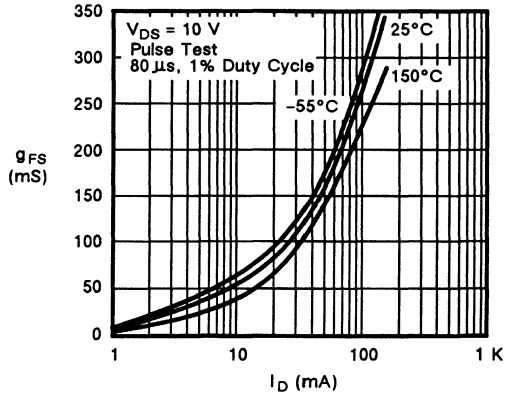
Effects on Load Conditions



Capacitance



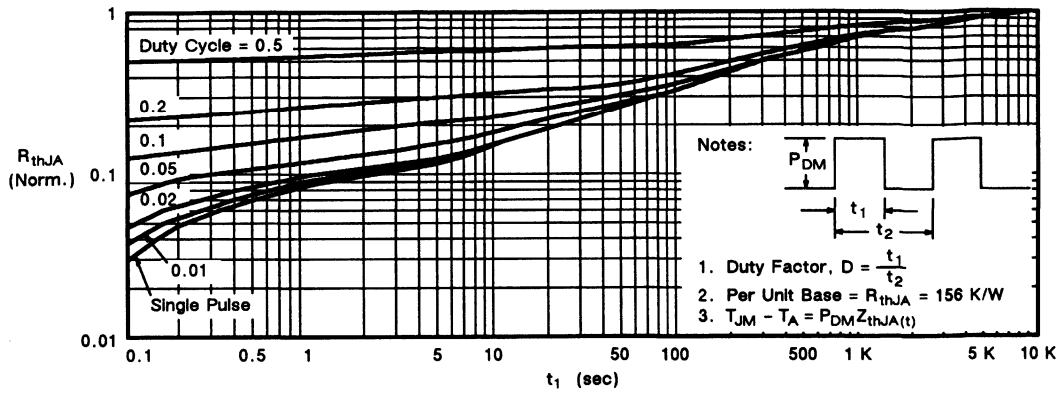
Transconductance



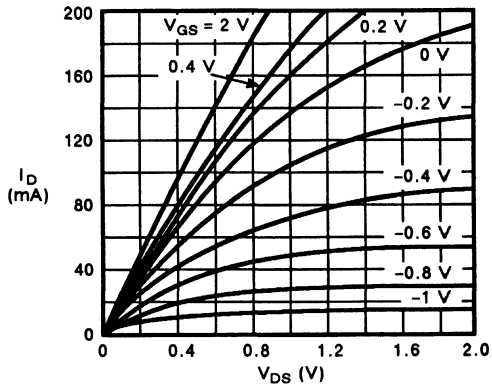
6

TYPICAL CHARACTERISTICS (Cont'd)

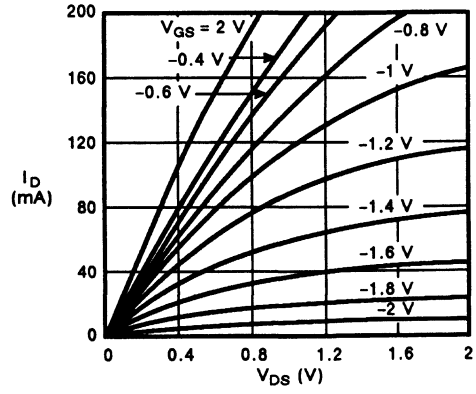
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



Output Characteristics (ND2410)



Output Characteristics (ND2406)



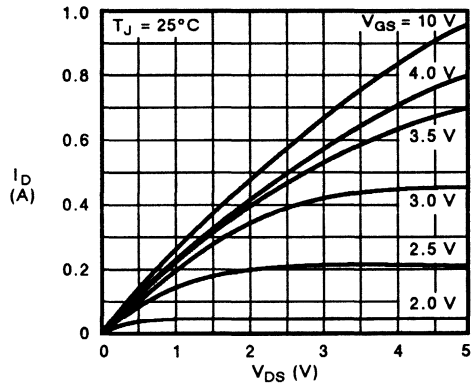
Siliconix incorporated

VNDB24
N-Channel
Enhancement-Mode MOSFET

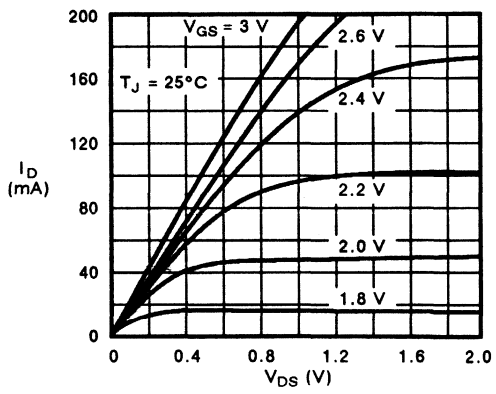
TYPE	PACKAGE	DEVICE
Single	TO-220	• VN2406D
Single	TO-92 (TO-226AA)	• VN2406L, TN2010L, TN2410L
Single	TO-237	• VN2406M
Single	Chip	• Available as VNDB1CHP

TYPICAL CHARACTERISTICS

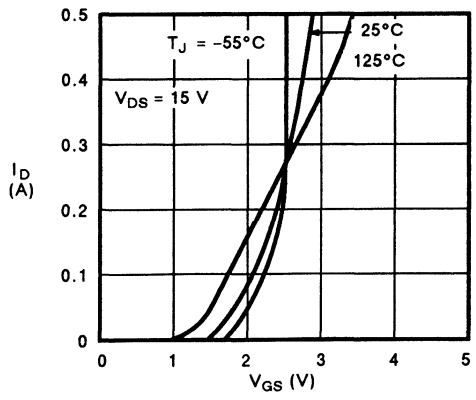
Ohmic Region Characteristics



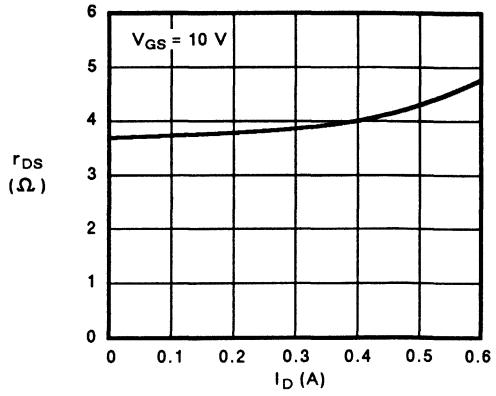
Output Characteristics for Low Gate Drive



Transfer Characteristics



On-Resistance



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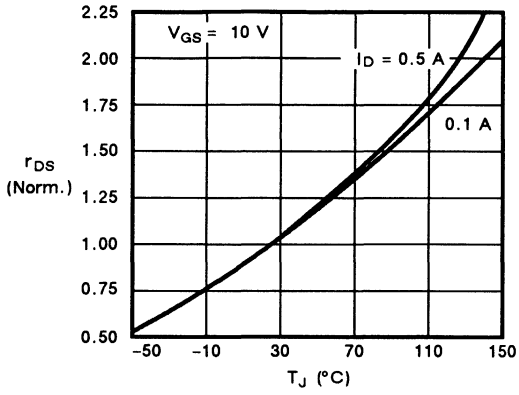
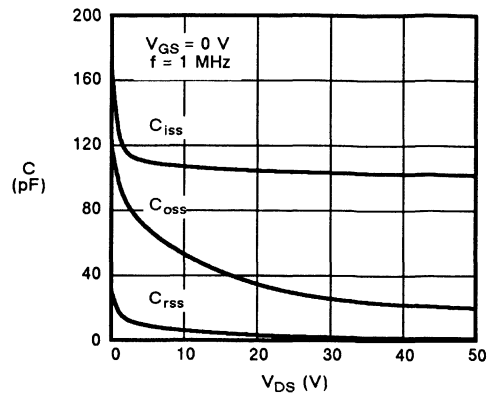
TYPICAL CHARACTERISTICS (Cont'd)

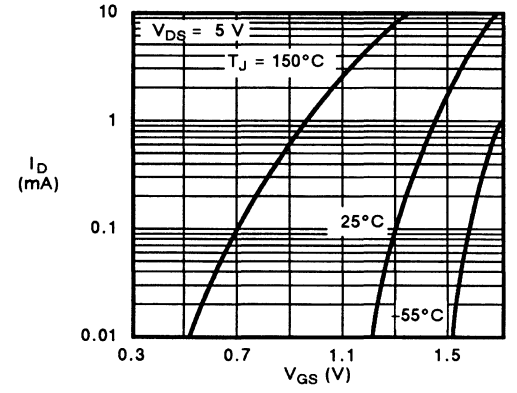
On-Resistance vs. Junction Temperature



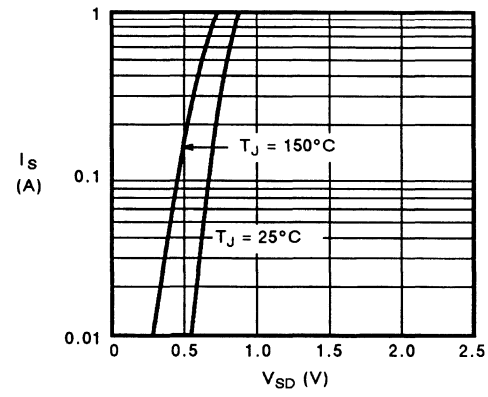
Capacitance



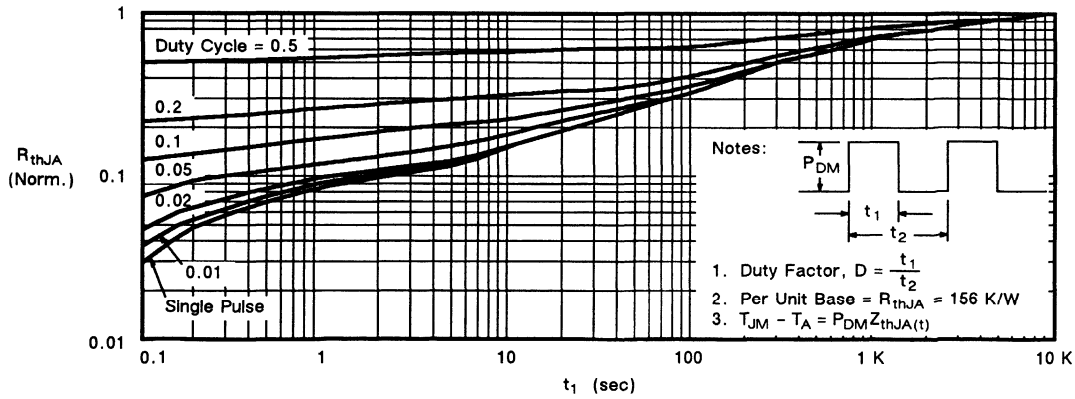
Threshold Region



Source-Drain Diode Forward Voltage

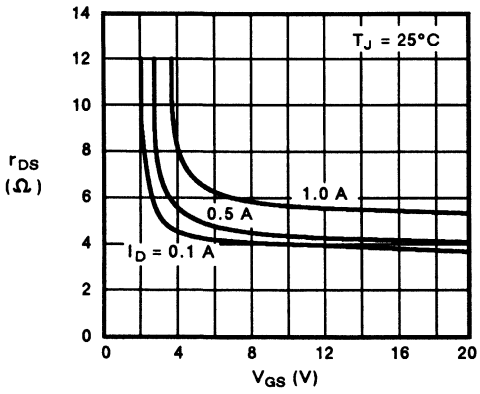


Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)

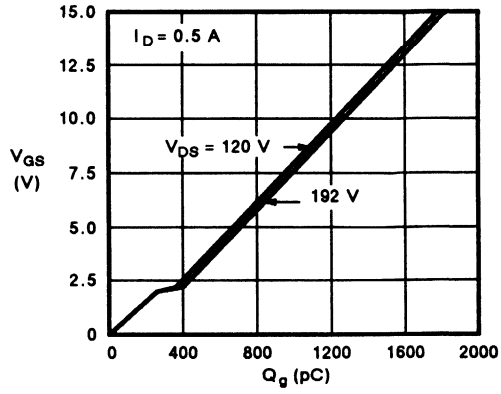


TYPICAL CHARACTERISTICS (Cont'd)

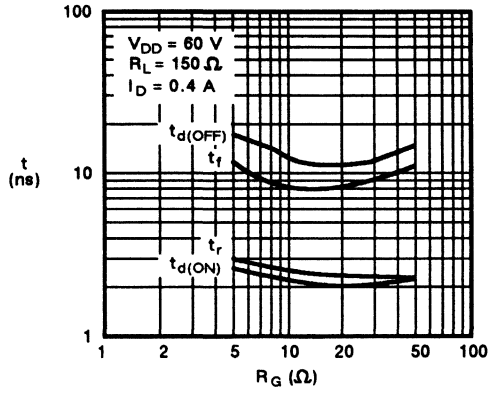
On-Resistance vs. Gate to Source Voltage



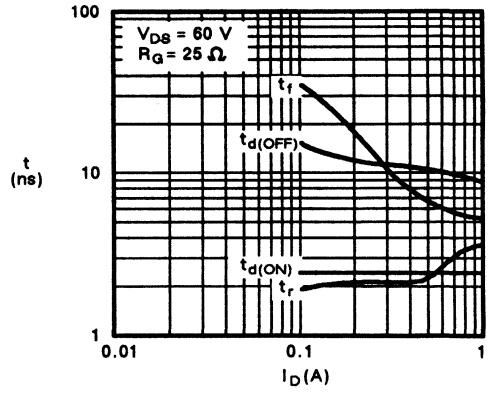
Gate Charge



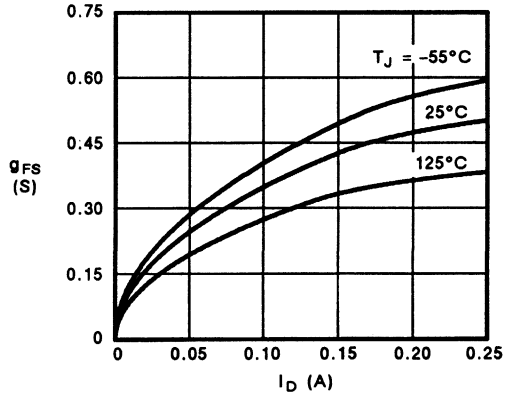
Drive Resistance Effects on Switching



Load Condition Effects on Switching



Transconductance



6

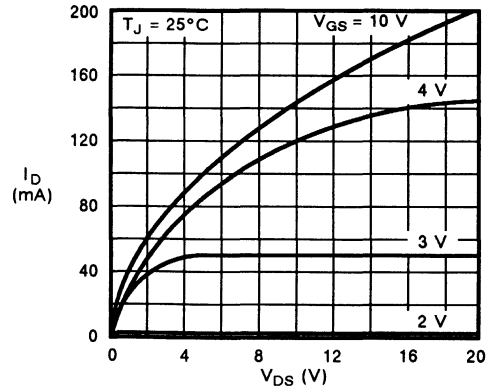
VNDN24
N-Channel
Enhancement-Mode MOSFETs

Siliconix incorporated

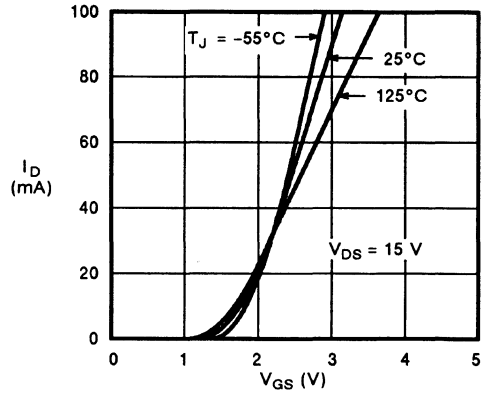
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• VN2406L
Single	TO-39 (TO-205AD)	• VN2406M
Single	TO-220	• VN2406D
Single	SOT-23	• TN2460T
Single	Chip	• Available as VNDN1CHP

TYPICAL CHARACTERISTICS

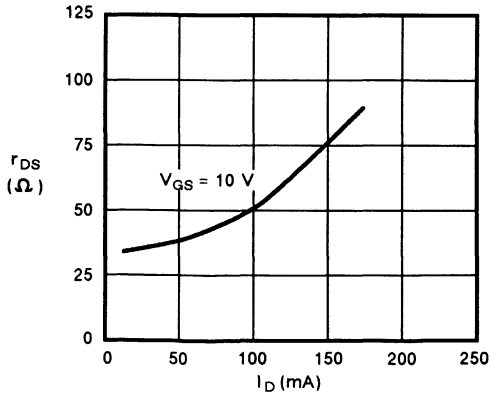
Ohmic Region Characteristics



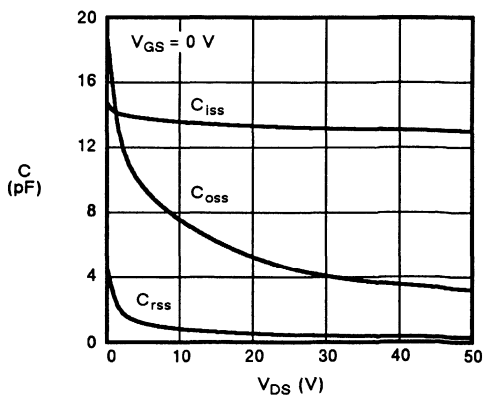
Transfer Characteristics



On-Resistance



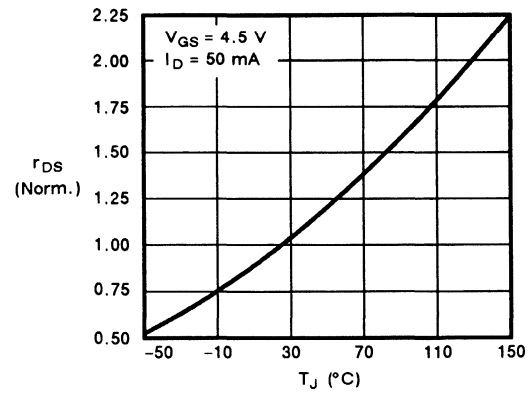
Capacitance



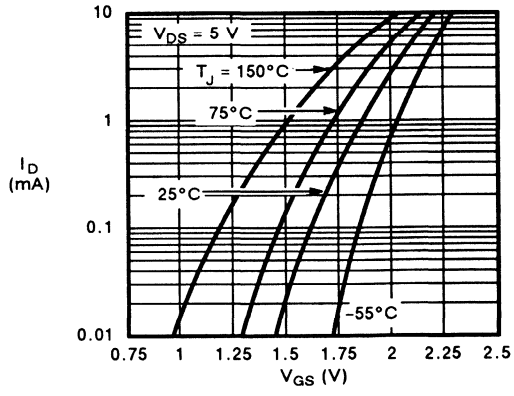
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

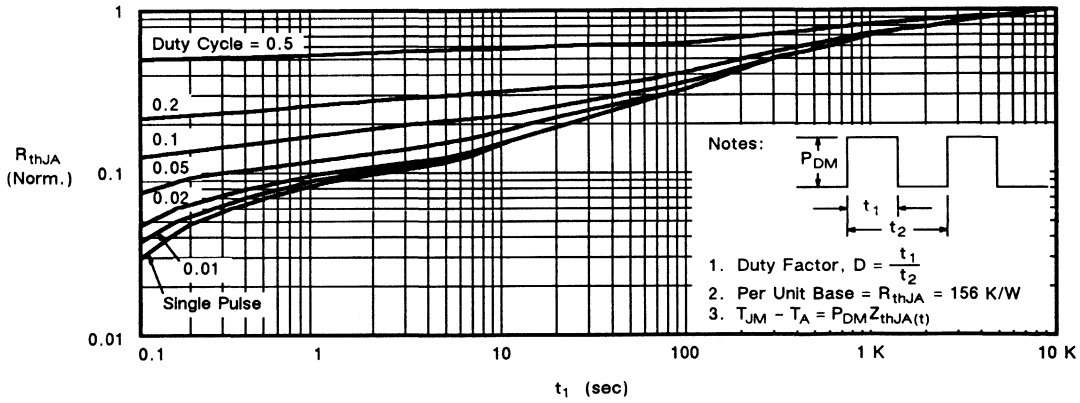
Normalized On-Resistance vs. Junction Temperature



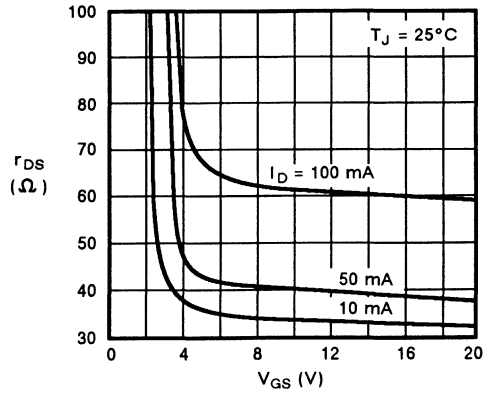
Threshold Region



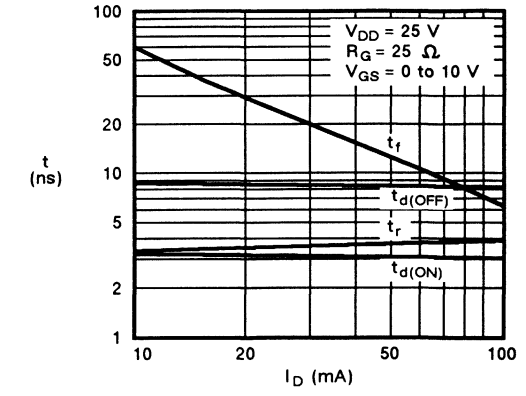
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



On-Resistance vs. Gate to Source Voltage



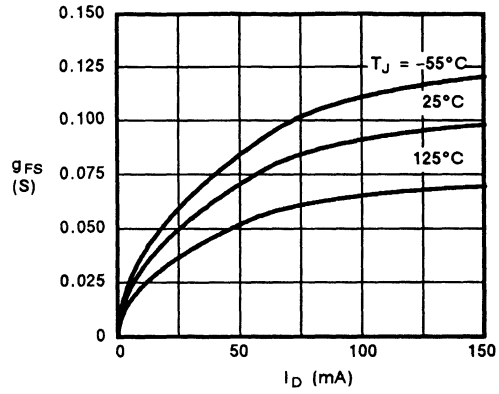
Load Condition Effects on Switching



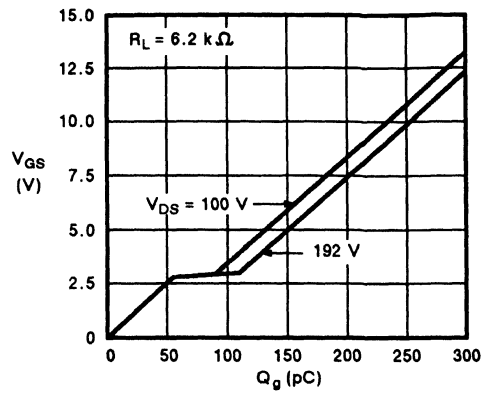
6

TYPICAL CHARACTERISTICS (Cont'd)

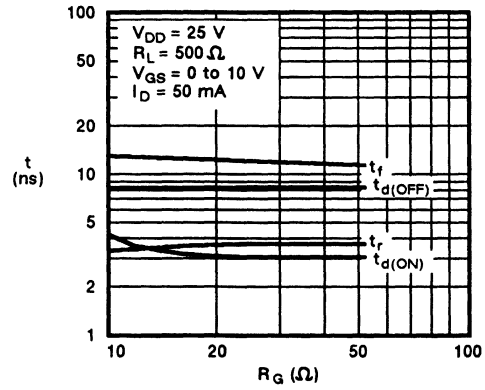
Transconductance



Gate Charge



Drive Resistance Effects on Switching



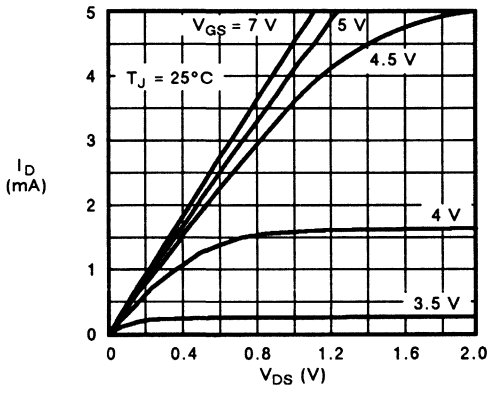
Siliconix incorporated

VNDO50
N-Channel
Enhancement-Mode MOSFETs

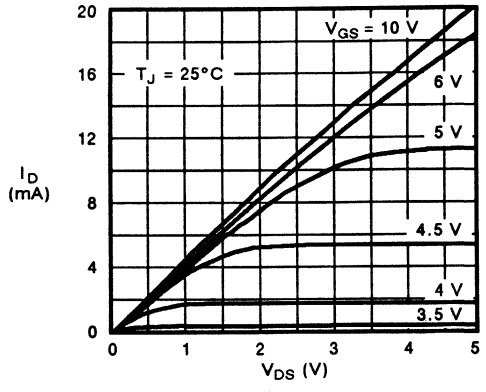
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• VN50300L
Single	SOT-23	• VN50300T
Single	Chip	• Available as VNDO1CHP

TYPICAL CHARACTERISTICS

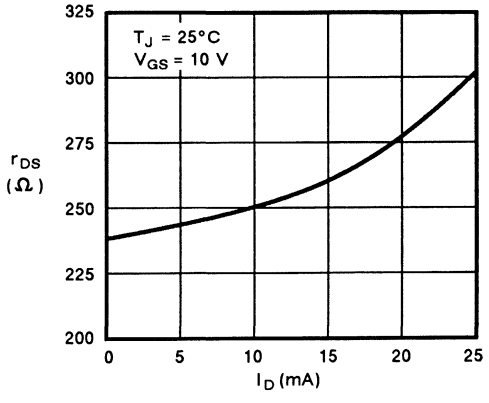
Output Characteristics for Low Gate Drive



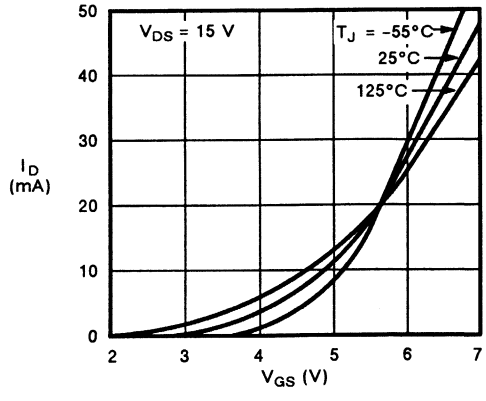
Ohmic Region Characteristics



On-Resistance



Transfer Characteristics



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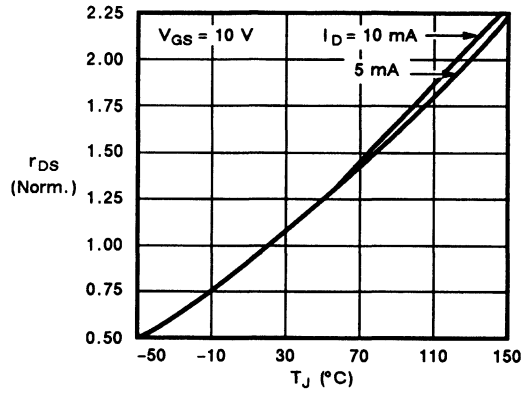
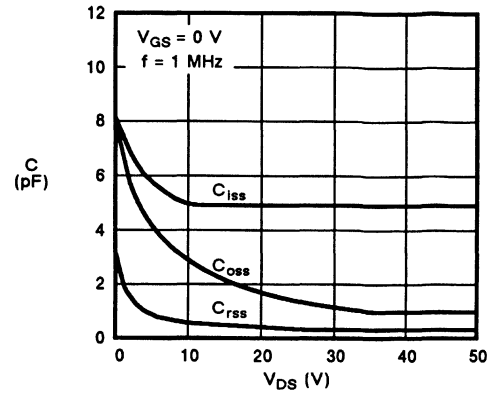
TYPICAL CHARACTERISTICS (Cont'd)

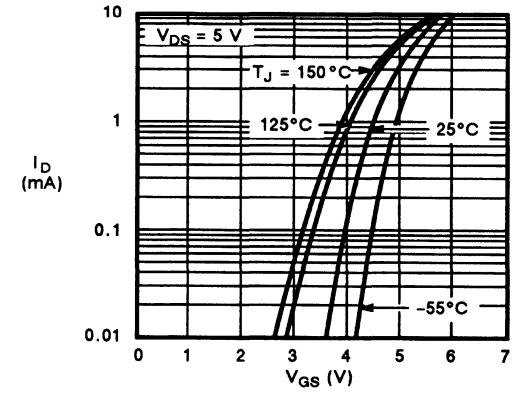
Normalized On-Resistance vs. Junction Temperature



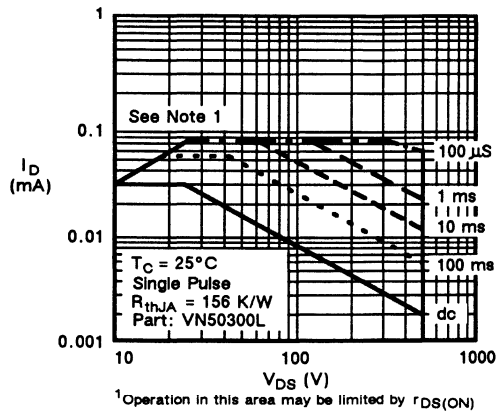
Capacitance



Threshold Region

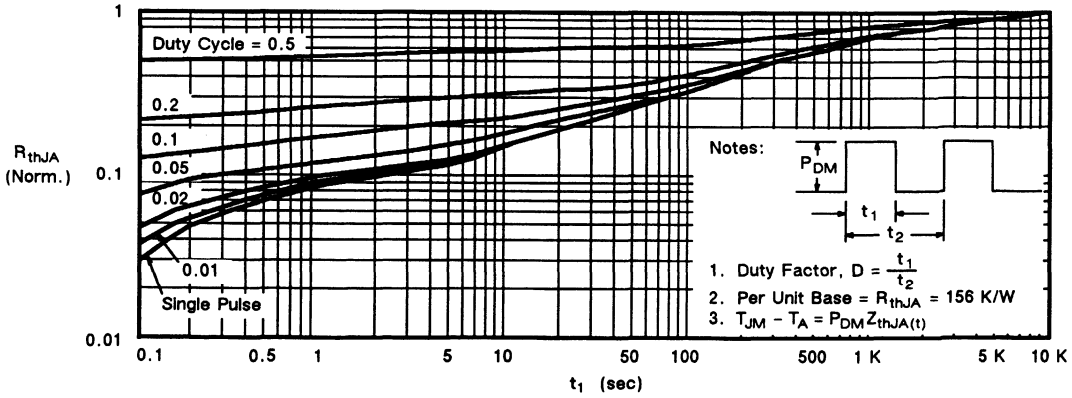


Safe Operating Area (VN50300L)



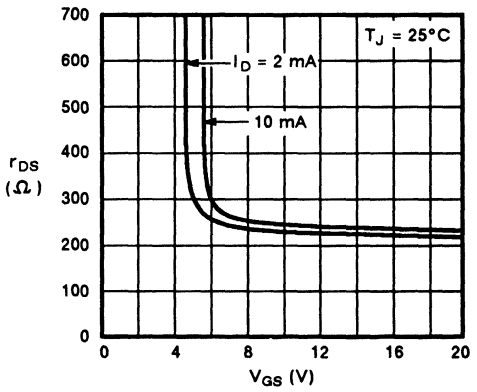
[1]Operation in this area may be limited by $r_{DS(ON)}$

Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)

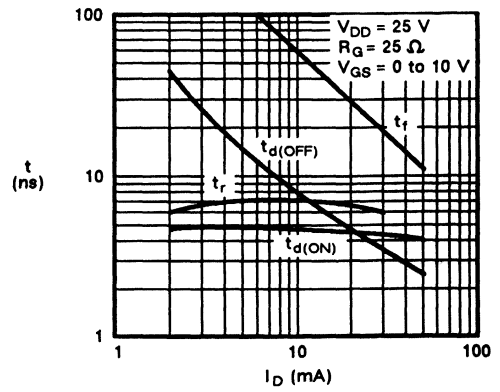


TYPICAL CHARACTERISTICS (Cont'd)

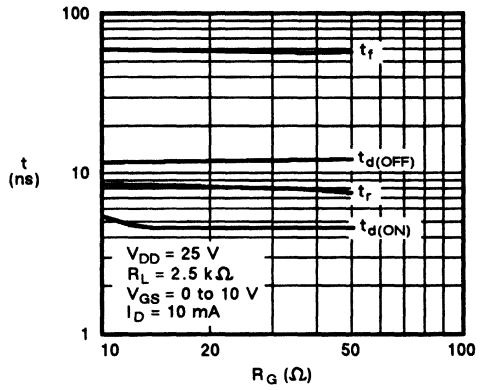
On-Resistance vs. Gate to Source Voltage



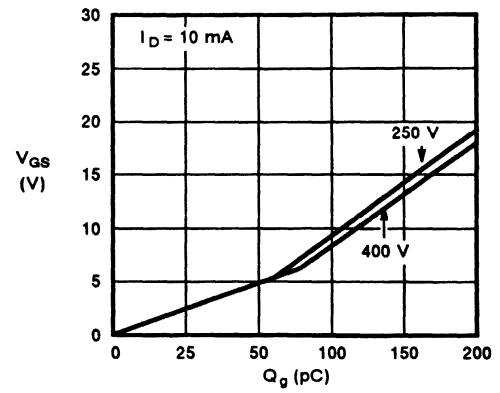
Load Condition Effects on Switching



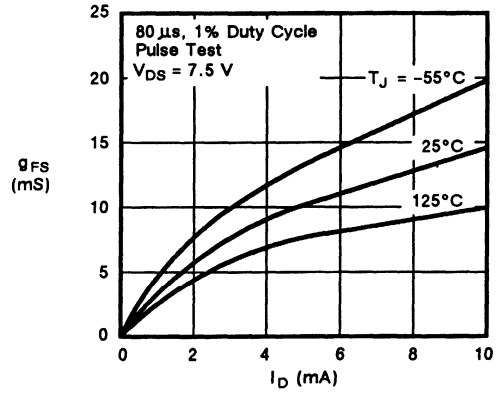
Drive Resistance Effects on Switching



Gate Charge



Transconductance



6

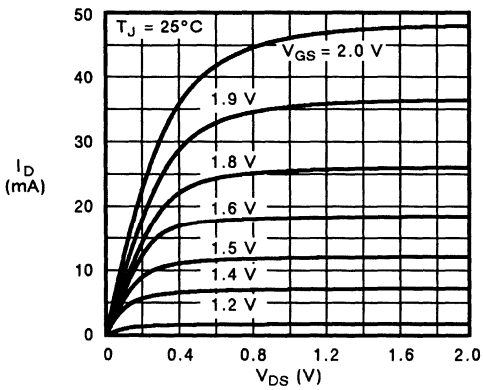
VNDP06
N-Channel
Enhancement-Mode MOSFETs

Siliconix incorporated

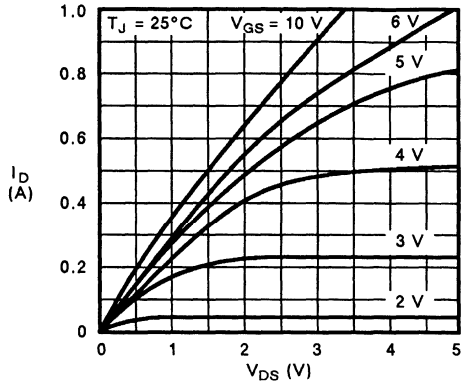
TYPE	PACKAGE	DEVICE
Single	TO-52 (TO-206AC)	• VN10KE
Single	TO-92 (TO-226AA)	• VN0610L, VN2222L
Single	TO-237	• VN10KM
Single	Chip	• Available as VNDP1CHP

TYPICAL CHARACTERISTICS

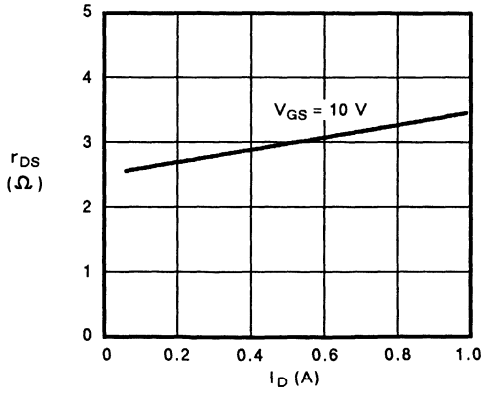
Output Characteristics for Low Gate Drive



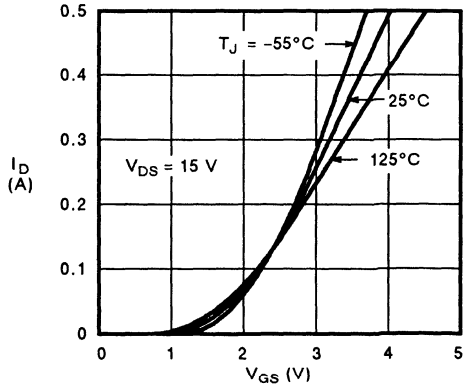
Ohmic Region Characteristics



On-Resistance



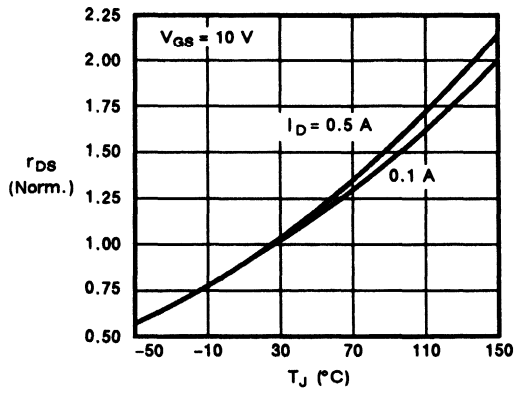
Transfer Characteristics



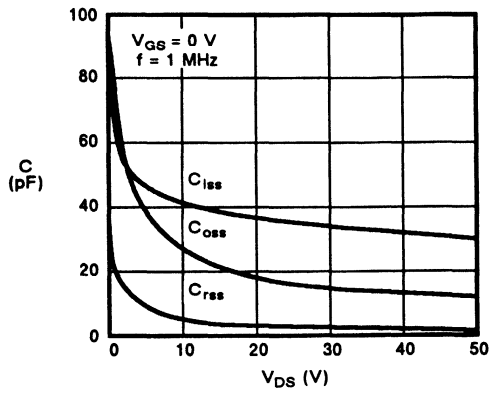
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

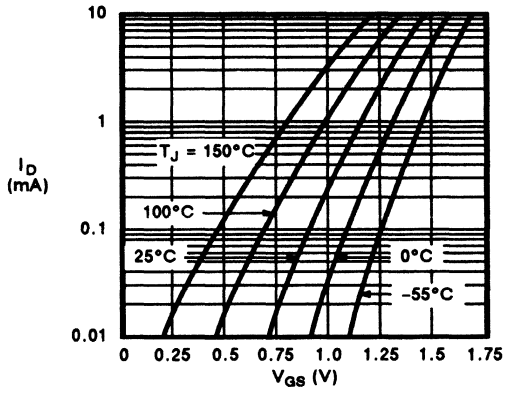
Normalized On-Resistance vs. Junction Temperature



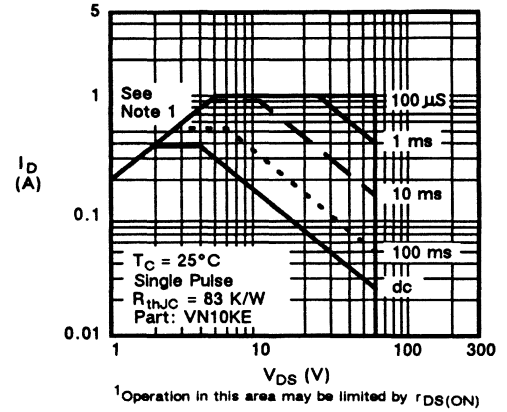
Capacitance



Threshold Region

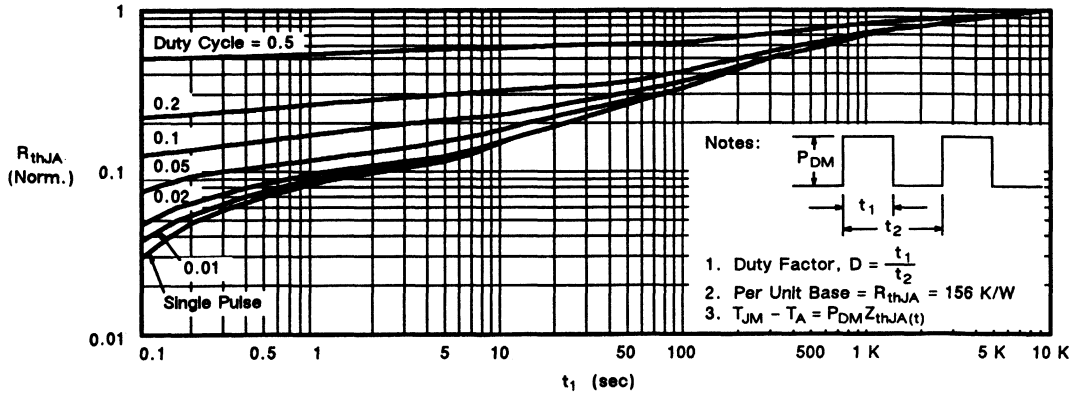


Safe Operating Area - TO-52 (TO-206AC)



[1]Operation in this area may be limited by $r_{DS(ON)}$

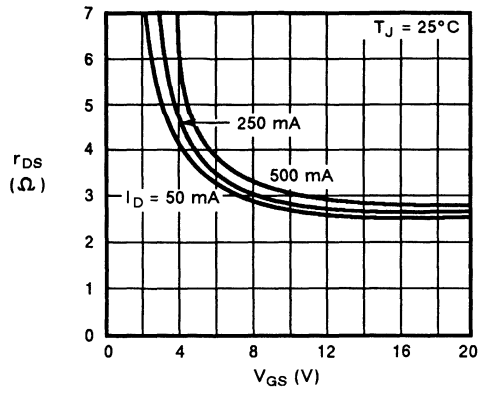
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



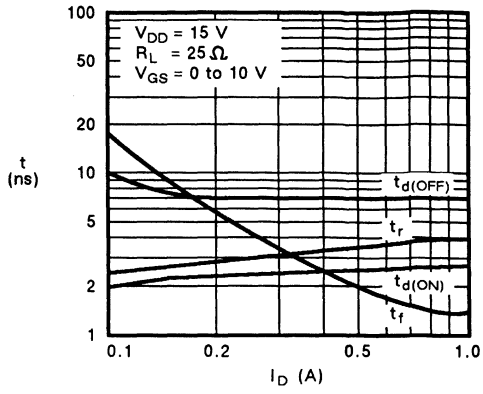
6

TYPICAL CHARACTERISTICS (Cont'd)

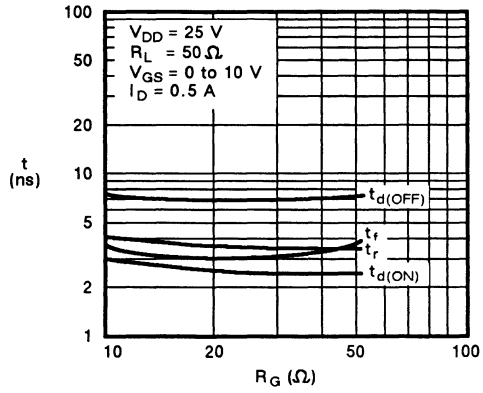
On-Resistance vs. Gate to Source Voltage



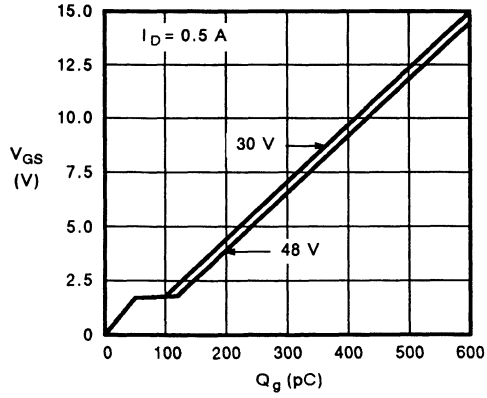
Load Condition Effects on Switching



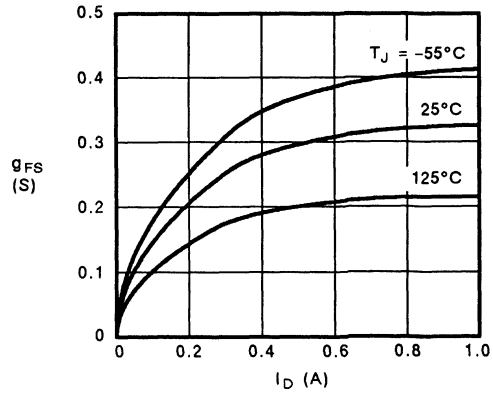
Drive Resistance Effects on Switching



Gate Charge



Transconductance



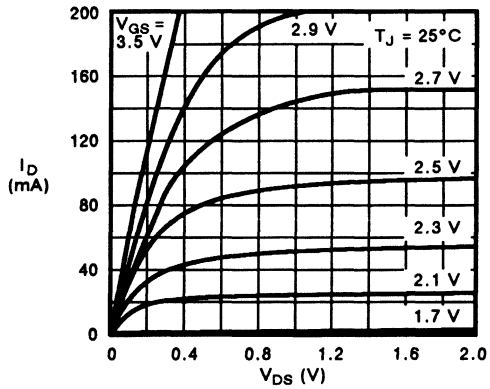
Siliconix incorporated

VNDQ03
N-Channel
Enhancement-Mode MOSFETs

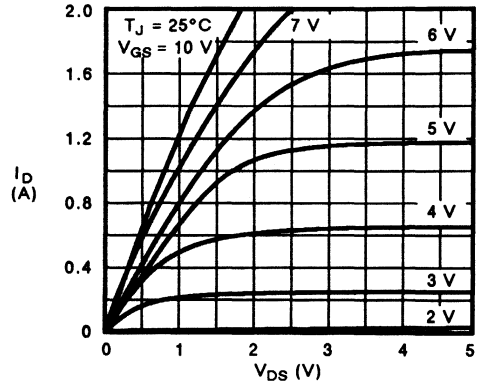
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• VN0300L, TN0201L, TN0401L
Single	TO-237	• VN0300M
Single	14-Pin Plastic	• VQ1001J
Quad	14-Pin Dual-In-Line	• VQ1001P
Quad	Chip	• Available as VNDQ1CHP

TYPICAL CHARACTERISTICS

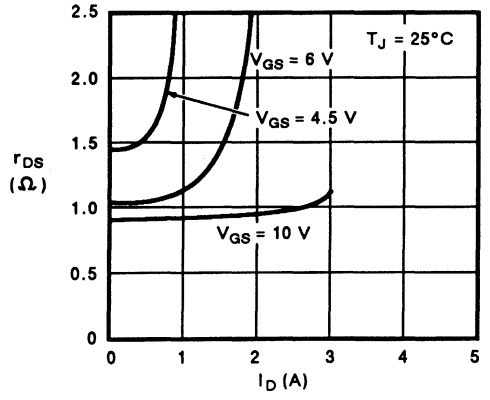
Output Characteristics for Low Gate Drive



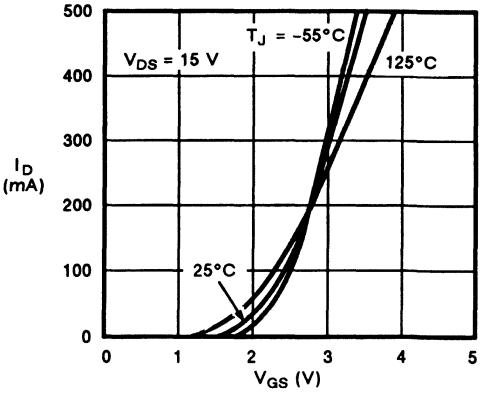
Ohmic Region Characteristics



On-Resistance



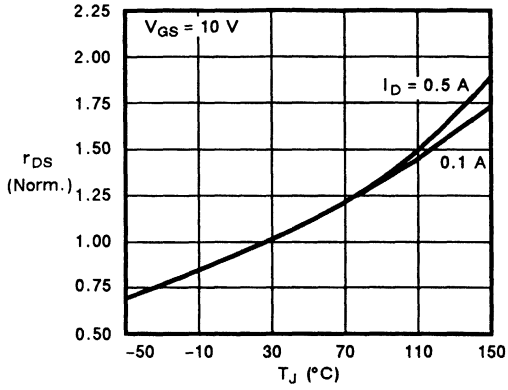
Transfer Characteristics



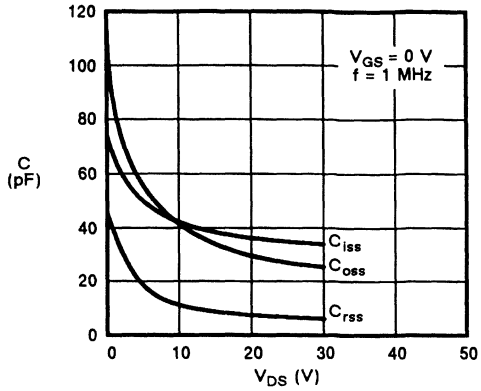
6

TYPICAL CHARACTERISTICS (Cont'd)

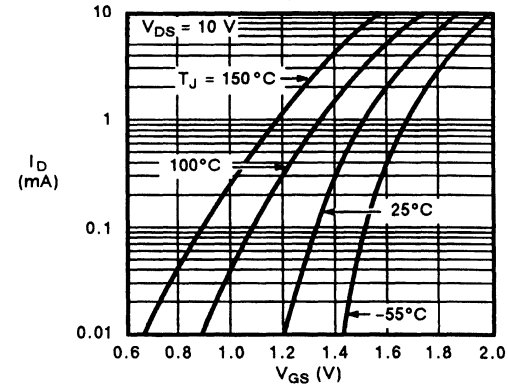
Normalized On-Resistance vs. Junction Temperature



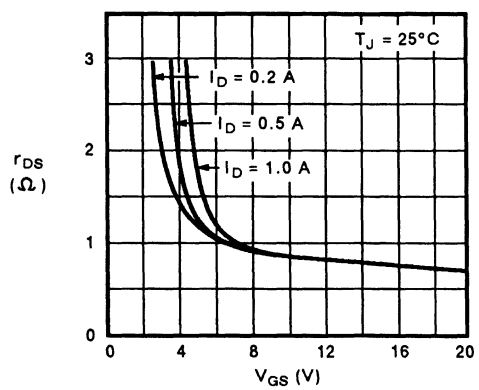
Capacitance



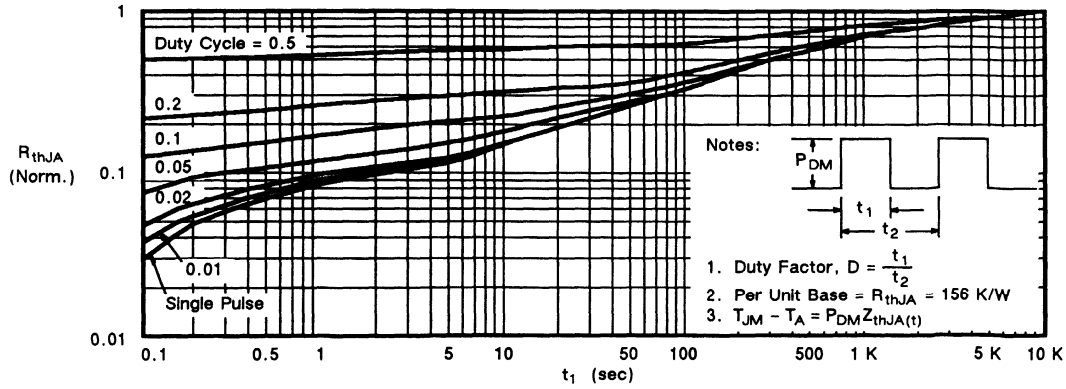
Threshold Region



On-Resistance vs. Gate to Source Voltage

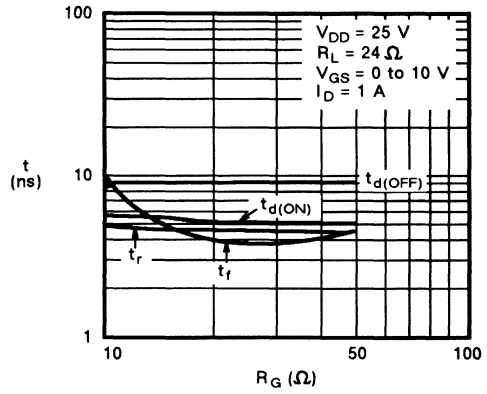


Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)

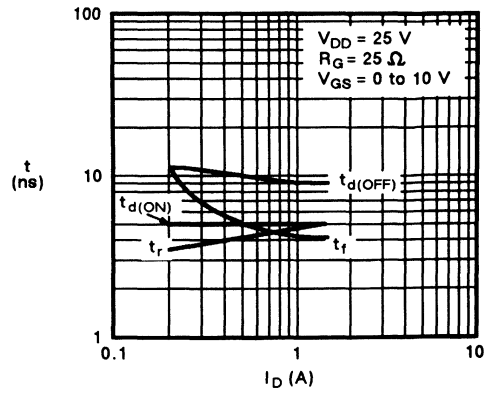


TYPICAL CHARACTERISTICS (Cont'd)

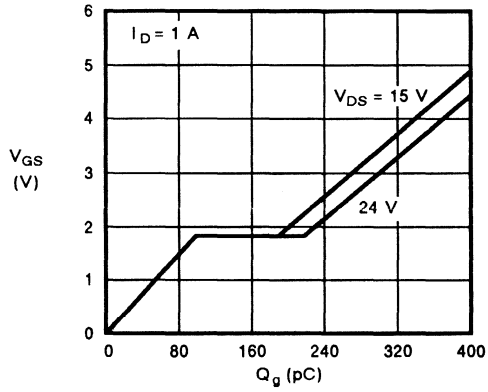
Drive Resistance Effects on Switching



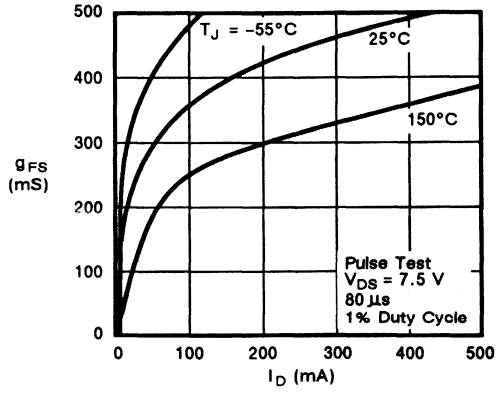
Load Condition Effects on Switching



Gate Charge



Transconductance



6

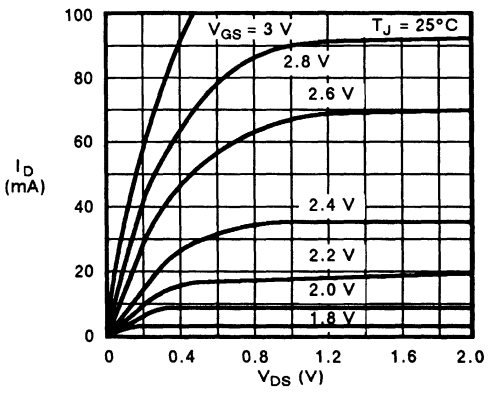
VNDQ06
N-Channel
Enhancement-Mode MOSFETs

Siliconix incorporated

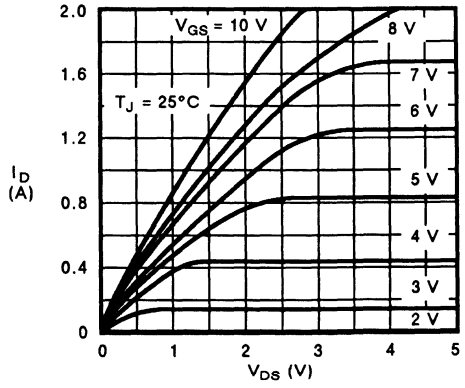
TYPE	PACKAGE	DEVICE
Single	TO-39 (TO-205AD)	• 2N6659, 2N6660
Single	TO-220SD	• VN46AFD, AN66AFD
Single	TO-237	• VN0606M
Single	TO-92 (TO-226AA)	• TN0601L
Quad	14-Pin Plastic	• VQ1004J, TQ1004J
Quad	14-Pin Dual-In-Line	• VQ1004P
Quad	Chip	• Available as VNDQ2CHP

TYPICAL CHARACTERISTICS

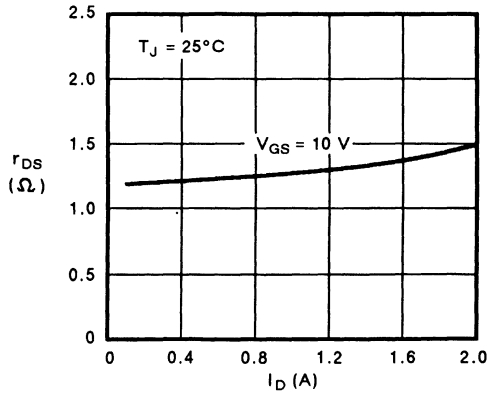
Output Characteristics for Low Gate Drive



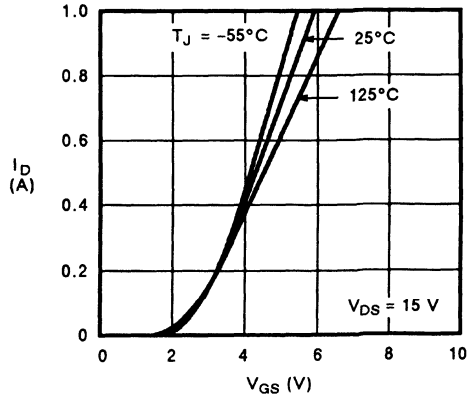
Ohmic Region Characteristics



On-Resistance



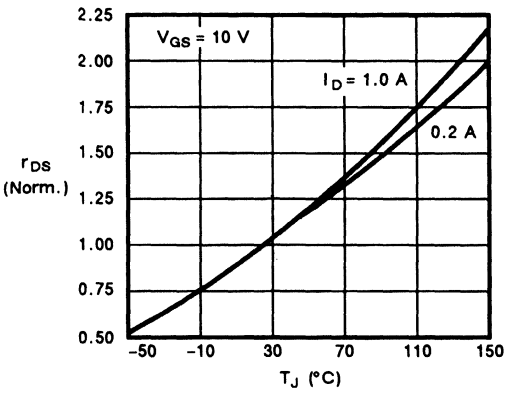
Transfer Characteristics



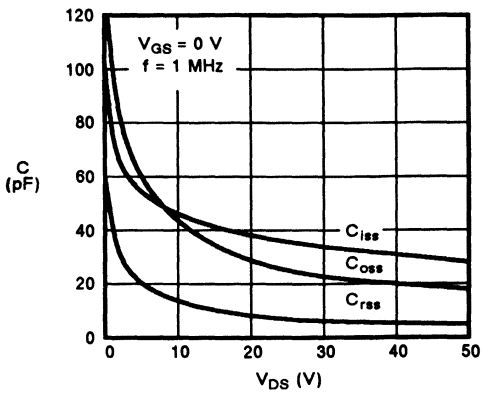
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

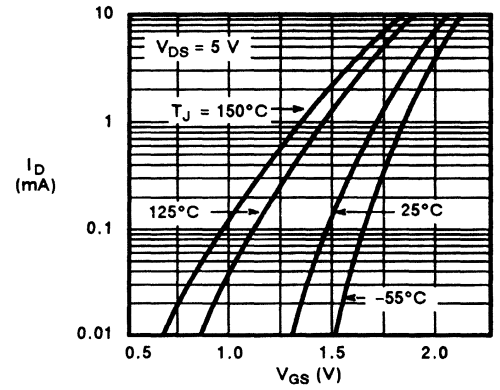
Normalized On-Resistance vs. Junction Temperature



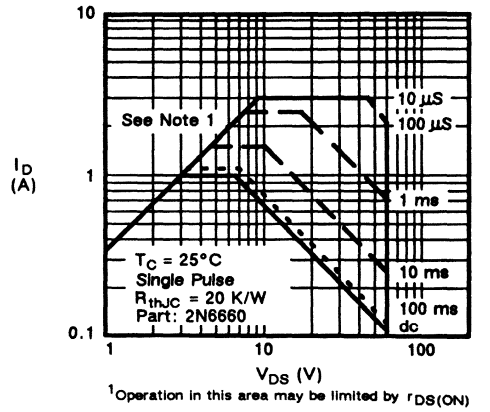
Capacitance



Threshold Region

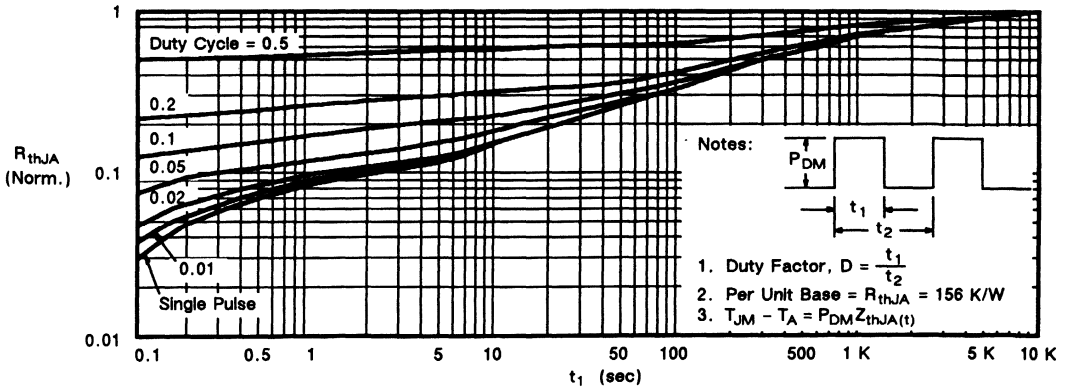


Safe Operating Area (2N6660)



[1]Operation in this area may be limited by $r_{DS(ON)}$

Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



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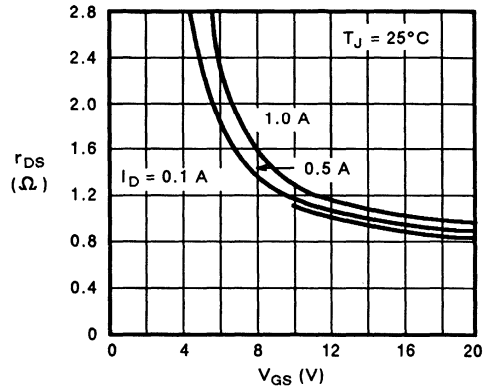
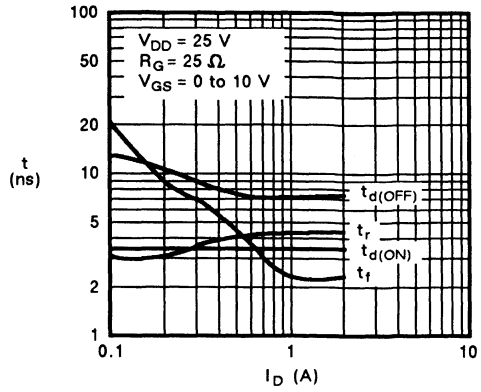
TYPICAL CHARACTERISTICS (Cont'd)

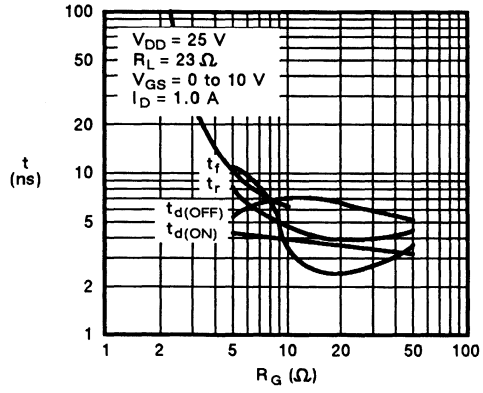
On-Resistance vs. Gate to Source Voltage



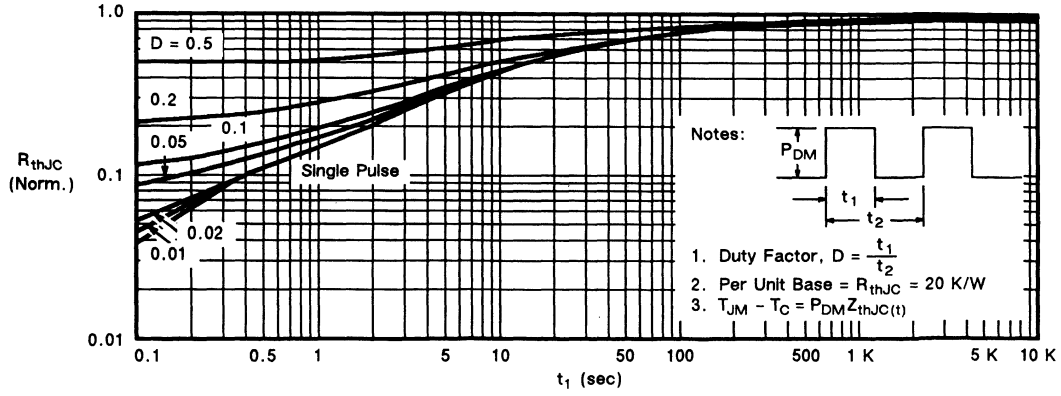
Load Condition Effects on Switching



Drive Resistance Effects on Switching

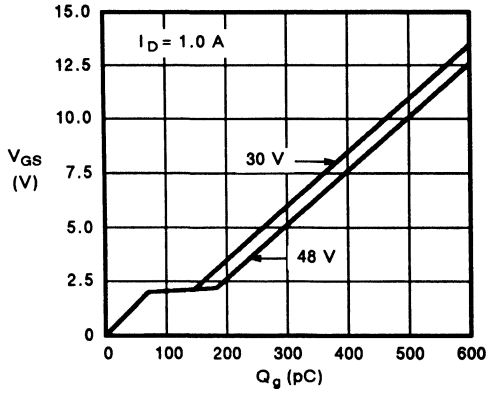


Normalized Effective Transient Thermal Impedance, Junction-to-Case (TO-39)

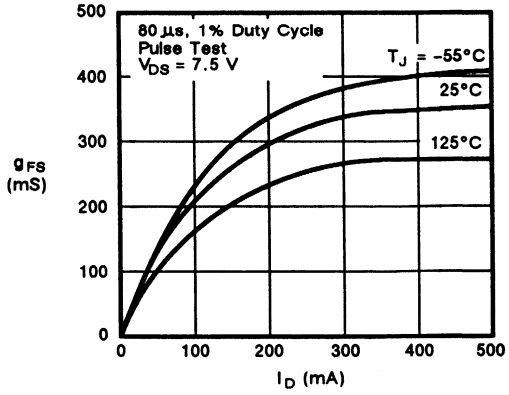


TYPICAL CHARACTERISTICS (Cont'd)

Gate Charge



Transconductance



6

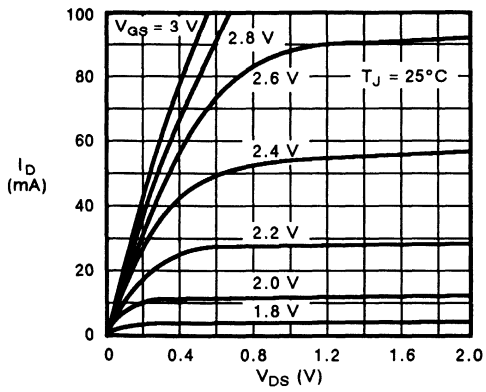
VNDQ09
N-Channel
Enhancement-Mode MOSFETs

Siliconix incorporated

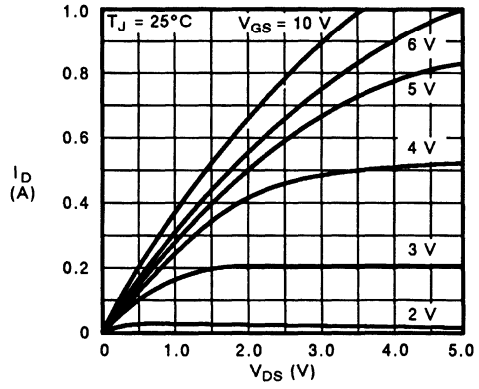
TYPE	PACKAGE	DEVICE
Single	TO-39 (TO-205AD)	• 2N6661
Single	TO-237	• VN0808M
Single	TO-220SD	• VN88AFD
Quad	14-Pin Plastic	• VQ1006J
Quad	14-Pin Dual-In-Line	• VQ1006P
Single	Chip	• Available as VNDQ3CHP

TYPICAL CHARACTERISTICS

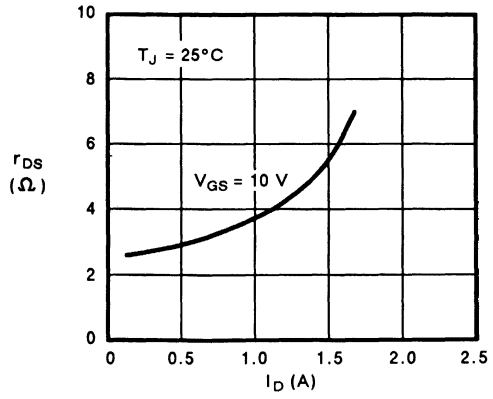
Output Characteristics for Low Gate Drive



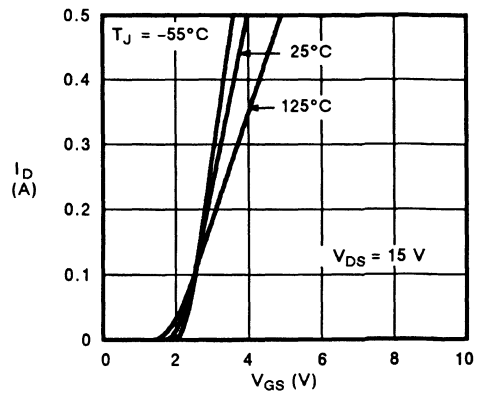
Ohmic Region Characteristics



On-Resistance



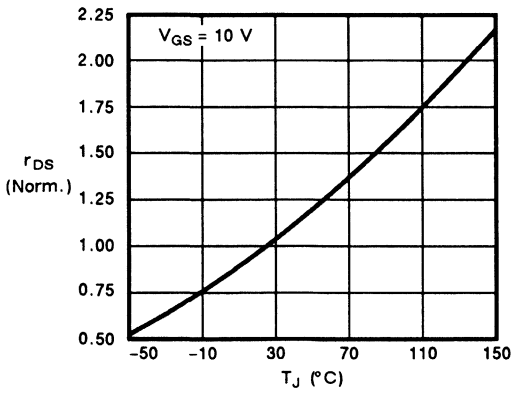
Transfer Characteristics



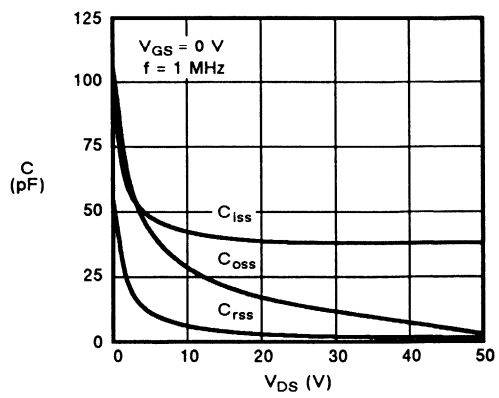
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

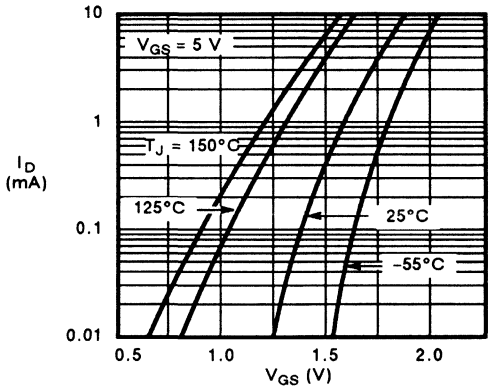
Normalized On-Resistance vs. Junction Temperature



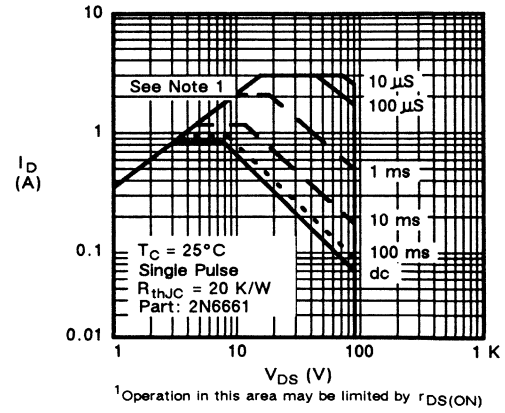
Capacitance



Threshold Region

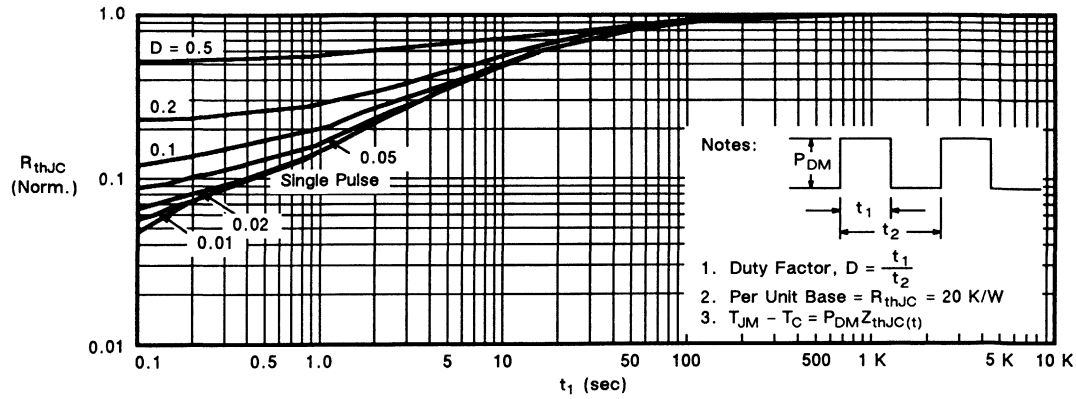


Safe Operating Area (2N6661)



[1]Operation in this area may be limited by $r_{DS(ON)}$

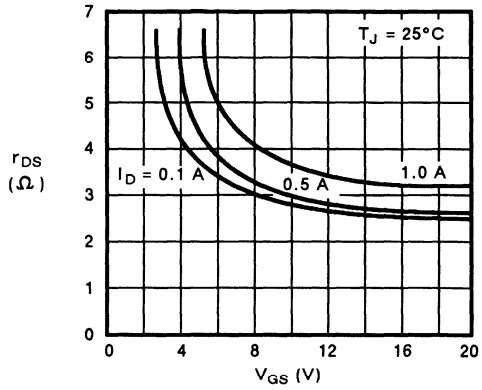
Normalized Effective Transient Thermal Impedance Junction-to-Case (2N6661)



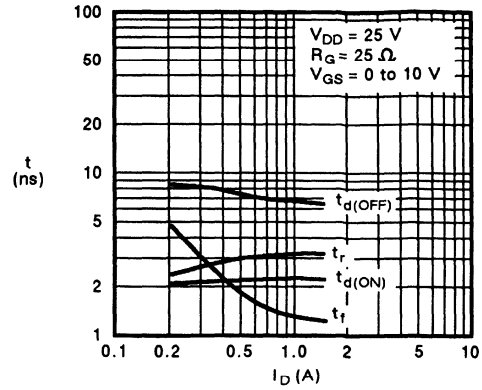
6

TYPICAL CHARACTERISTICS (Cont'd)

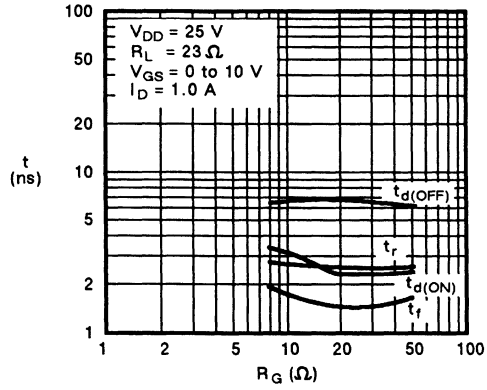
On-Resistance vs. Gate to Source Voltage



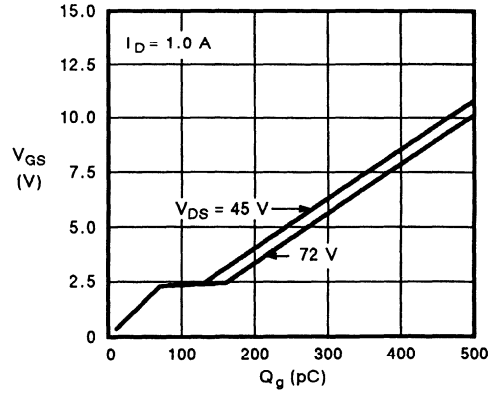
Load Condition Effects on Switching



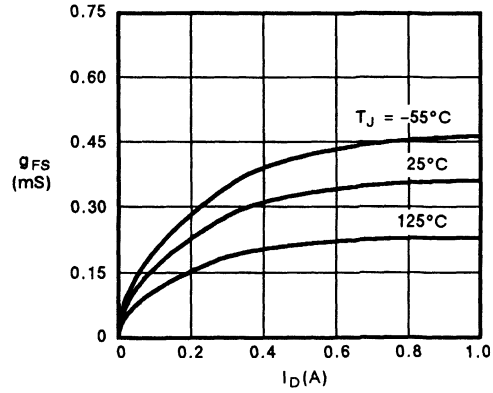
Drive Resistance Effects on Switching



Gate Charge



Transconductance



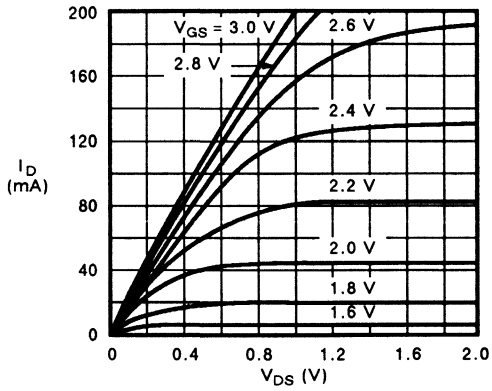
Siliconix incorporated

VNDQ12
N-Channel
Enhancement-Mode MOSFETs

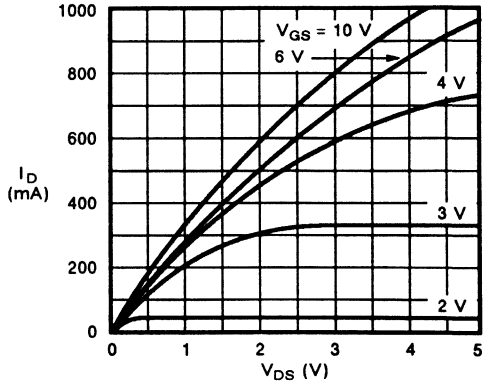
TYPE	PACKAGE	DEVICE
Single	TO-237	• VN1206M, VN1210M
Single	T0-92 (TO-226AA)	• VN1206L, VN1210L, TN1206L
Single	Chip	• Available as VNDQ4CHP

TYPICAL CHARACTERISTICS

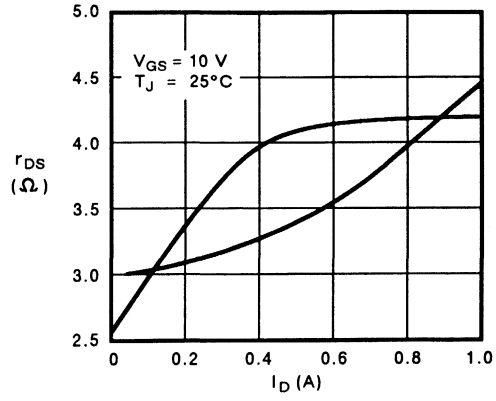
Output Characteristics for Low Gate Drive



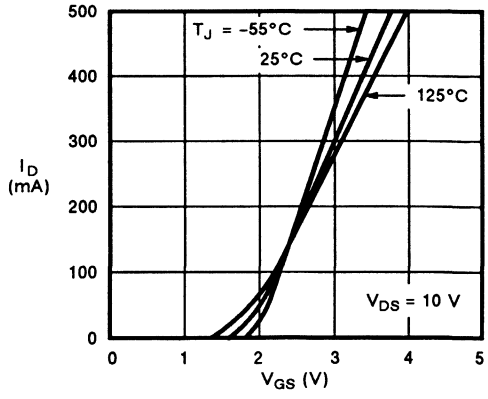
Ohmic Region Characteristics



On-Resistance



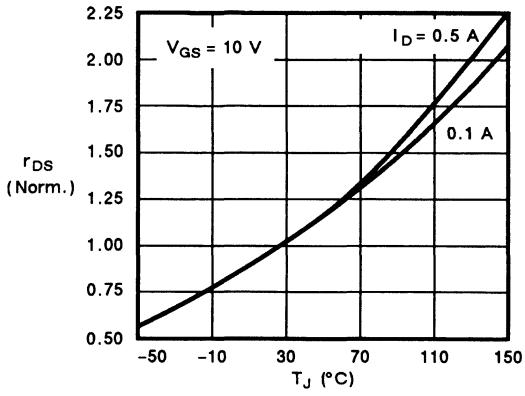
Transfer Characteristics



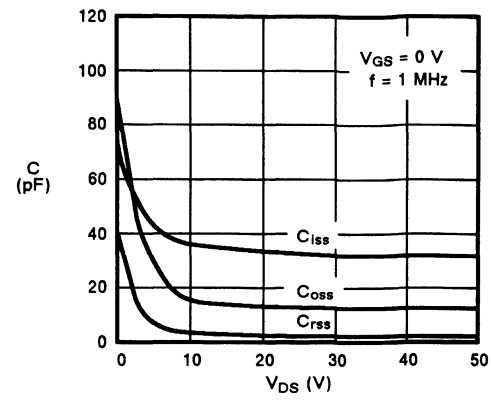
6

TYPICAL CHARACTERISTICS (Cont'd)

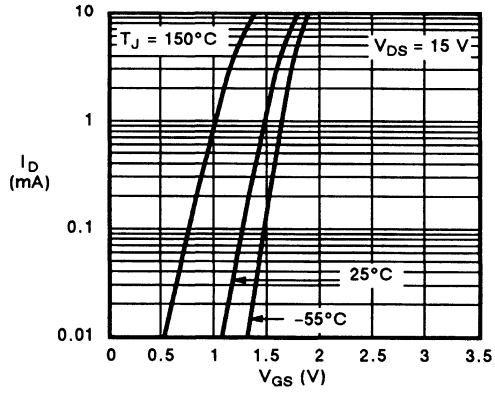
On-Resistance vs. Junction Temperature



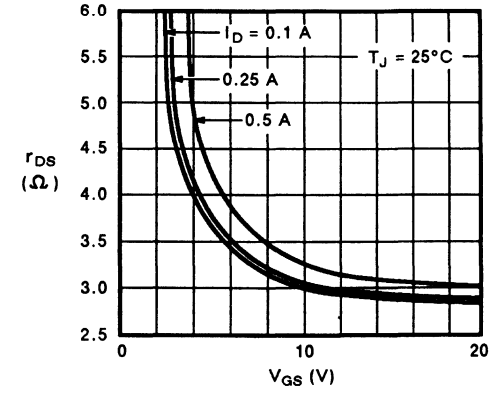
Capacitance



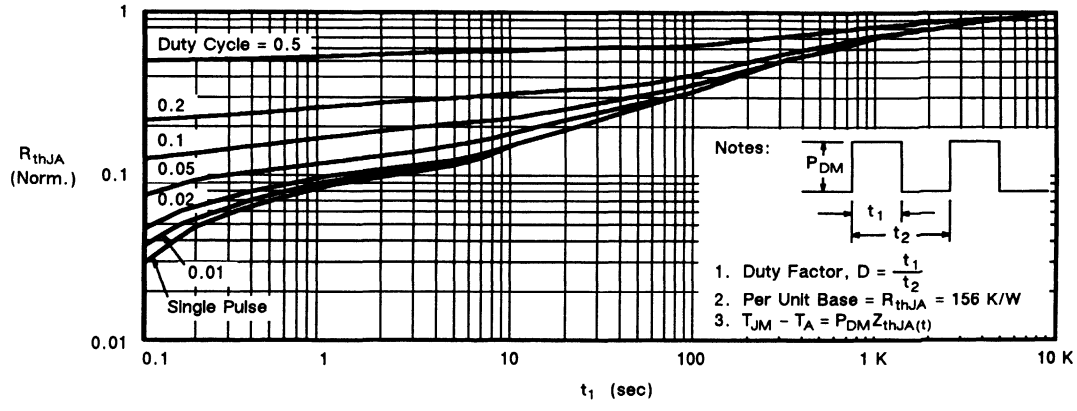
Threshold Region



On-Resistance vs. Gate to Source Voltage

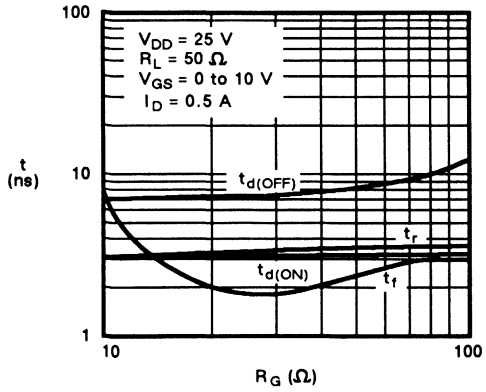


Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)

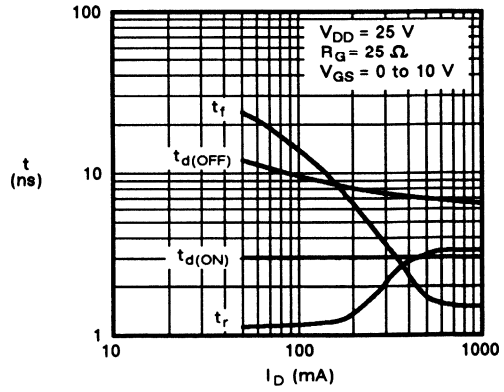


TYPICAL CHARACTERISTICS (Cont'd)

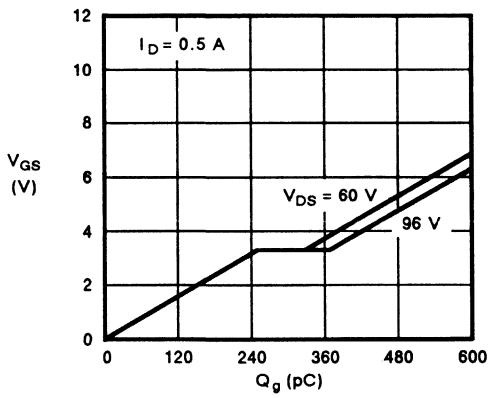
Drive Resistance Effects on Switching



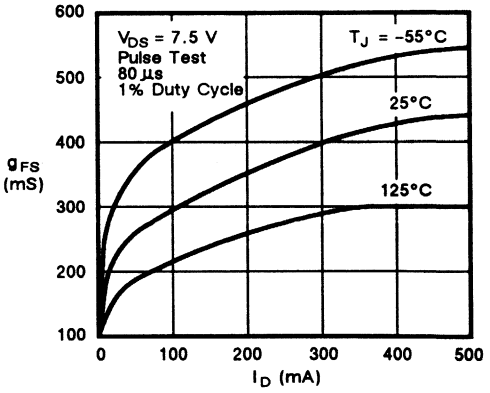
Load Condition Effects on Switching



Gate Charge



Transconductance



6

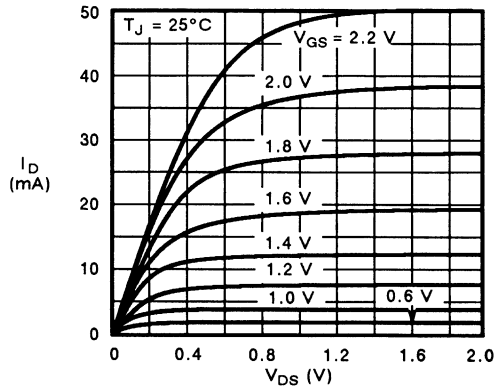
VNDQ20
N-Channel
Enhancement-Mode MOSFETs

Siliconix incorporated

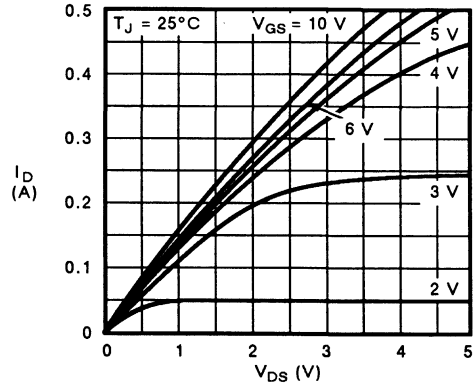
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• BS107 VN2010L
Single	Chip	• Available as VNDQ5CHP

TYPICAL CHARACTERISTICS

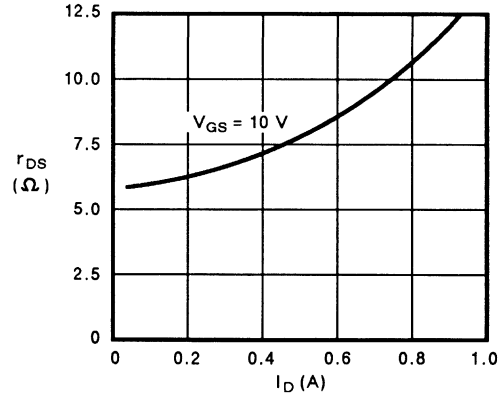
Output Characteristics for Low Gate Drive



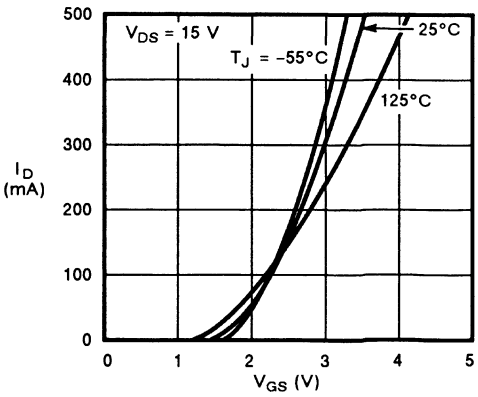
Ohmic Region Characteristics



On-Resistance



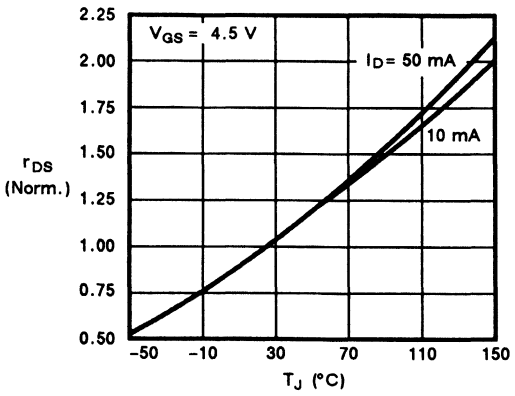
Transfer Characteristics



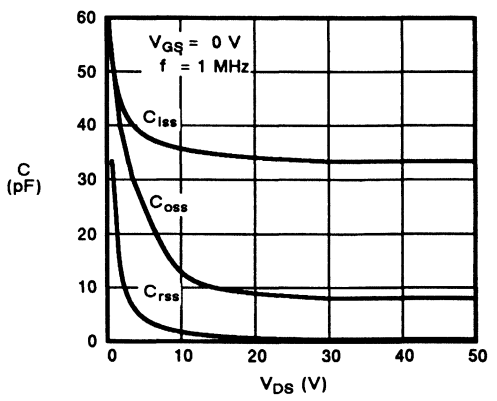
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

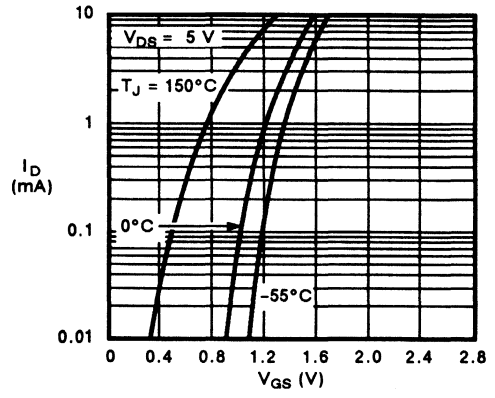
Normalized On-Resistance vs. Junction Temperature



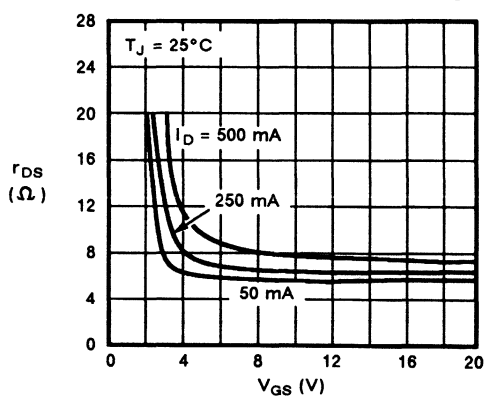
Capacitance



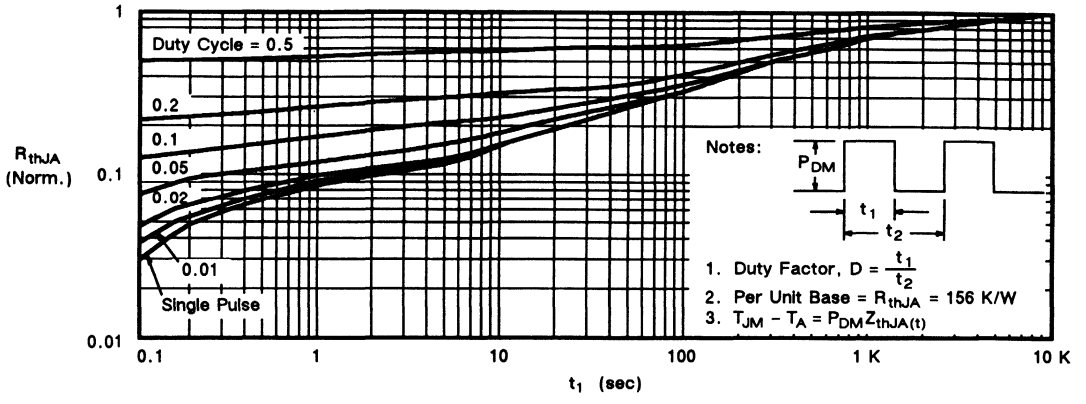
Threshold Region



On-Resistance vs. Gate to Source Voltage



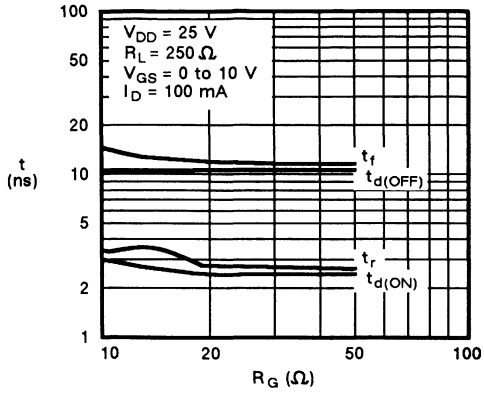
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



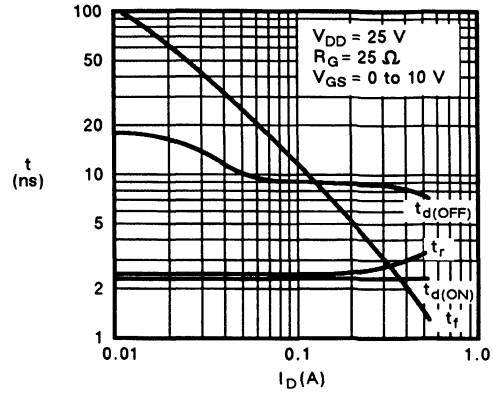
6

TYPICAL CHARACTERISTICS (Cont'd)

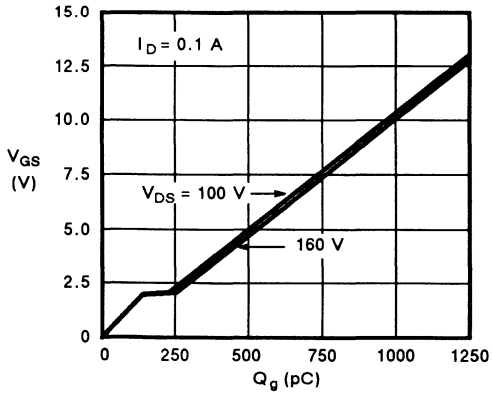
Drive Resistance Effects on Switching



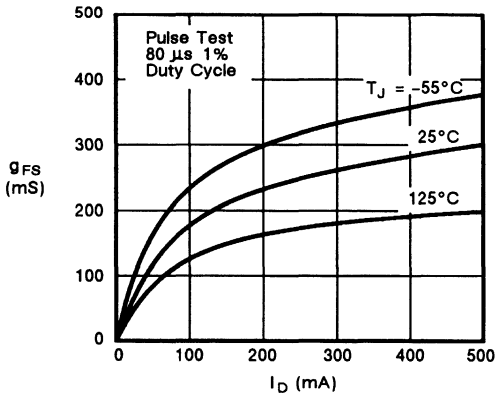
Load Condition Effects on Switching



Gate Charge



Transconductance



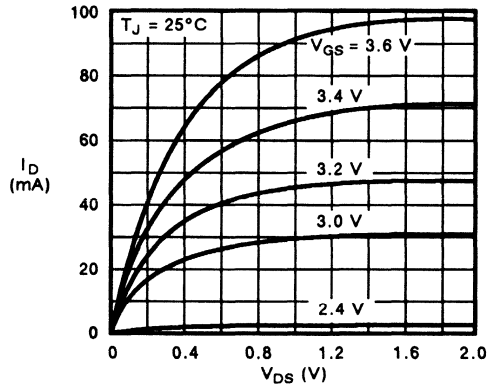
Siliconix incorporated

VNDS06
N-Channel
Enhancement-Mode MOSFETs

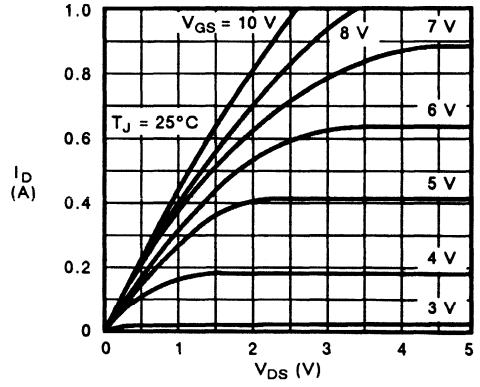
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• 2N7000, VN0610LL, VN2222LL
Single	TO-237	• VN2222LM
Single	SOT-23	• VN0605T, 2N7002
Quad	14-Pin Plastic	• VQ1000J
Quad	14-Pin Dual-In-Line	• VQ1000P
Quad	Chip	• Available as VNDS1CHP

TYPICAL CHARACTERISTICS

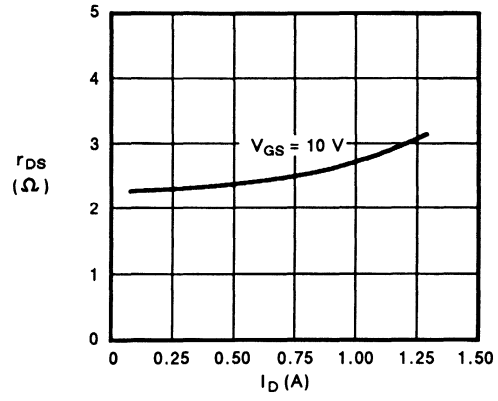
Output Characteristics for Low Gate Drive



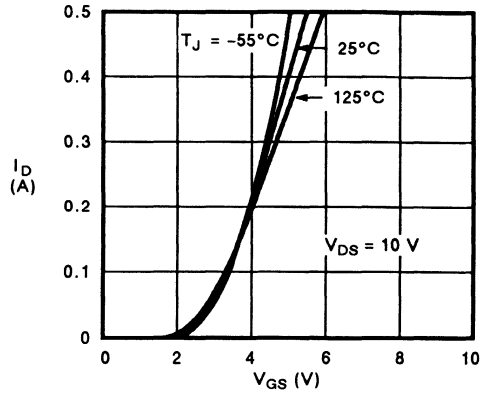
Ohmic Region Characteristics



On-Resistance



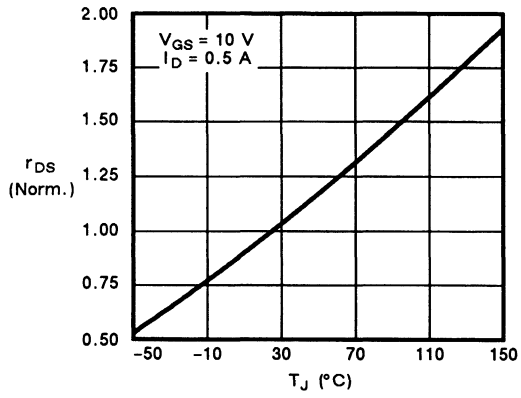
Transfer Characteristics



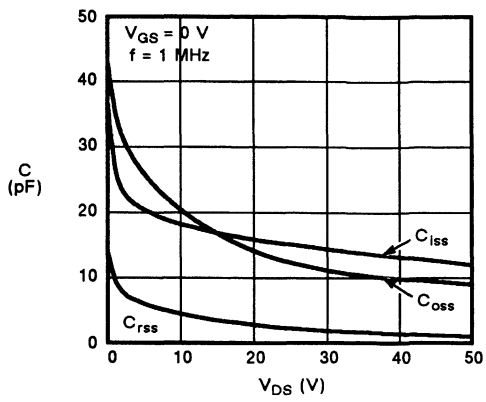
6

TYPICAL CHARACTERISTICS (Cont'd)

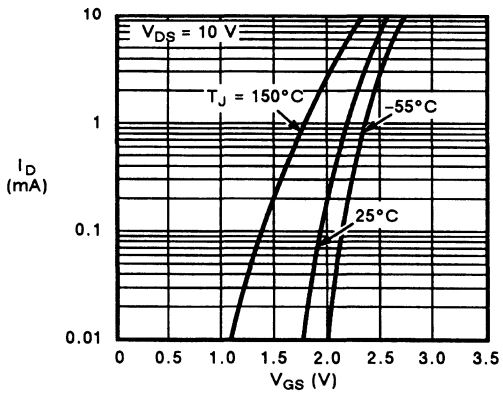
On-Resistance vs. Junction Temperature



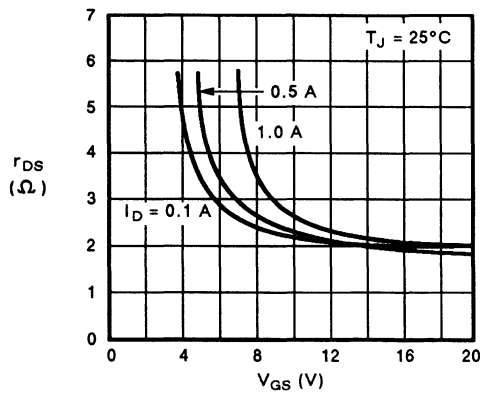
Capacitance



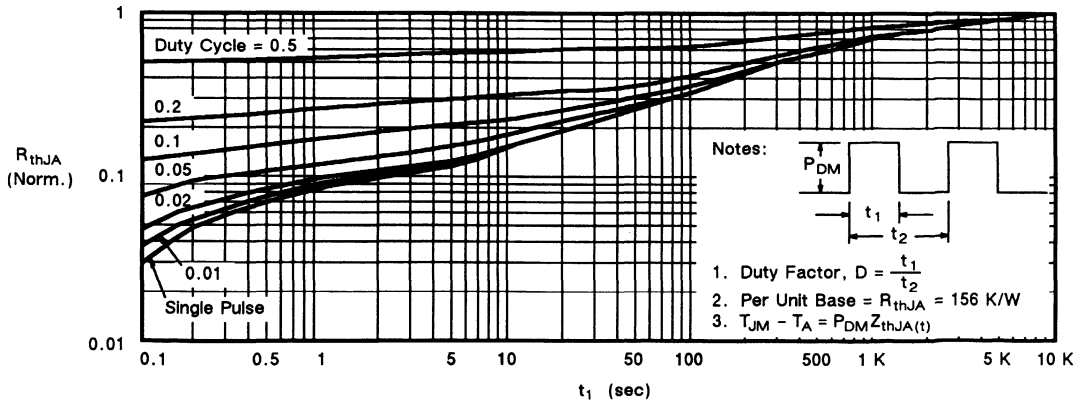
Threshold Region



On-Resistance vs. Gate to Source Voltage

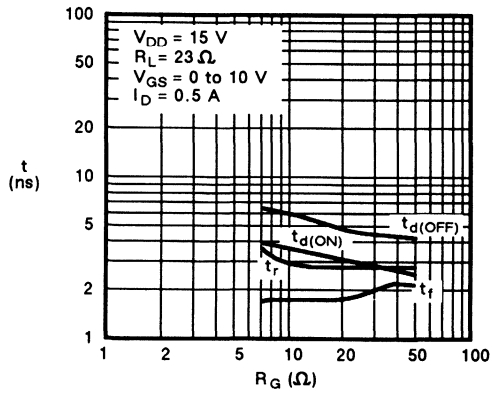


Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)

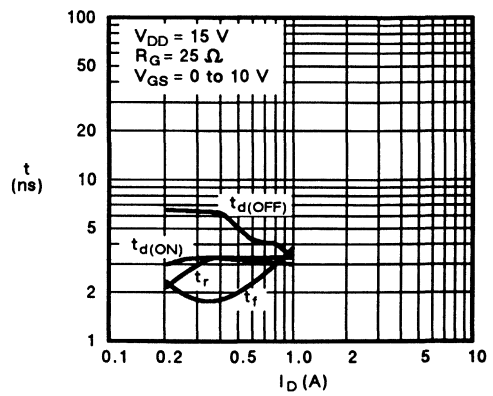


TYPICAL CHARACTERISTICS (Cont'd)

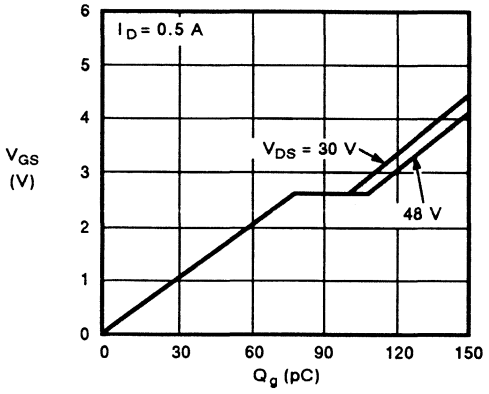
Drive Resistance Effects on Switching



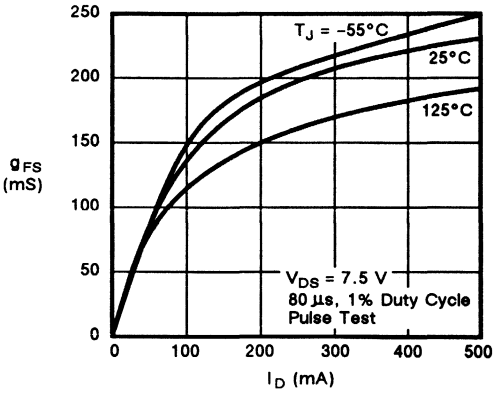
Load Condition Effects on Switching



Typical Gate Charge



Typical Transconductance



6

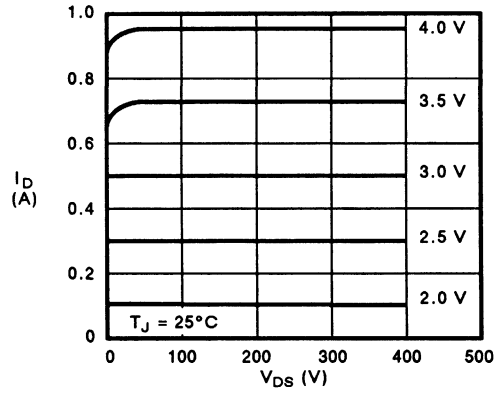
VNDV40
N-Channel
Enhancement-Mode MOSFETs

Siliconix incorporated

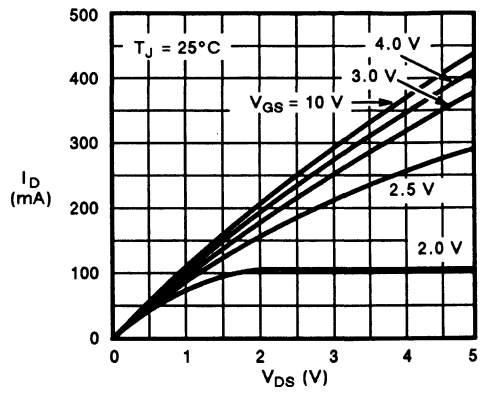
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• TN3512L, TN4012L, VN3515L, VN4012L
Single	Chip	• Available as VNDV1CHP

TYPICAL CHARACTERISTICS

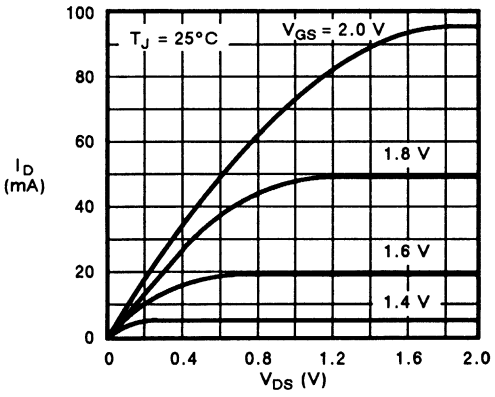
Output Characteristics



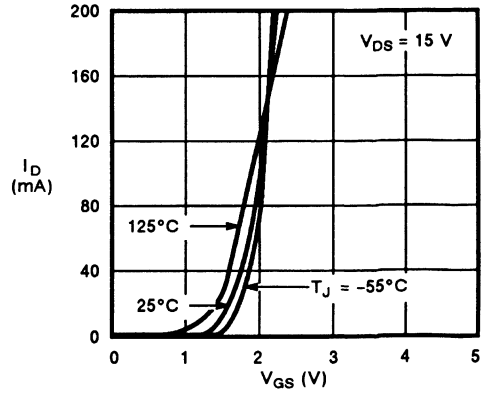
Ohmic Region Characteristics



Output Characteristics for Low Gate Drive



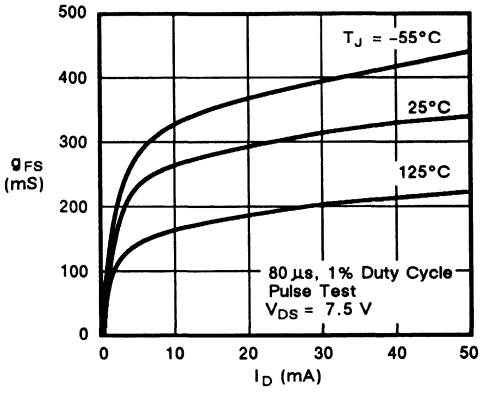
Transfer Characteristics



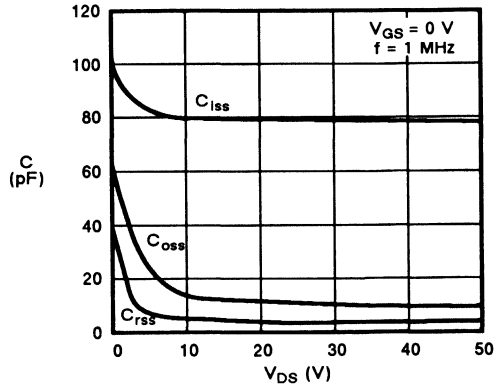
Revised (02/11/91)

TYPICAL CHARACTERISTICS

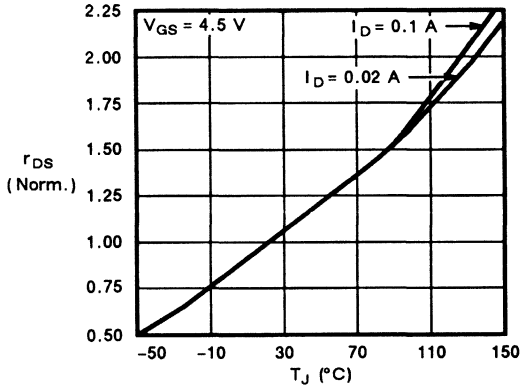
Transconductance



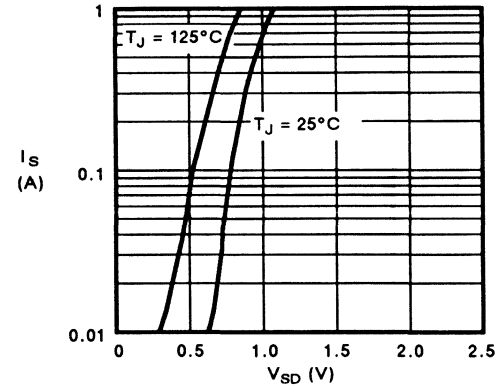
Capacitance



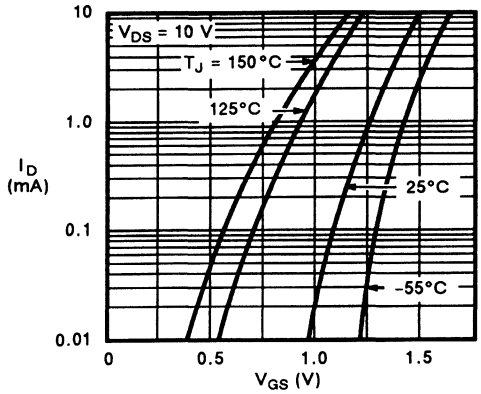
On-Resistance vs. Junction Temperature



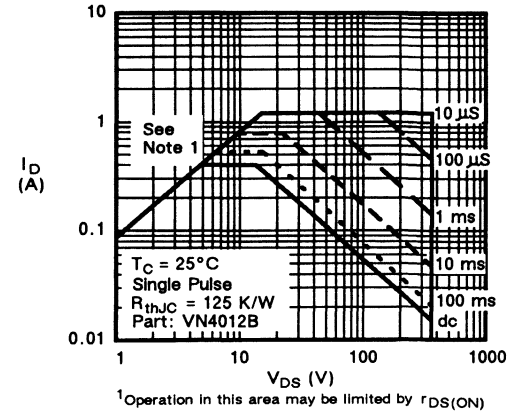
Source-Drain Diode Forward Voltage



Threshold Region



Safe Operating Area

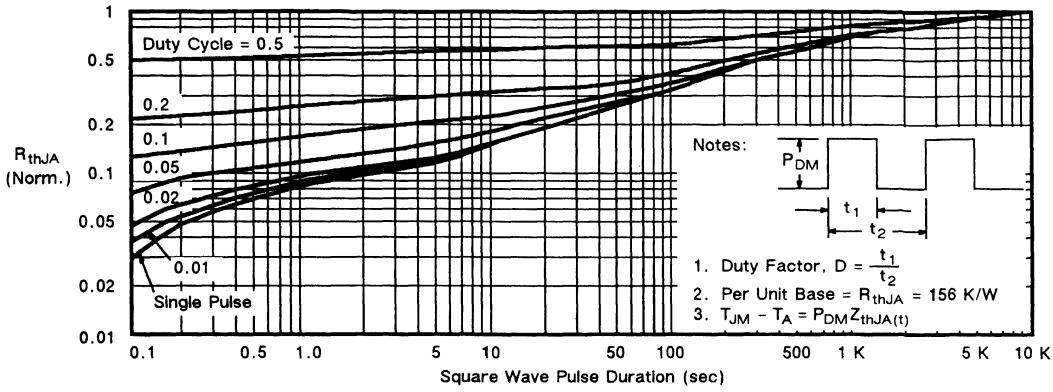


[1]Operation in this area may be limited by $r_{DS(ON)}$

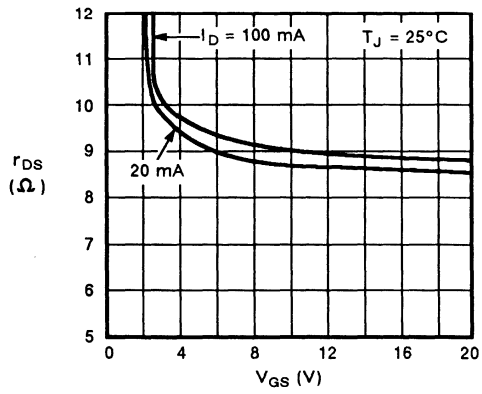
6

TYPICAL CHARACTERISTICS

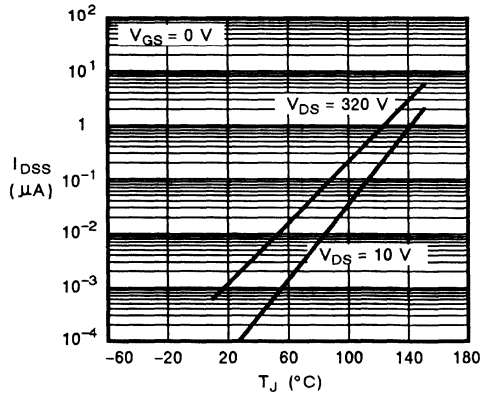
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



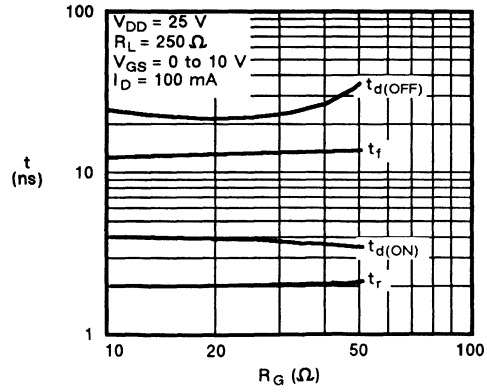
On-Resistance vs. Gate to Source Voltage



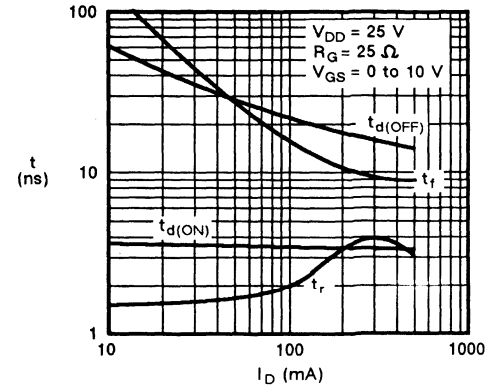
Off State Current



Drive Resistance Effects on Switching

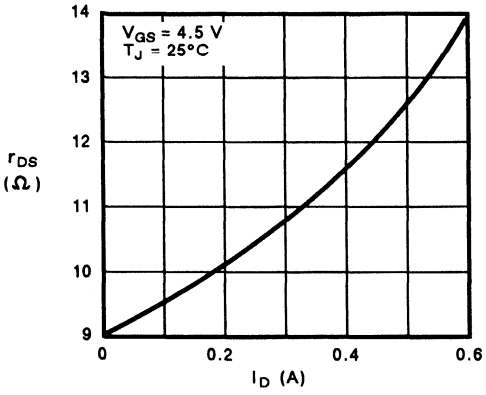


Load Condition Effects on Switching

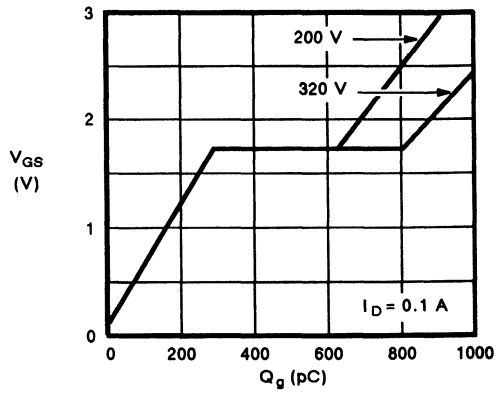


TYPICAL CHARACTERISTICS (Cont'd)

On-Resistance



Gate Charge



6

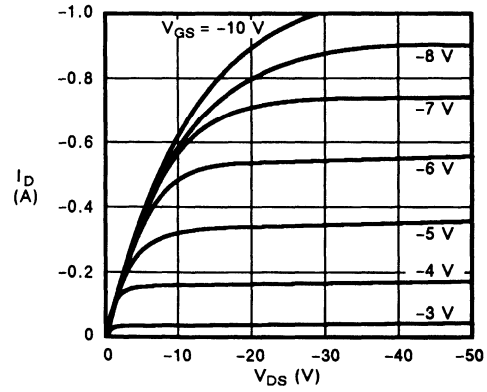
VPDQ20
P-Channel
Enhancement-Mode MOSFETs

Siliconix incorporated

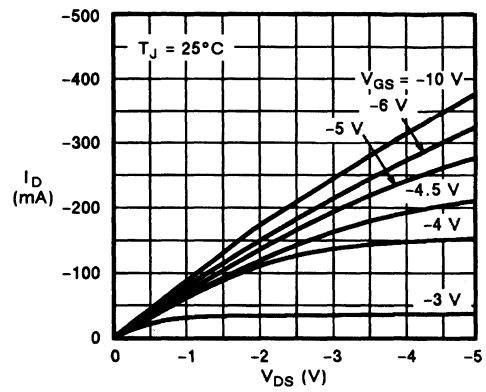
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• VP2020L, BSS92
Single	Chip	• Available as VPDQ1CHP

TYPICAL CHARACTERISTICS

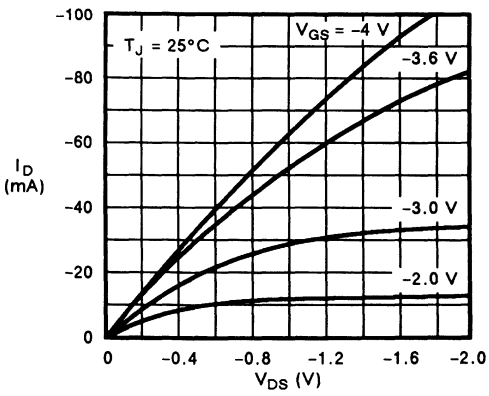
Output Characteristics



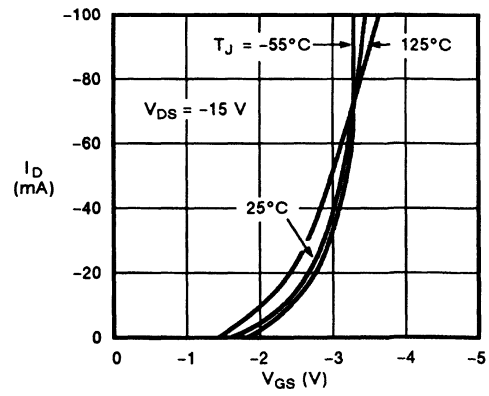
Ohmic Region Characteristics



Output Characteristics for Low Gate Drive



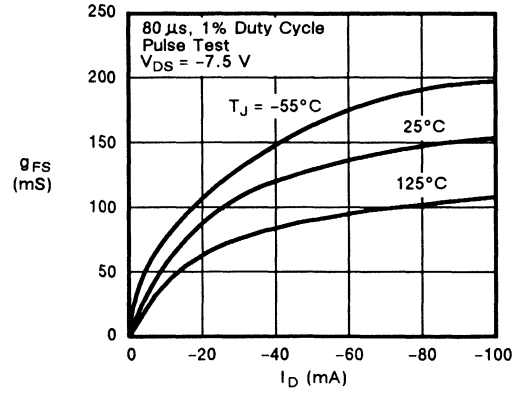
Transfer Characteristics



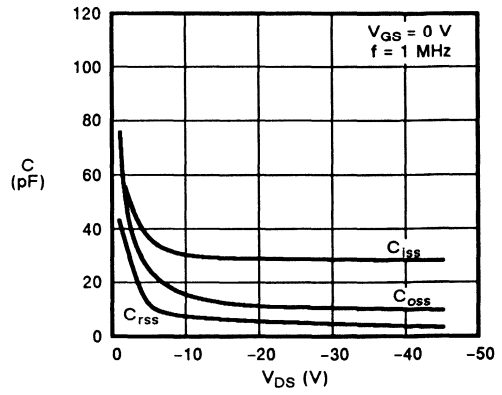
Revised (02/11/91)

TYPICAL CHARACTERISTICS

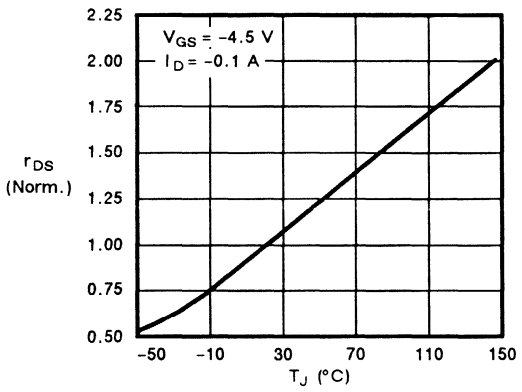
Transconductance



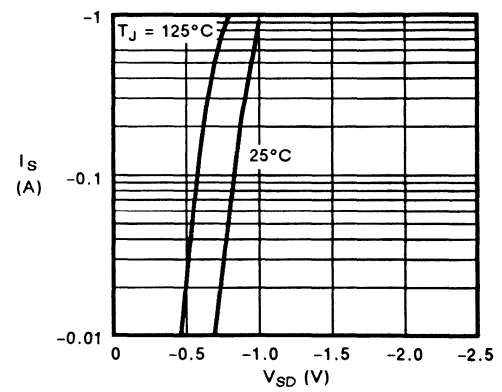
Capacitance



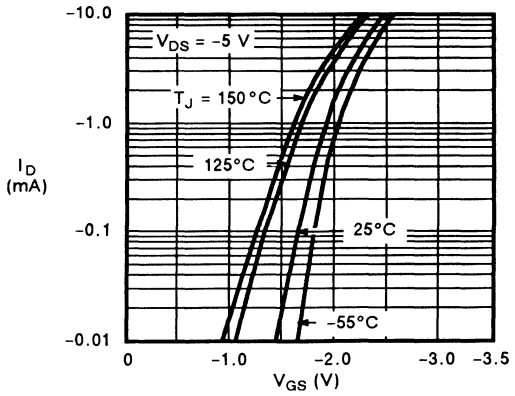
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



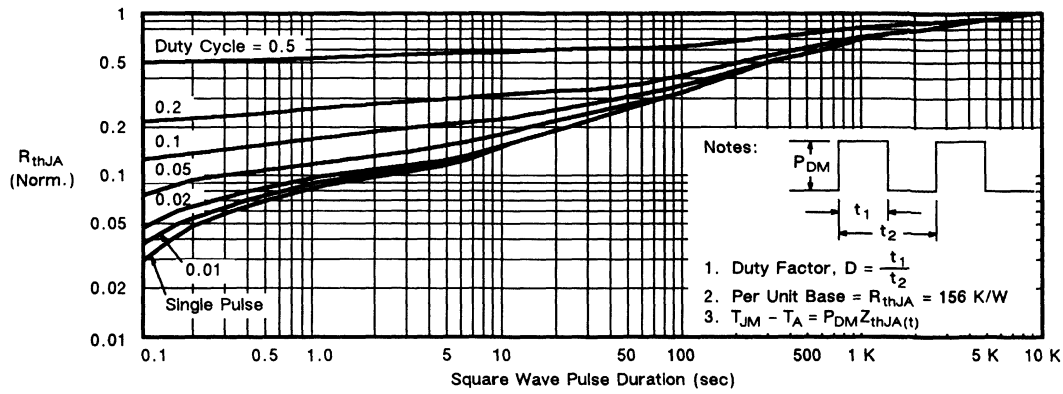
Threshold Region



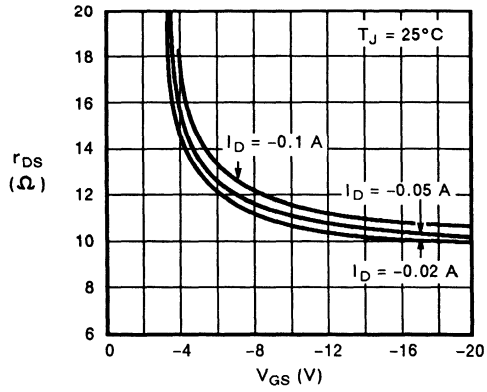
6

TYPICAL CHARACTERISTICS

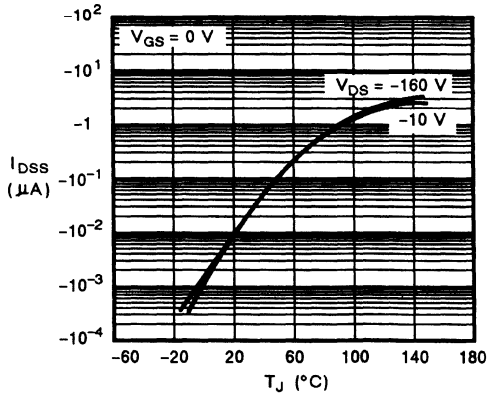
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



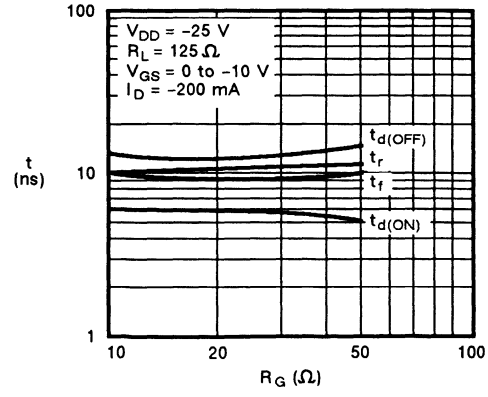
On-Resistance vs. Gate to Source Voltage



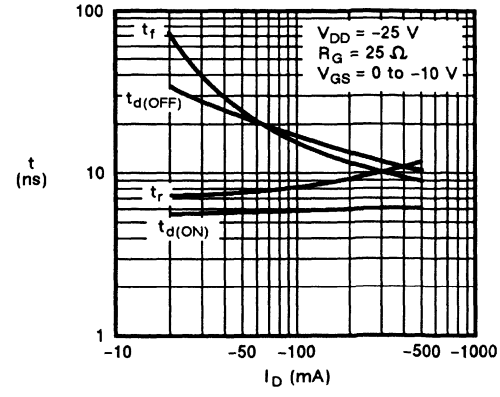
Off State Current



Drive Resistance Effects on Switching

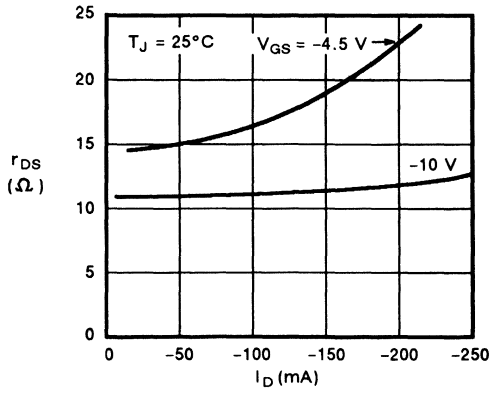


Load Condition Effects on Switching

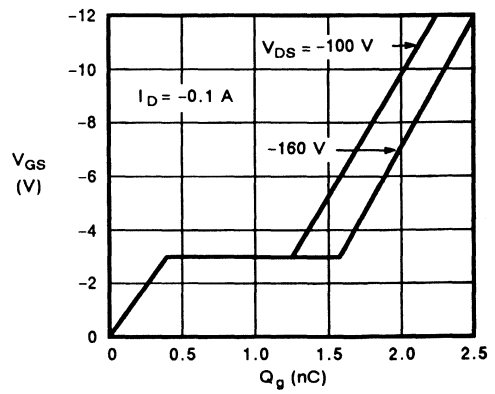


TYPICAL CHARACTERISTICS (Cont'd)

On-Resistance



Gate Charge



6

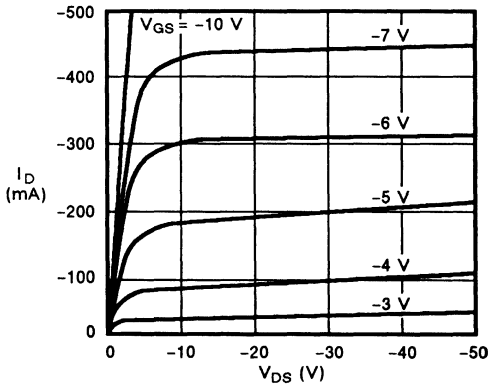
VPDS06
P-Channel
Enhancement-Mode MOSFET

Siliconix incorporated

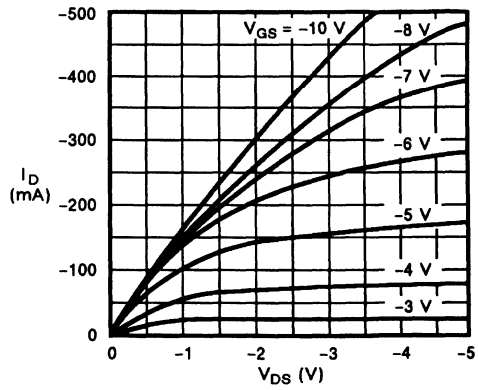
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• VP0610L, TP0610L
Single	SOT-23	• VP0610T, TP0610T
Single	Chip	• Available as VPDS1CHP

TYPICAL CHARACTERISTICS

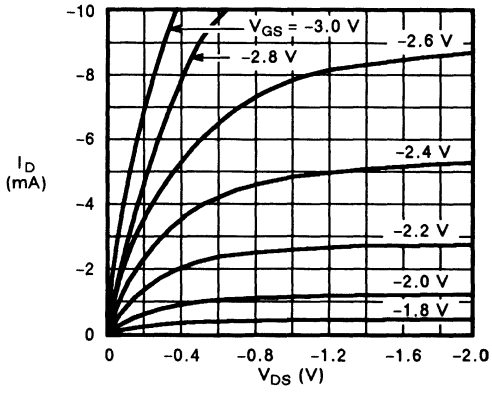
Output Characteristics



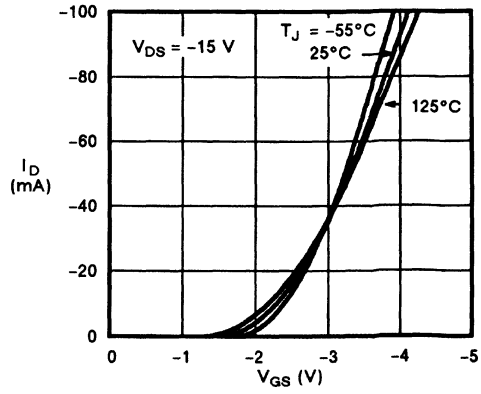
Ohmic Region Characteristics



Output Characteristics for Low Gate Drive



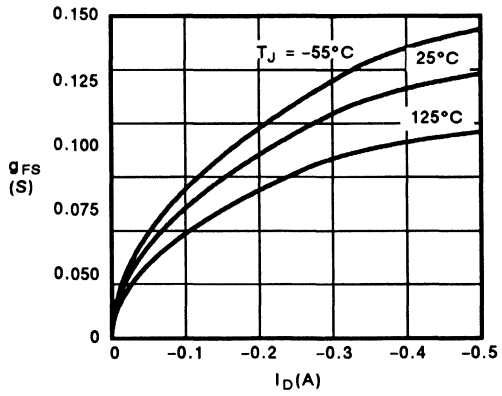
Transfer Characteristics



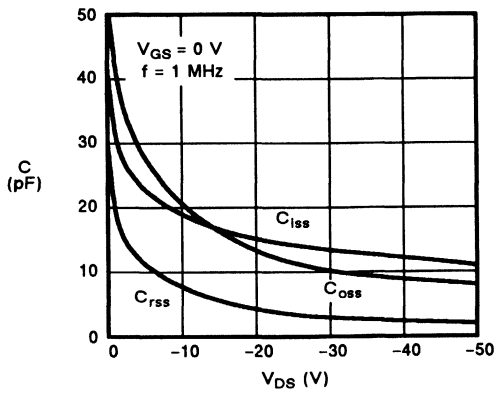
Revised (02/11/91)

TYPICAL CHARACTERISTICS

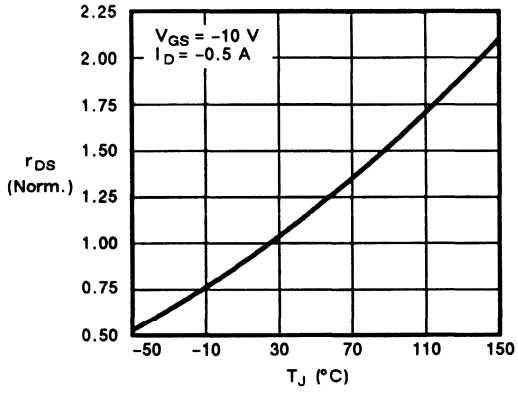
Transconductance



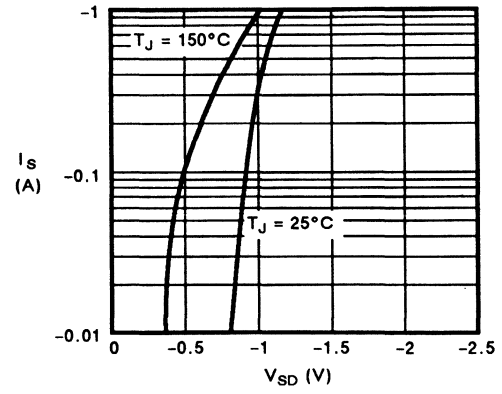
Capacitance



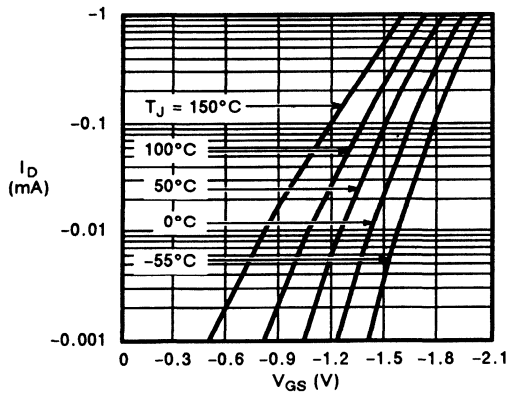
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



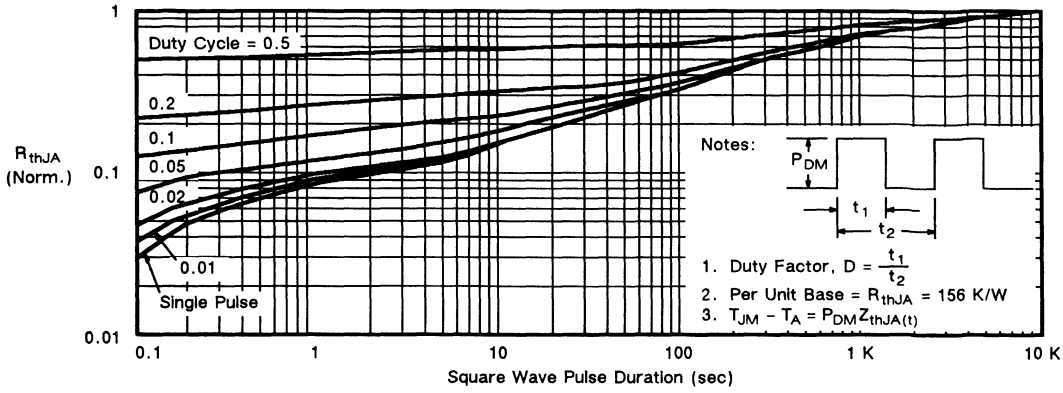
Threshold Region



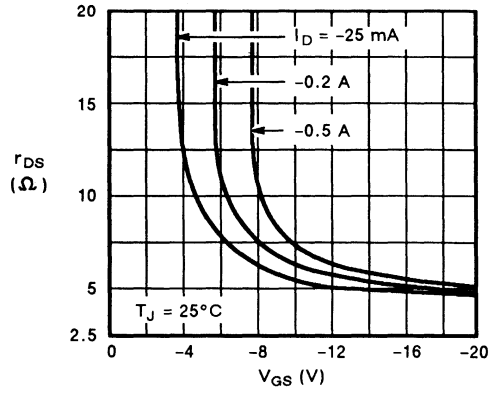
6

TYPICAL CHARACTERISTICS

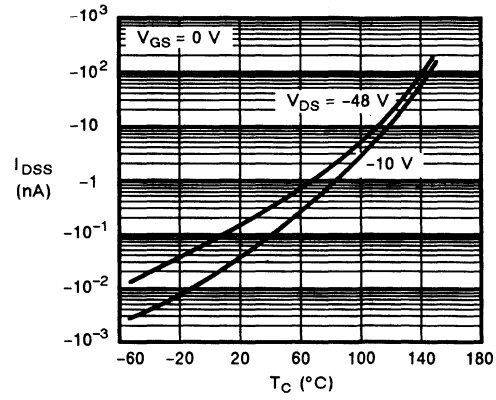
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



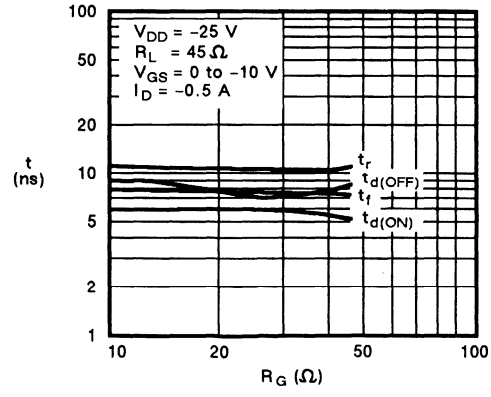
On-Resistance vs. Gate to Source Voltage



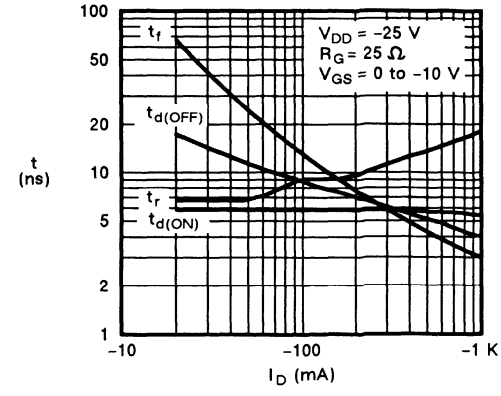
Off State Current



Drive Resistance Effects on Switching

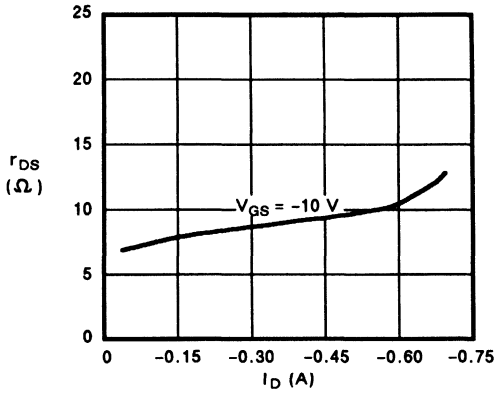


Load Condition Effects on Switching

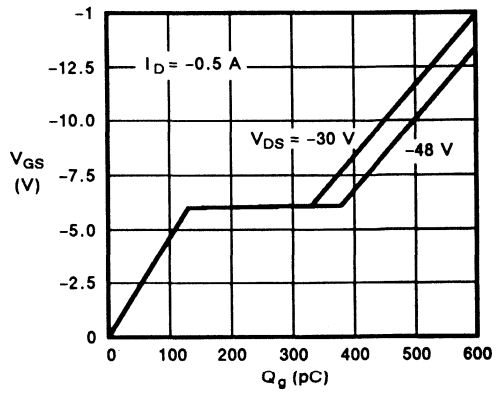


TYPICAL CHARACTERISTICS (Cont'd)

On-Resistance



Gate Charge



6

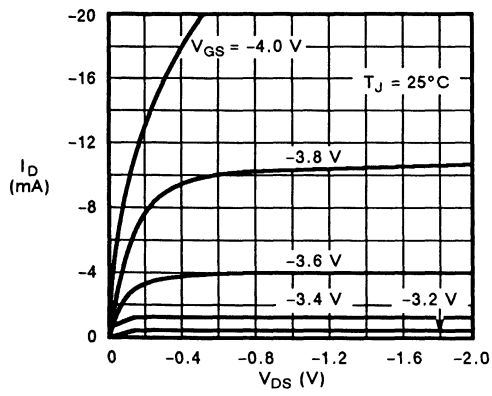
VPDV10
P-Channel
Enhancement-Mode MOSFETs

Siliconix incorporated

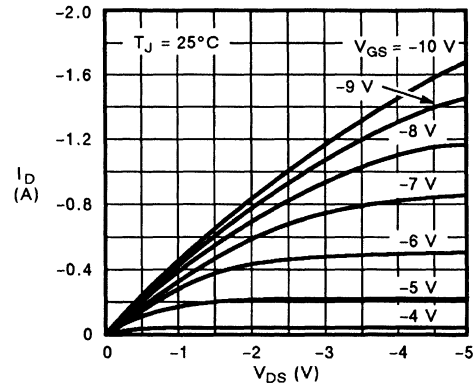
TYPE	PACKAGE	DEVICE
Single	TO-39 (TO-205AD)	• VP0808B, VP1008B
Single	TO-92 (TO-226AA)	• VP0808L, VP1008L
Single	TO-237	• VP0808M, VP1008M
Quad	14-Pin Plastic	• VQ2004J, VQ2006J
Quad	Chip	• Available as VPDV1CHP

TYPICAL CHARACTERISTICS

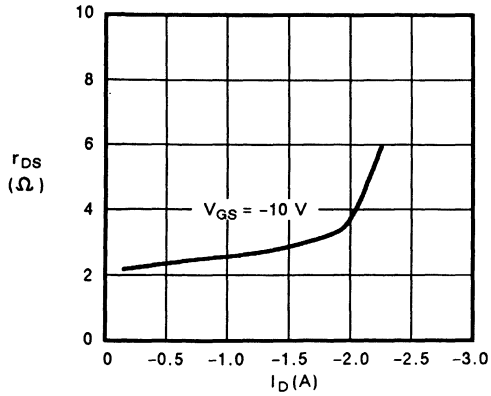
Output Characteristics for Low Gate Drive



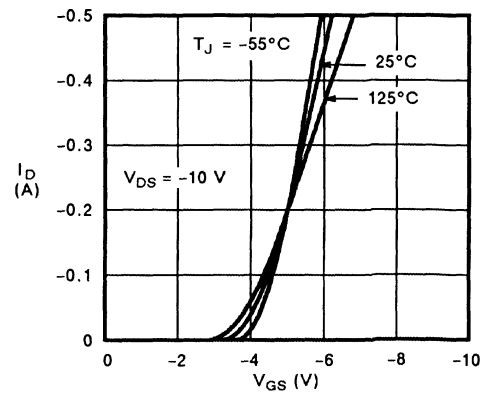
Ohmic Region Characteristics



On-Resistance



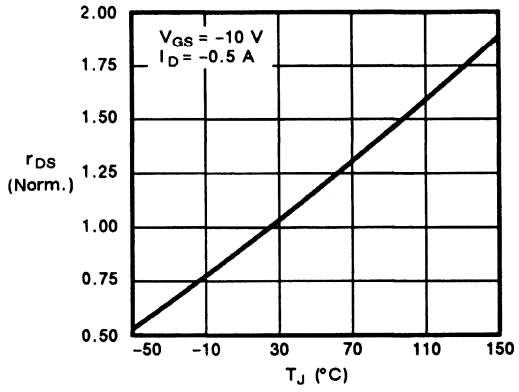
Transfer Characteristics



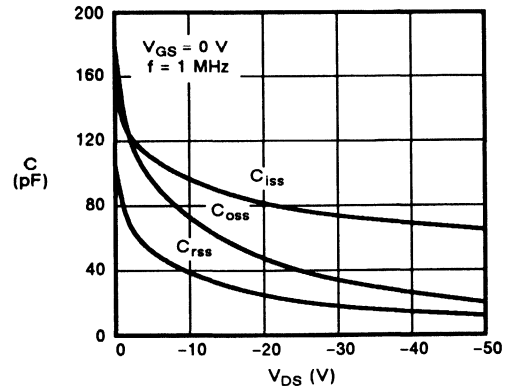
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

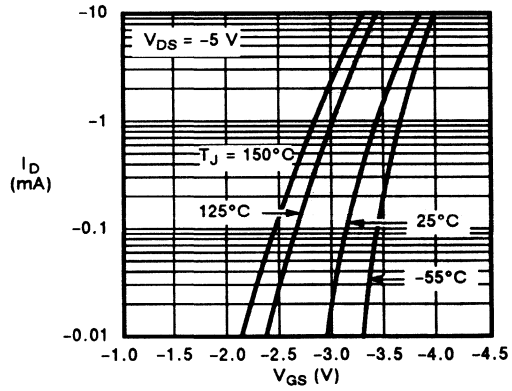
Normalized On-Resistance vs. Junction Temperature



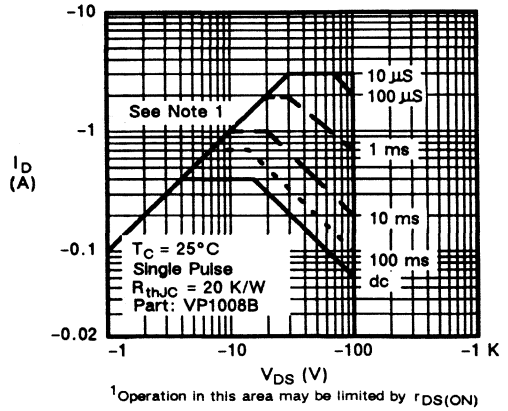
Capacitance



Threshold Region

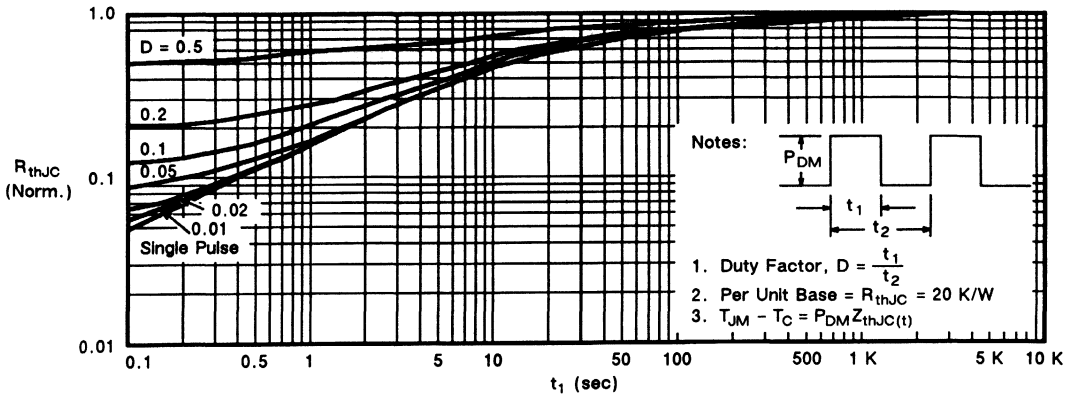


Safe Operating Area (VP1008B)



[1]Operation in this area may be limited by $r_{DS(ON)}$

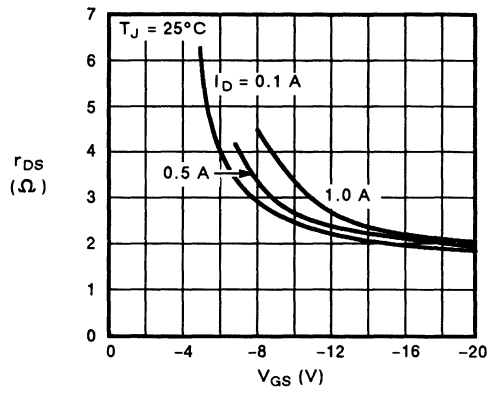
Normalized Effects Transient Thermal Impedance Junction-to-Case (TO-39)



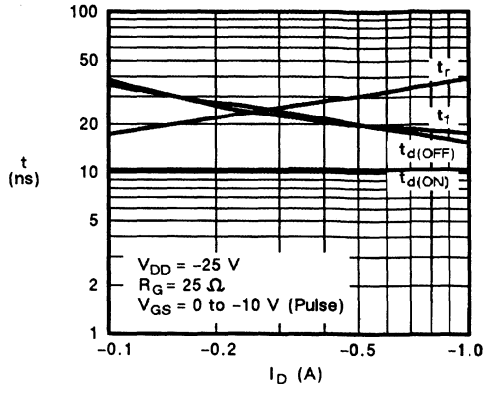
6

TYPICAL CHARACTERISTICS (Cont'd)

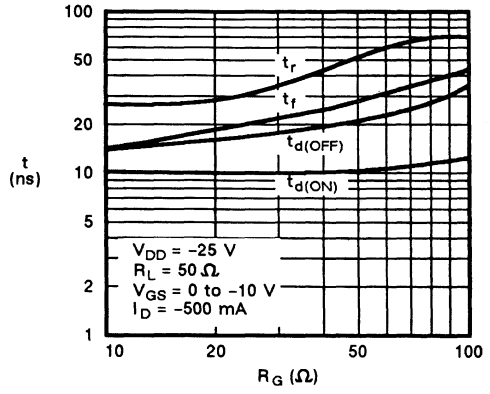
On-Resistance vs. Gate to Source Voltage



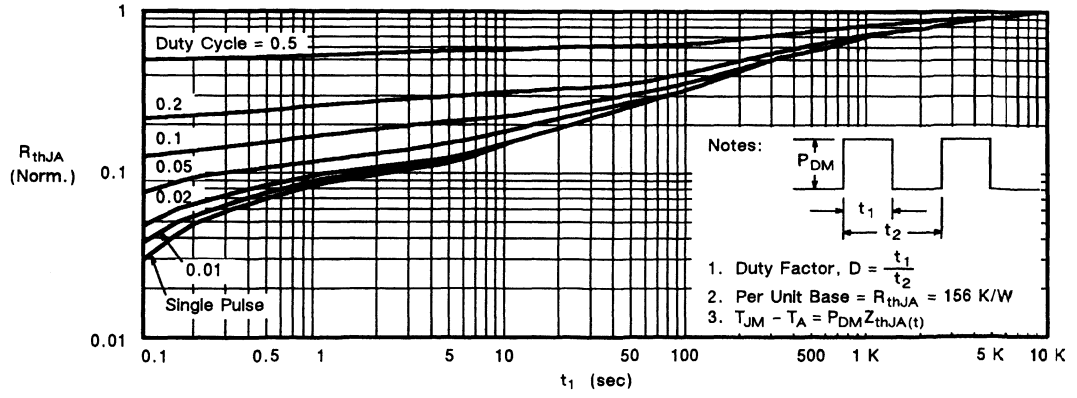
Load Condition Effects on Switching



Drive Resistance Effects on Switching

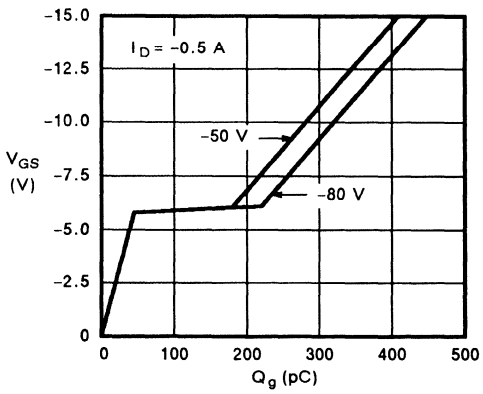


Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)

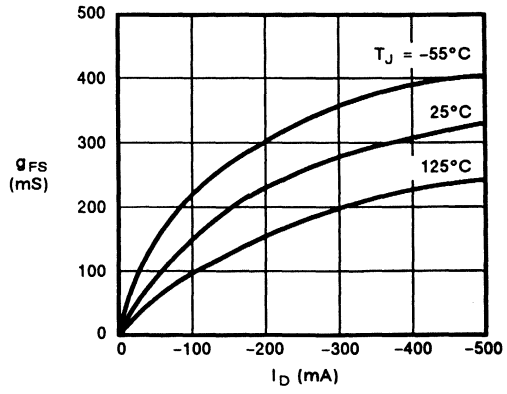


TYPICAL CHARACTERISTICS (Cont'd)

Gate Charge



Transconductance



6

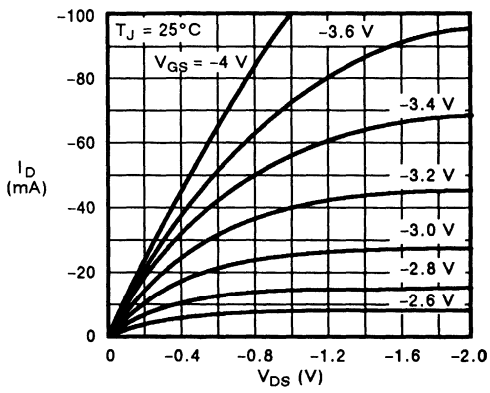
VPDV24
P-Channel
Enhancement-Mode MOSFETs

Siliconix incorporated

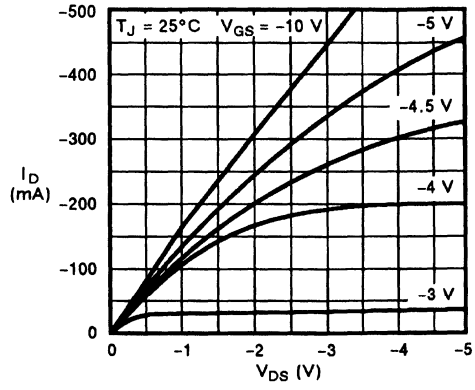
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• BS208 TP2410L, TP2010L VP2410L
Single	Chip	• Available as VPDV2CHP

TYPICAL CHARACTERISTICS

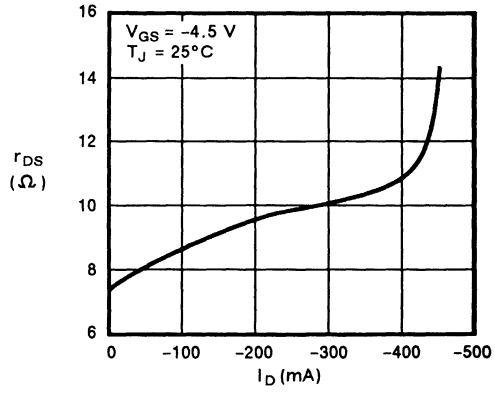
Output Characteristics for Low Gate Drive



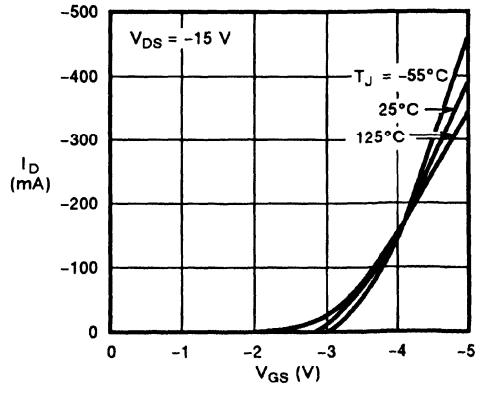
Ohmic Region Characteristics



On-Resistance



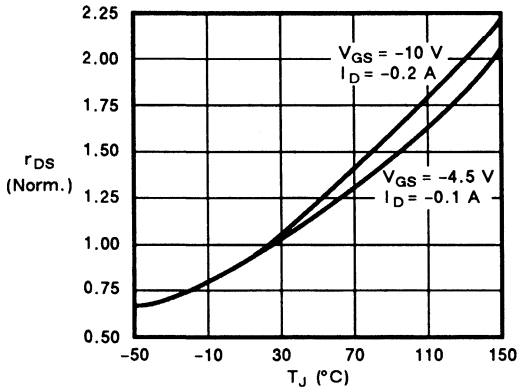
Transfer Characteristics



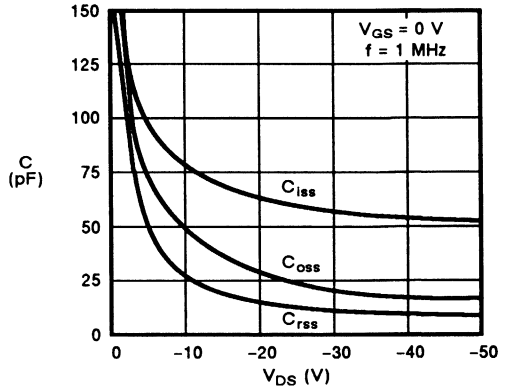
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

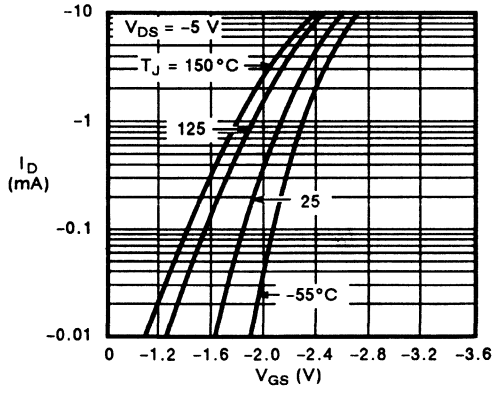
Normalized On-Resistance vs. Junction Temperature



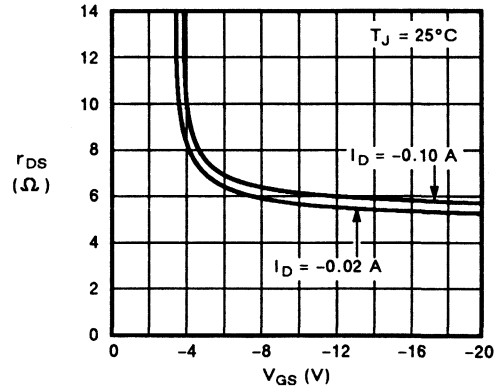
Capacitance



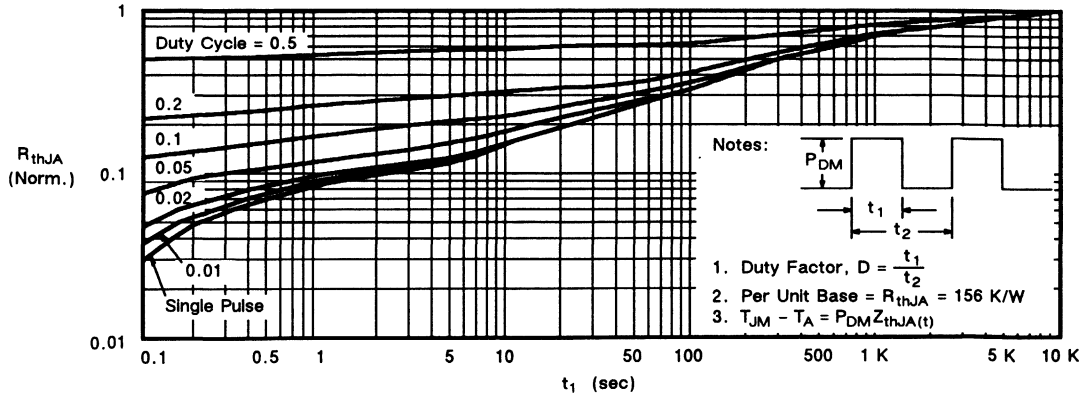
Threshold Region



On-Resistance vs. Gate to Source Voltage



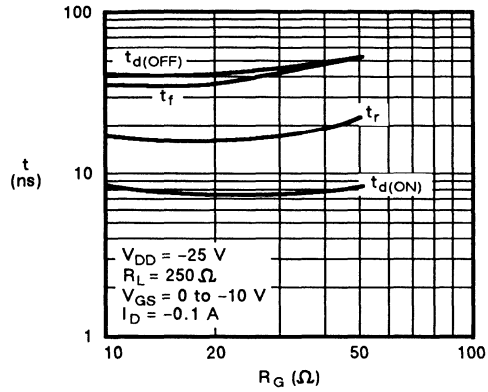
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



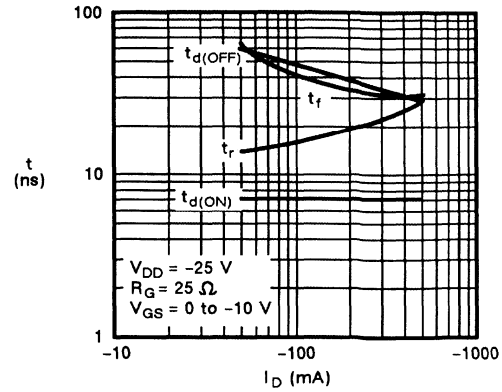
6

TYPICAL CHARACTERISTICS (Cont'd)

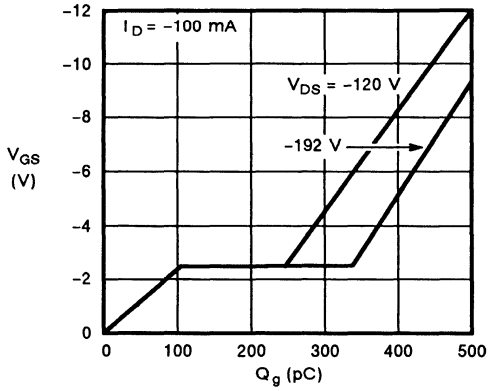
Drive Resistance Effects on Switching



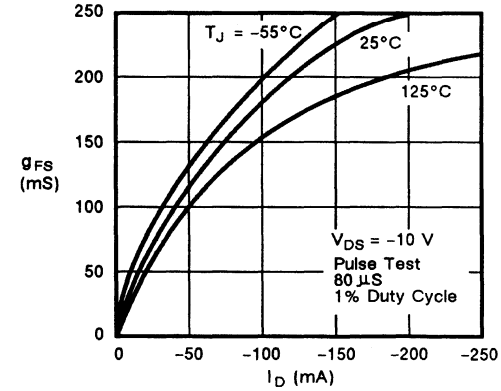
Load Condition Effects on Switching



Gate Charge

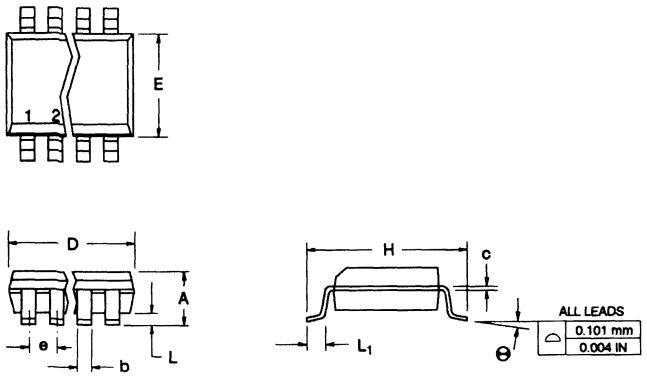


Transconductance



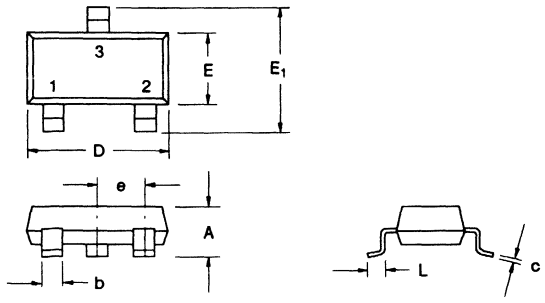
General Information
Cross Reference
Selector Guide
JFET
DMOS
Low Power MOS
Package Outlines 7
Applications
Publications Index
Worldwide Sales Offices and Distributors

■ SO Package (8, 14 Leads)



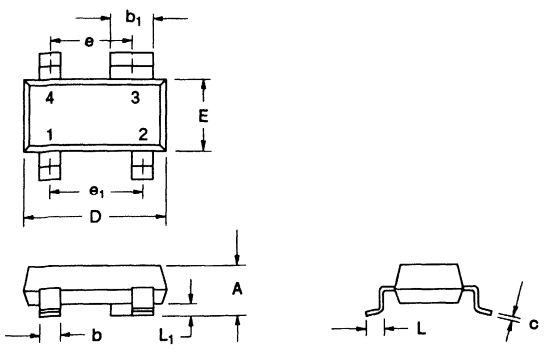
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
b	0.35	0.45	0.014	0.018
c	0.18	0.23	0.007	0.009
D-8	4.60	5.20	0.181	0.205
D-14	8.35	8.95	0.329	0.352
E	3.55	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.10	0.20	0.004	0.008
L_1	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

■ SOT-23



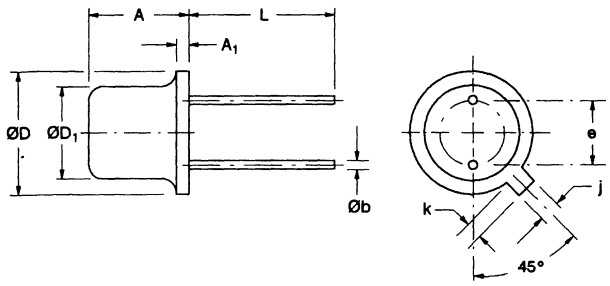
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.10	0.032	0.043
b	0.37	0.43	0.015	0.017
c	0.10	0.15	0.004	0.005
D	2.80	3.10	0.111	0.122
E	1.20	1.70	0.048	0.066
E_1	2.40	2.60	0.095	0.102
e	0.92	0.98	0.036	0.039
L	0.13	0.25	0.005	0.010

■ SOT-143



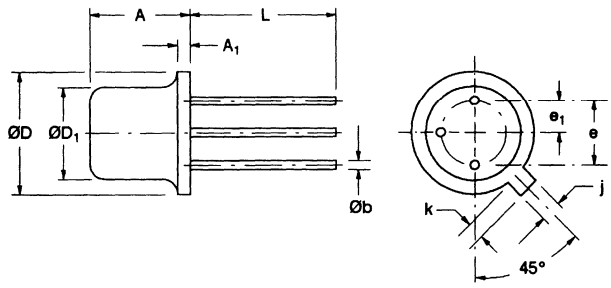
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.75	0.85	0.030	0.033
b	0.37	0.43	0.015	0.016
b_1	0.77	0.83	0.031	0.032
c	0.10	0.15	0.004	0.005
D	2.80	3.10	0.110	0.122
E	1.20	1.70	0.049	0.067
e	1.67	1.73	0.066	0.068
e_1	1.87	1.93	0.074	0.075
L	0.13	0.25	0.005	0.010
L_1	0.05	0.10	0.002	0.004

■ TO-18 (2 Leads)



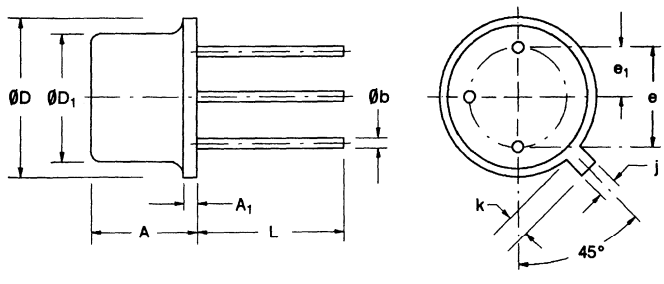
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
A_1	–	0.76	–	0.030
Øb	0.41	0.48	0.016	0.019
ØD	5.31	5.84	0.209	0.230
$ØD_1$	4.52	4.95	0.178	0.195
e	2.54 BSC		0.100 BSC	
j	0.92	1.17	0.036	0.046
k	0.72	1.22	0.028	0.048
L	12.70	–	0.500	–

■ TO-18 (TO-206AA, 3 Leads)



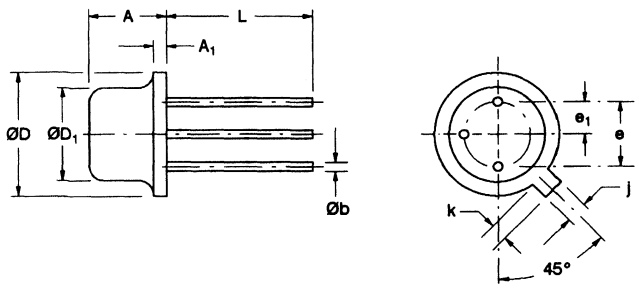
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
A_1	–	0.76	–	0.030
Øb	0.41	0.48	0.016	0.019
ØD	5.31	5.84	0.209	0.230
$ØD_1$	4.52	4.95	0.178	0.195
e	2.54 BSC		0.100 BSC	
e_1	1.27 BSC		0.050 BSC	
j	0.92	1.17	0.036	0.046
k	0.72	1.22	0.028	0.048
L	12.70	–	0.500	–

■ TO-39 (TO-205AD)



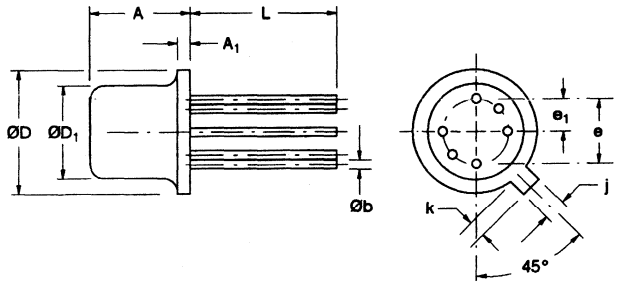
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
A_1	0.23	1.04	0.009	0.041
Øb	0.41	0.53	0.016	0.021
ØD	8.51	9.39	0.335	0.370
$ØD_1$	7.75	8.51	0.305	0.335
e	5.08 BSC		0.200 BSC	
e_1	2.54 BSC		0.100 BSC	
j	0.72	0.86	0.028	0.034
k	0.74	1.14	0.029	0.045
L	12.70	19.05	0.500	0.750

■ TO-52 (TO-206AC)



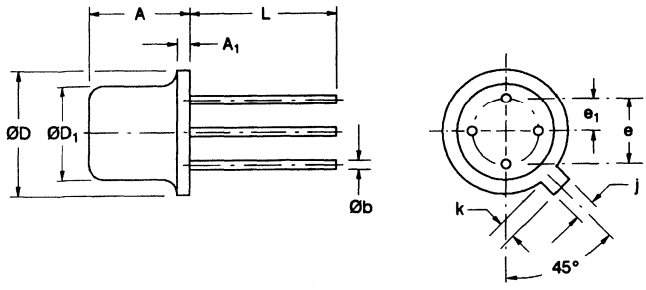
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.92	3.81	0.115	0.150
A_1	–	0.76	–	0.030
Øb	0.41	0.48	0.016	0.019
ØD	5.31	5.84	0.209	0.230
$ØD_1$	4.52	4.95	0.178	0.195
e	2.54 BSC		0.100 BSC	
e_1	1.27 BSC		0.050 BSC	
j	0.92	1.17	0.036	0.046
k	0.72	1.22	0.028	0.048
L	12.70	–	0.500	–

■ TO-71



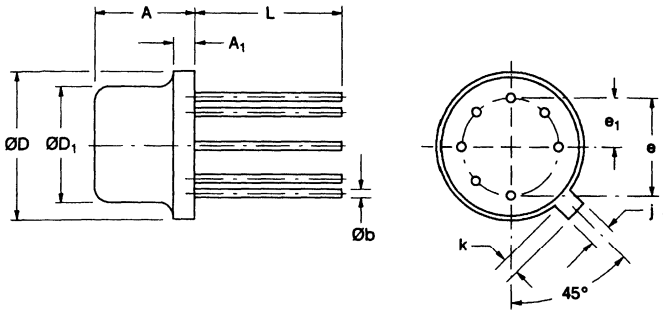
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
A_1	–	0.76	–	0.030
Øb	0.41	0.48	0.016	0.019
ØD	5.31	5.84	0.209	0.230
$ØD_1$	4.52	4.95	0.178	0.195
e	2.54 BSC		0.100 BSC	
e_1	1.27 BSC		0.050 BSC	
j	0.92	1.17	0.036	0.046
k	0.72	1.22	0.028	0.048
L	12.70	–	0.500	–

■ TO-72 (TO-206AF)



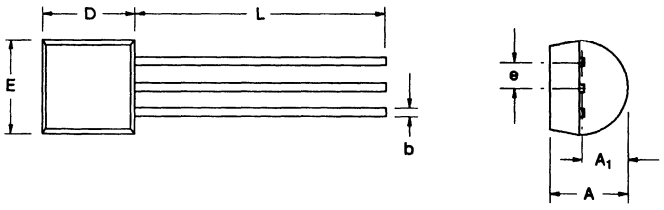
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
A_1	–	0.762	–	0.030
Øb	0.41	0.48	0.016	0.019
ØD	5.31	5.84	0.209	0.230
$ØD_1$	4.52	4.95	0.178	0.195
e	2.54 BSC		0.100 BSC	
e_1	1.27 BSC		0.050 BSC	
j	0.92	1.17	0.036	0.046
k	0.72	1.22	0.028	0.048
L	12.70	–	0.500	–

■ TO-78



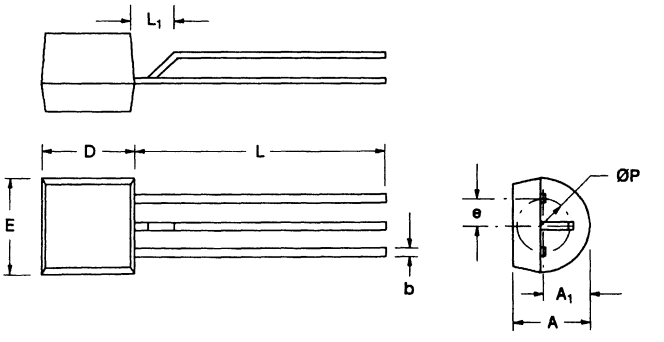
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.19	4.70	0.165	0.185
A_1	–	1.02	–	0.040
Øb	0.41	0.49	0.016	0.019
ØD	8.51	9.40	0.335	0.370
$ØD_1$	7.75	8.51	0.305	0.335
e	5.08 BSC		0.200 BSC	
e_1	2.54 BSC		0.100 BSC	
j	0.72	0.86	0.028	0.034
k	0.74	1.14	0.029	0.045
L	12.70	–	0.500	–

■ TO-92 (TO-226AA)



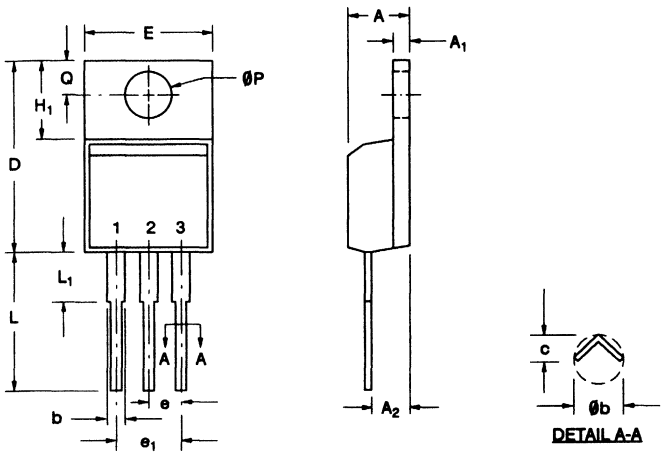
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.18	4.19	0.125	0.165
A_1	2.03	2.67	0.080	0.105
b	0.41	0.55	0.016	0.021
D	4.57	5.08	0.180	0.200
E	4.45	4.70	0.175	0.185
e	1.14	1.40	0.045	0.055
L	12.70	–	0.500	–

■ TO-92 (TO-226AA Lead Form -18)



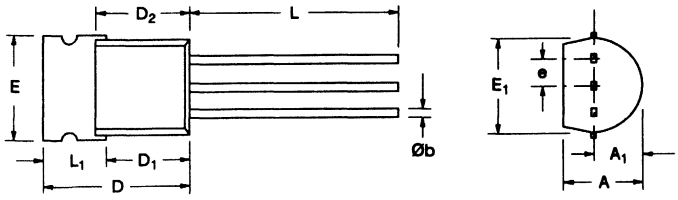
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.18	4.19	0.125	0.165
A_1	2.03	2.67	0.080	0.105
b	0.41	0.55	0.016	0.021
D	4.57	5.08	0.180	0.200
E	4.45	4.70	0.175	0.185
e	1.14	1.40	0.045	0.055
L	10.16	–	0.400	–
L_1	–	3.81	–	0.150
ØP	1.21	1.33	0.047	0.052

■ TO-220AB



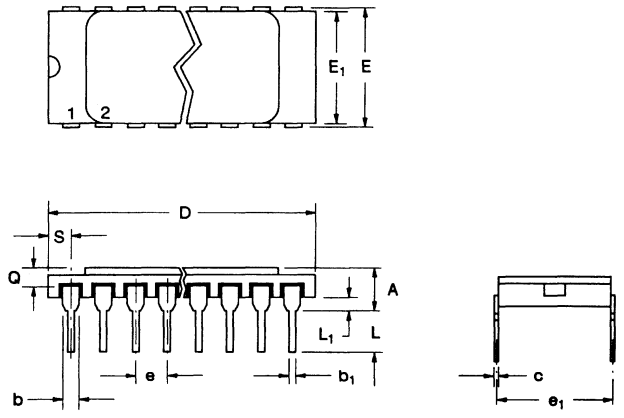
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.70	0.170	0.185
A_1	1.14	1.40	0.045	0.055
A_2	2.41	2.79	0.095	0.110
b	1.27	1.65	0.050	0.065
Øb	0.76	1.02	0.030	0.040
c	0.38	0.76	0.015	0.030
D	14.60	15.49	0.575	0.610
E	10.03	10.41	0.395	0.410
e	2.41	2.67	0.095	0.105
e_1	4.95	5.33	0.195	0.210
H	5.97	6.73	0.235	0.265
L	13.08	14.22	0.515	0.560
L_1	-	3.81	-	0.150
ØP	3.68	3.94	0.145	0.155
Q	2.54	3.05	0.100	0.120

■ TO-237



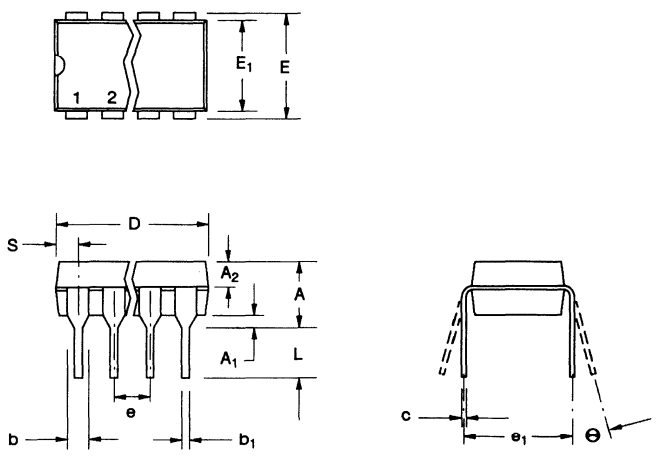
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.43	3.68	0.135	0.145
A_1	2.03	2.67	0.080	0.105
Øb	0.41	0.48	0.016	0.019
D	6.60	6.86	0.260	0.270
D_1	4.19 TYP		0.165 TYP	
D_2	4.45	4.70	0.175	0.185
E	4.95	5.21	0.195	0.205
E_1	4.45	4.70	0.175	0.185
e	1.14	1.40	0.045	0.055
L	12.70	-	0.500	-
L_1	2.41	2.67	0.095	0.105

■ Sidebraze DIP (14,16 Leads)

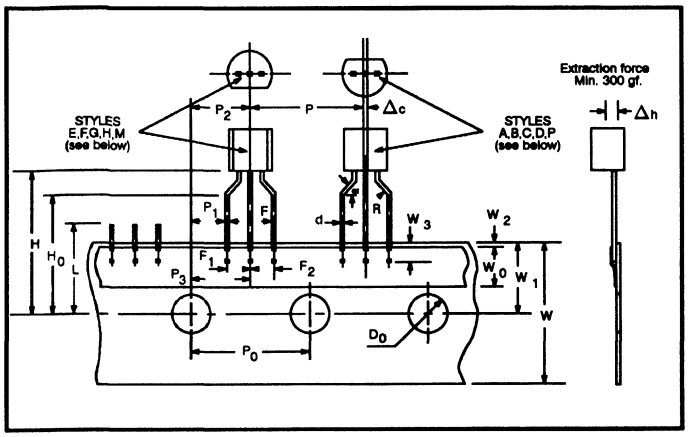


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.67	4.44	0.105	0.175
b	0.97	1.52	0.038	0.060
b_1	0.38	0.53	0.015	0.021
c	0.20	0.30	0.008	0.012
D-14	17.53	19.55	0.690	0.770
D-16	19.56	21.08	0.770	0.830
E	7.37	8.25	0.290	0.325
E_1	7.12	7.87	0.280	0.310
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.18	4.44	0.125	0.175
L_1	0.64	1.39	0.025	0.055
Q	0.25	-	0.010	-
S-14	0.77	2.41	0.030	0.095
S-16	0.51	1.65	0.020	0.065

■ Plastic DIP (14, 16 Leads)



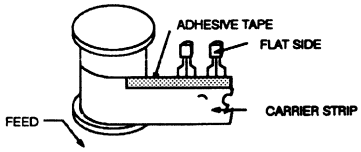
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-14	17.27	19.30	0.680	0.760
D-16	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	3.18	3.81	0.125	0.150
S-14	1.02	2.03	0.040	0.080
S-16	0.38	1.52	0.015	0.060
Θ	0°	15°	0°	15°



P	12.7 ± 1.0	F		5	$^{+0.8}_{-0.2}$
P_0	12.7 ± 0.2	$F_1 - F_2$			±0.3
P_1	3.85 ± 0.5	D_0			4 ± 0.2
P_2	6.35 ± 0.5	t			1.4
P_3	6.35	Δh			0 ± 1
W	18 $^{+0.5}_{-0.5}$	d	0.50	$^{+0.6}_{-0.5}$	dia.
W_0	6 ± 3	R			0.8
W_1	9 ± 0.5	α			45° - 60°
W_2	MAX 0.5	L			MIN 11
W_3	MIN 4.5	Δc			0 ± 0.5
H	18.5 $^{+3.0}_{-0.75}$				

OPTION 1

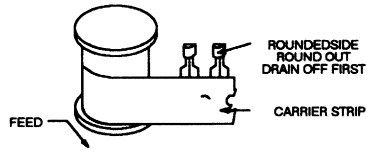
STYLE A IS PREFERRED



STANDARD TAPE & REEL FLAT OUT GATE OFF FIRST

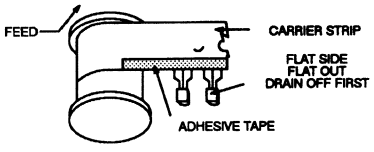
OPTION 3

STYLE A IS PREFERED



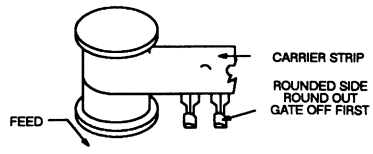
ROUNDED SIDE TRANSISTER AND ADHESIVE TAPE NOT VISIBLE

OPTION 2



FLAT SIDE OF TRANSISTER AND ADHESIVE TAPE VISIBLE

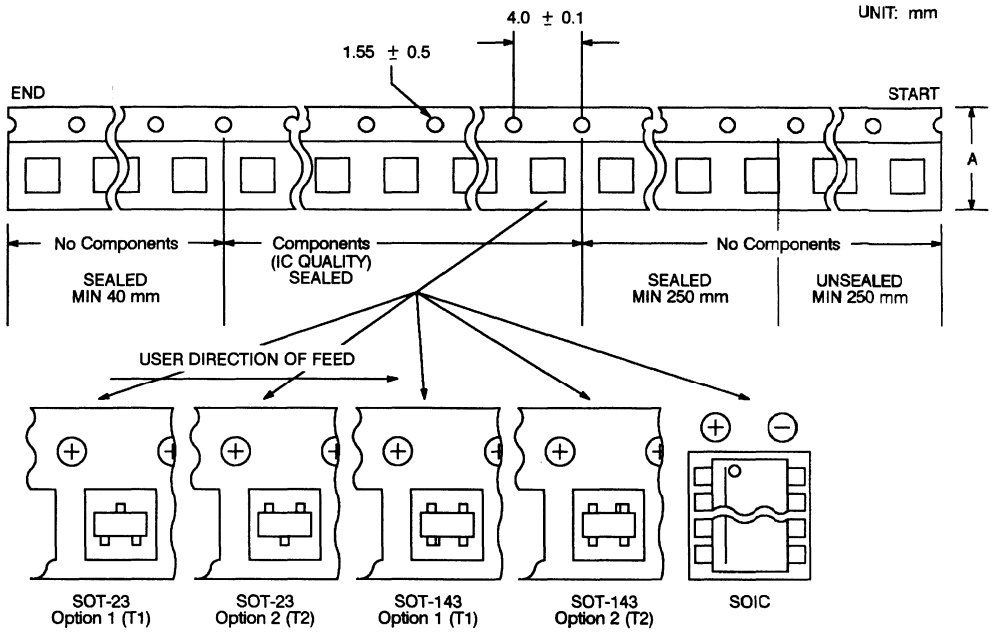
OPTION 4

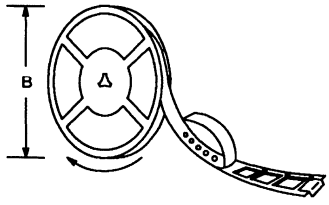


ROUNDED SIDE TRANSISTER AND ADHESIVE TAPE NOT VISIBLE

TO-92 TAPING SPECIFICATIONS AND WINDING STYLES

(ALL DIMENSIONS IN MILLIMETERS)





	A	B	C
SOT-23/SOT-143	8.0 ± 0.3 MIN	178 MIN	2500 EA
SOIC-8	12.0 ± 0.3	330	2500 EA
SOIC-14/SOIC-16	16.0 ± 0.3	330	2500 EA

SOT-23/143/SOIC TAPE AND REEL

General Information
Cross Reference
Selector Guide
JFETs
DMOS
Low Power MOS
Package Outlines
Applications 8
Publications Index
Worldwide Sales Offices and Distributors

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LPD-1

AN INTRODUCTION TO FETS

INTRODUCTION

The basic principle of the field-effect transistor (FET) has been known since J. E. Lilienfeld's patent of 1925. The theoretical description of a FET made by Shockley in 1952 paved the way for development of a classic electronic device which provides the designer the means to accomplish nearly every circuit function. At one time, the field-effect transistor was known as a "unipolar" transistor. The term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology, parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

Amplifiers
- Small Signal
- Low Distortion
- High Gain
- Low Noise
- Selective
- dc
- High-frequency

Current Limiters

Voltage-Controlled Resistors

Mixers

Oscillators

Switches
- Chopper-type
- Analog Gate
- Communicator

Protection Diodes
- Low-leakage

The family tree of FET devices (Figure 1) may be divided into two main branches, Junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, metal-oxide-silicon field-effect transistors). Junction FETs are inherently depletion-mode devices, and are available in both n- and p-channel configurations. MOSFETs are available in both enhancement and depletion modes, and also exist as both n- and p-channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.

Junction FETs

In its most elementary form, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased pn junction formed along the channel. Implicit in this description is the fundamental difference between JFET and bipolar devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The JFET is a high-input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes. n-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs tend to be more efficient conductors than their p-channel counterparts.

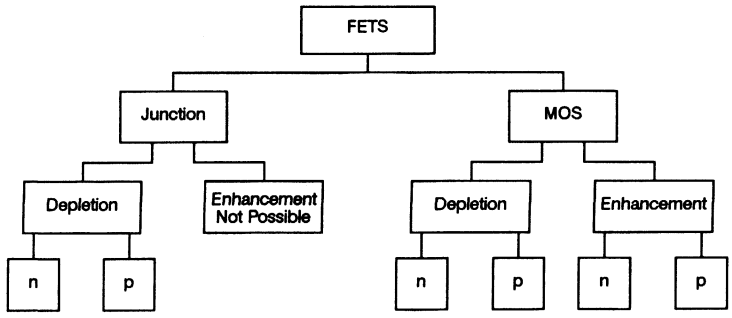


Figure 1. FET Family Tree

8

Junction FETs are particularly suited to manufacture by modern planar epitaxial processes. Figure 2 shows this process in an idealized manner. First, n-type silicon is deposited epitaxially (single-crystal condensation surface) onto monocrystalline p-type silicon, so that crystal integrity is maintained. Then, a layer of silicon dioxide is grown on the surface of the n-type layer, and the surface is etched so that an acceptor-type impurity can be diffused through into the silicon. The resulting cross-section is shown in Figure 2c, and demonstrates how a p-type annulus has been formed in the layer on n-type silicon. Figure 2d shows how a further sequence of oxide growth, etching, and diffusion can produce a channel of n-type material within the substrate.

In addition to the channel material, a JFET contains two ohmic (non-rectifying) contacts: the source and the drain. These are shown in Figure 2e. Since a symmetrical geometry is shown in the idealized JFET chip, it is immaterial which contact is called the source and which is called the drain; the JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.

(For certain JFET applications, such as amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged).

Figure 2e also shows how the n-channel is embedded in the p-type silicon substrate, so that the gate above the channel becomes part of this substrate. Figure 3 shows how the JFET functions. If the gate is connected to the source, then the applied voltage (V_{DS}) will appear between the gate and the drain. Since the pn junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away. The most depleted portion is in the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the n-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel. This limiting current is known as I_{DSS} (Drain-to-Source current with the gate shorted to the source). Figure 3b shows the almost complete depletion of the channel under these conditions.

Figure 3c shows the output characteristics of an n-channel JFET with the gate short-circuited to the

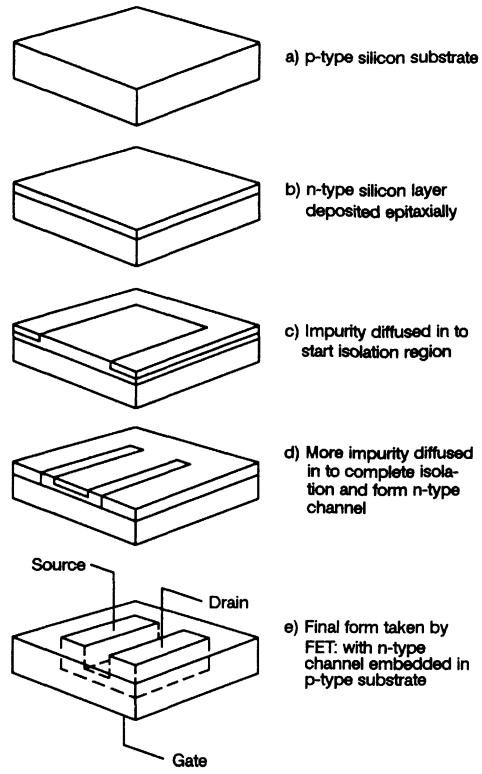


Figure 2. Idealized Manufacture of an n-channel Junction FET

source. The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases. The curve approaches the level of the limiting current I_{DSS} when I_D begins to be pinched off. The physical meaning of this term leads to one definition of pinch-off voltage, V_p, which is the value of V_{DS} at which the maximum I_{DSS} flows.

In Figure 4, consider the case where $V_{DS} = 0$ and where a negative voltage V_{GS} is applied to the gate. Again, a depletion layer has built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for $V_{GS} = 0$. In fact, at a value of $V_{GS} > V_p$ the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol V_p or by $V_{GS(off)}$. V_p has been widely used in the past, but $V_{GS(off)}$ is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off.

The mechanisms of Figures 3 and 4 react together to provide the family of output characteristics shown in Figure 5a. The area below the pinch-off voltage locus is known as the triode or "below pinch-off" region: the area above pinch-off is often referred to as the pentode or saturation region. JFET behavior in these regions is comparable to that of a power-grid vacuum tube, and for this reason JFETs operating in the saturation region make excellent amplifiers. Note that in the "below pinchoff" region both V_{GS} and V_{DS} control the channel current, while in the saturation region V_{DS} has little effect and V_{GS} essentially controls I_D.

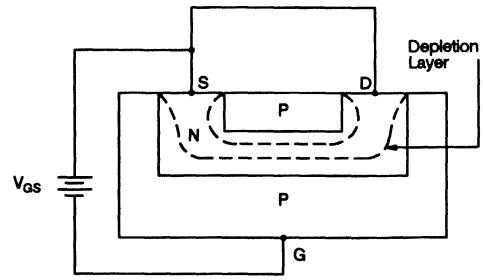
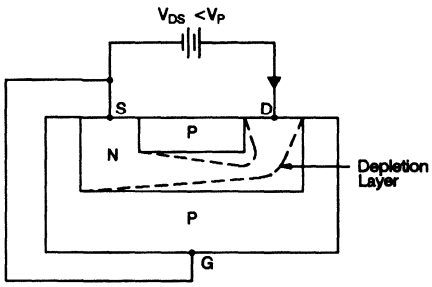
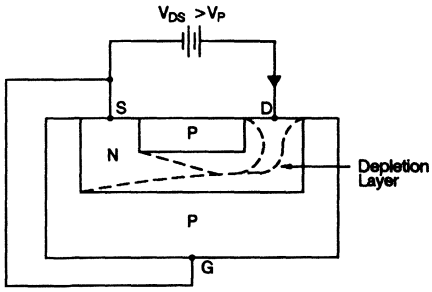


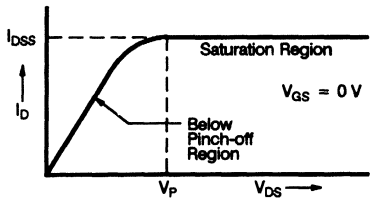
Figure 4. N-channel FET Showing Depletion Due to Gate-Source Voltage (V_{DS} = 0).



a) N-channel FET working below saturation (V_{GS} = 0). (Depletion shown only in channel region.)



b) N-channel FET working in saturation region (V_{GS} = 0).



c) Idealized output characteristic for V_{GS} = 0.

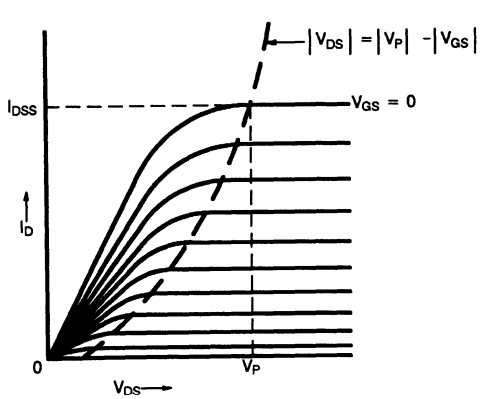
Figure 3.

Figure 5b relates the curves in Figure 5a to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS}. Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.

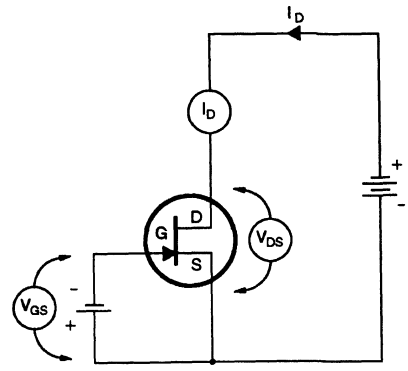
The p-channel JFET works in precisely the same way as the n-channel JFET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto n-type silicon, and the donor impurity diffused later to form a second n-type region and leave a p-type channel. In the p-channel JFET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow. Figure 6a shows the circuit arrangement for a p-channel JFET, and Figure 6b shows the output characteristics of the device. Note that the curves are shown in another quadrant than those of the n-channel JFET in order to stress the current directions and polarities involved.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS}. When V_{DS} is greater than V_p, the channel current is controlled largely by V_{GS} alone, because V_{GS} is applied to a reverse-biased junction. The resulting gate current is extremely small.

8

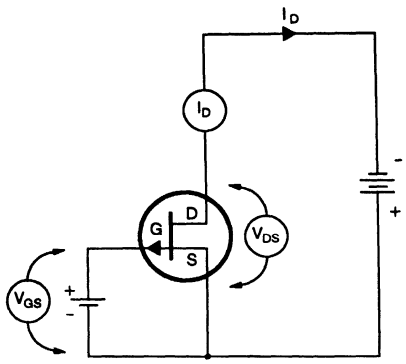


a) Family of output characteristics for n-channel FET

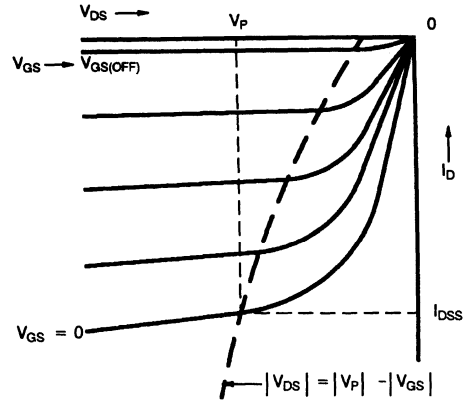


b) Circuit arrangement for n-channel FET

Figure 5.



a) Circuit arrangement for p-channel FET



b) Family of output characteristics for p-channel JFET

Figure 6.

MOSFETs

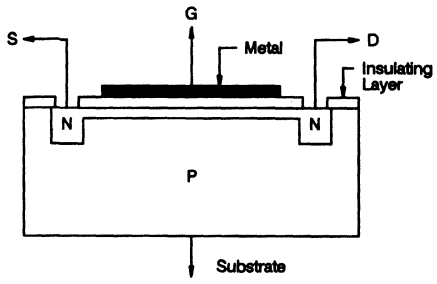
The metal-oxide-silicon FET (MOSFET) depends on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. On a MOSFET, the metallic or polysilicon gate is isolated from the channel by a thin layer of silicon dioxide (see Figure 7a). Although the bottom of the insulating layer is in contact with the p-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate in the interface, inverting the p-type material and spontaneously forming an n-type channel. Thus, a conduction path exists between the diffused n-type channel source and drain regions.

There are, however, some fundamental performance differences between MOSFETs and JFETS. JFETs, by nature, operate only in the depletion mode. That is, a reverse gate bias depletes, or pinches off the flow of channel current. A MOSFET, by virtue of its electrically-insulated gate, can be fabricated to perform as either a depletion-mode or enhancement-mode FET. Quite unlike the JFET, a depletion-mode MOSFET will also perform as an enhancement-mode FET.

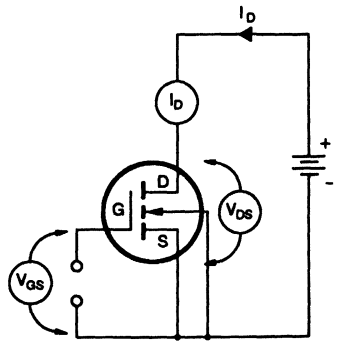
While the great majority of JFETs are fabricated in a manner similar to that shown in Figure 2, and operate as described in Figures 3 and 4, MOSFETs can assume several forms and operate in either the depletion/enhancement-mode or enhancement-mode only.

There are three types of small-signal MOSFETs. First, we have the planar, lateral MOSFET, similar to that shown in Figure 7a. By virtue of the n-doped channel spanning from source to drain, it performs as an n-channel depletion-mode MOSFET in a fashion not unlike that of the depletion-mode JFET when a voltage of the correct polarity is applied to the gate, as in Figure 7b. However, if we forward-bias the gate (that is, place a gate voltage whose polarity equals the drain voltage polarity) additional electrons will be attracted to the region beneath the gate, further enhancing - and inverting (from p to n) the region. As the channel region thickens, the channel resistance will further decrease, allowing greater channel current to flow beyond that identified as I_{DSS}, as we see in the family of output characteristics in Figure 7c.

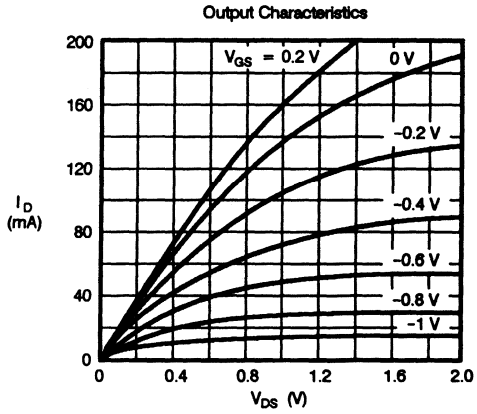
MOSFETs can also be constructed for enhancement-mode-only performance, as shown in Figure 8. Unlike the depletion-mode device, the enhancement-mode MOSFET offers no channel between the source and drain. Not until a forward bias on the gate enhances a channel by attracting electrons beneath the gate oxide will current begin to flow.



a) Idealized cross-section through an n-channel depletion-type MOSFET



b) Circuit arrangement for n-channel depletion MOSFET



c) Family of output characteristics for n-channel depletion MOSFET

Figure 7.

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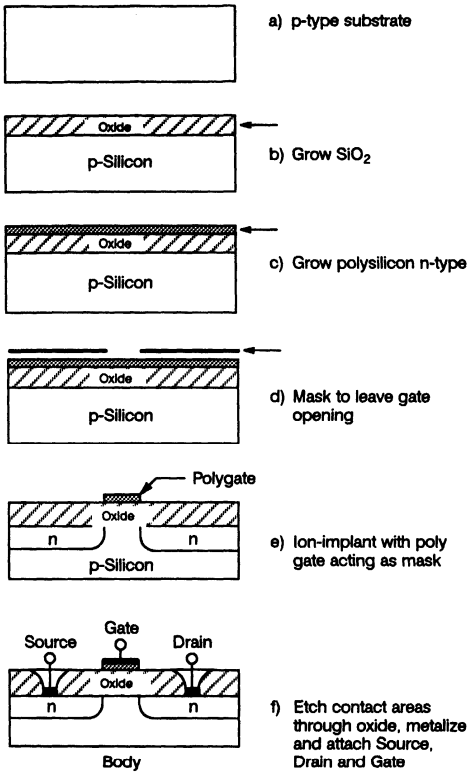

Figure 8. Fabrication of Planar Enhancement-Mode MOS

A newer MOSFET offering superior performance is the lateral double-diffused or DMOS FET. Because of the limitations of photo-lithographic masking, the earlier, older-style MOSFET was severely limited in performance. Some of these former limitations involved switching speeds, channel conductivity (too high an r_{DS}), and current handling in general. The lateral DMOS FET removed these limitations, offering a viable alternative between the JFET and the GaAs FET for video and high-speed switching applications.

The lateral DMOS FET differs radically in its channel construction when compared with the older planar MOSFET. A self-explanatory series-of-construction views of an n-channel, enhancement-mode device is shown in Figure 9. Note the double-diffused source implant into the implanted p-doped channel region, shown in Figures 9f and 9g. The improved the performance of DMOS is a result of both the precisely-defined short channel that results and the "drift region" resulting from the remaining p-doped silicon body and light n-doped ion implant, shown if Figures 9k and 9l.

Although Figures 8 and 9 illustrate the fabrication sequences for n-channel enhancement-mode DMOS FETs, by reversing the doping sequences, p-channel DMOS FETs can easily be fabricated. Furthermore, by lightly doping across the short channel and drift region, depletion-mode DMOS FETs can be constructed.

As a result of the short channel, the MOSFET is allowed to operate in "velocity saturation" and as a result of the drift region, the MOSFET offers higher operating voltages. Together, the short channel and the drift region offer low on-resistance and low interelectrode capacitances, especially gate-to-drain, V_{GD}.

Velocity saturation coupled with low interelectrode capacitance offers us high-speed and high-frequency performance.

The novelty of the short-channel DMOS FET led to the evolution of a yet more advanced, higher-voltage, higher-current MOSFET: the Vertical Double-Diffused MOSFET, shown in Figure 10. Where this vertical MOSFET offers improved power-handling capabilities, its fundamental shortcoming is that because of its construction and to a lesser extent because of its size, it fails to challenge the high-speed performance of the lateral DMOS FET. Consequently, the vertical and lateral DMOS FETs complement each other in a wide selection of applications.

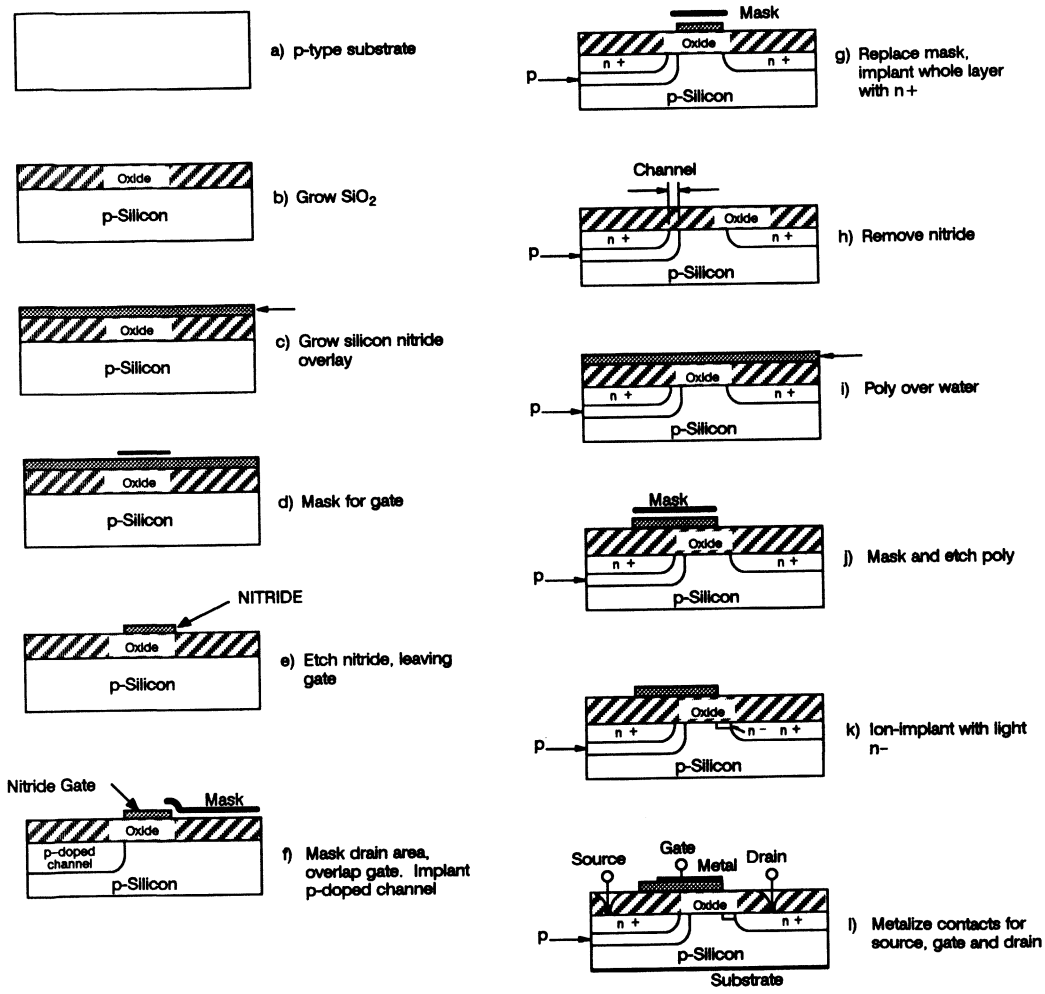

Figure 9. Fabrication of Planar Enhancement-mode DMOS

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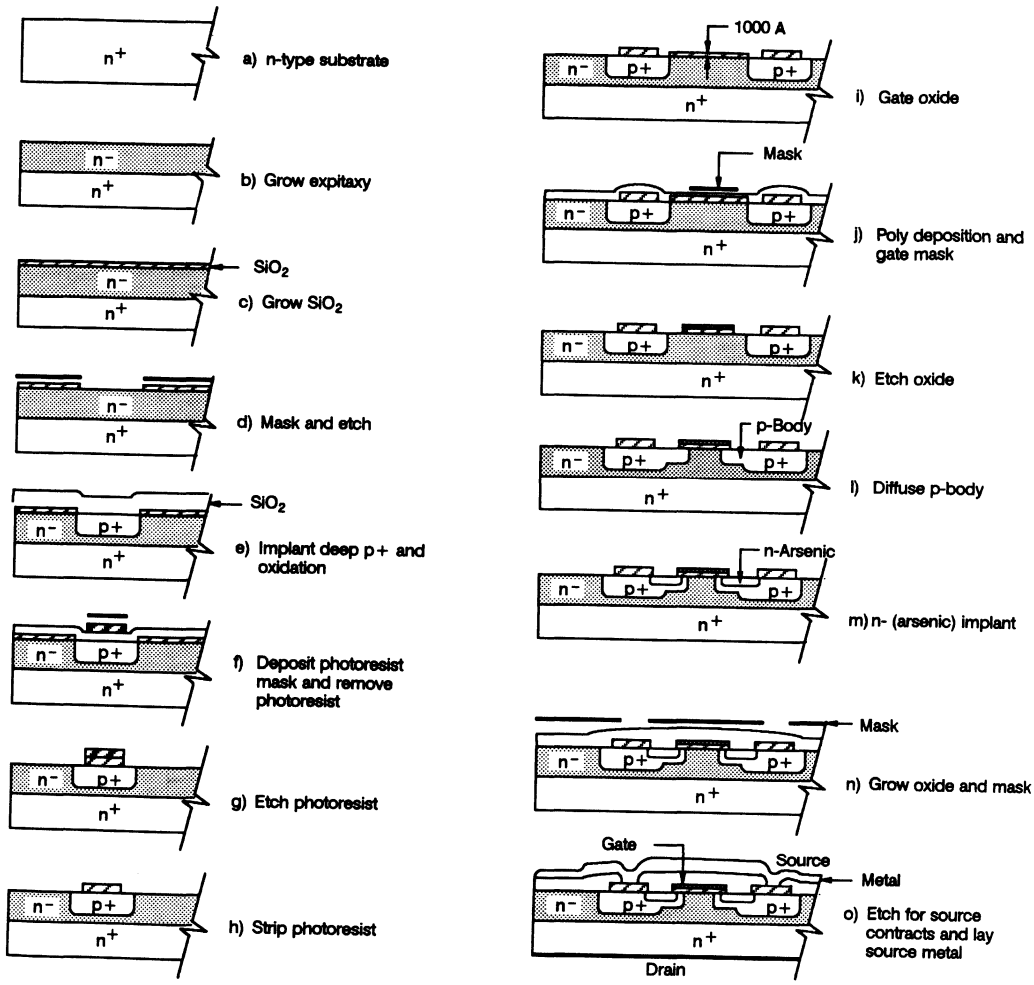

Figure 10. Vertical n-channel, Enhancement-mode DMOS FET

FET BIASING

INTRODUCTION

Engineers who are not familiar with proper biasing methods often design FET amplifiers that are unnecessarily sensitive to device characteristics.

One way to obtain consistent circuit performance, in spite of device variations, is to use a combination of constant voltage and self biasing. The combined circuit configuration turns out to be the same as that generally used with bipolar transistors, but its operation and design are quite different.

Three Basic Circuits

Let's examine three basic common-source circuits that can be used to establish a FET's operating point (Q-point) and then see how two of them can be combined to provide greatly improved performance. The three basic biasing schemes are:

- Constant-voltage bias, which is most useful for rf and video amplifiers employing small dc drain resistors.
- Constant-current bias, which is best suited to low-drift dc amplifier applications such as source followers and source-coupled differential pairs.
- Self bias (also called source bias or automatic bias), which is a somewhat universal scheme particularly valuable for ac amplifiers.

The Q-point established by the intersection of the load line and the V_{GS} = -0.4 V output characteristic of Figure 1 provides a convenient starting point for the circuit comparison. The load line shows that a drain supply voltage, V_{DD}, of 30 V and a drain resistance, R_D, of 39 kΩ are being used.

The quiescent drain-to-source voltage, V_{DSQ}, is 15 V, allowing large signal excursions at the drain. Maximum input signal variations of ±0.2 V will produce output voltage swings of ±7.0 V, a voltage gain of 35.

The constant-voltage bias circuit (Figure 2) is analyzed by superimposing a line for V_{GG} = constant on the transfer characteristic of the FET.

The transfer characteristic is a plot of I_D vs. V_{GS} for constant V_{DS}. Since the curve doesn't change much with changes in V_{DS}, it is useful in establishing operating bias points. In fact, it is probably more useful than the output characteristics because its curvature clearly warns of the distortion to be expected with large input signals. Furthermore, when a bias load line is superimposed, allowable signal excursions become evident, and input voltage, gate-source signal voltage, and output signal current calculations may be made graphically.

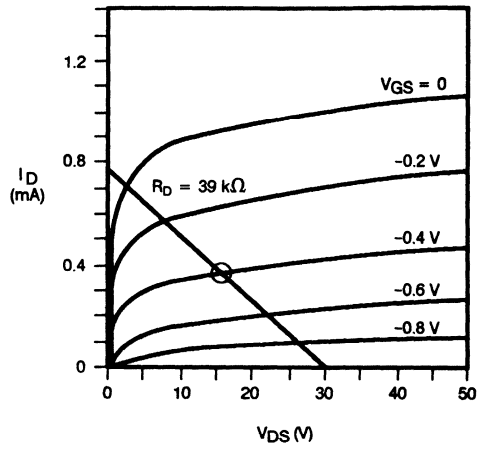

Figure 1. A large dynamic range is provided by the operating point at V_{DSQ} = 15 V, I_{DQ} = 0.39 mA, and V_{GSQ} = -0.4 V.

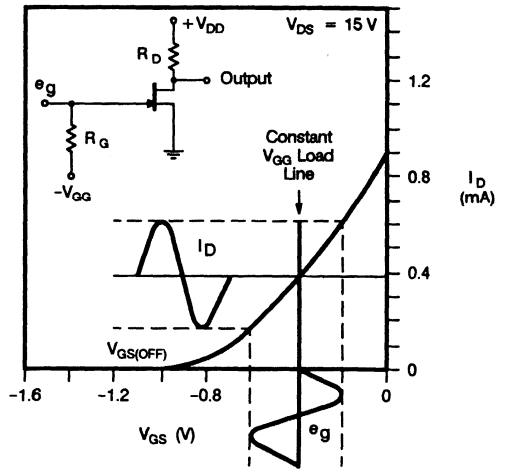

Figure 2. Constant-voltage bias is maintained by the V_{GG} supply as shown on this typical transfer curve. Input signal e_g moves the load line horizontally.

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The heavy vertical line at V_{GS} = -0.4 V establishes the Q-point of Figure 1. No voltage is dropped across resistor R_G because the gate current is essentially zero. R_G serves mainly to isolate the input signal from the V_{GG} supply.

Excursions of the input signal, e_g, combine in series with V_{GS} so that they add algebraically to the fixed value of -0.4 V. The effect of signal variation is to instantaneously shift the bias line horizontally without changing its slope. The shifting bias line then develops the output signal current as shown in Figure 2.

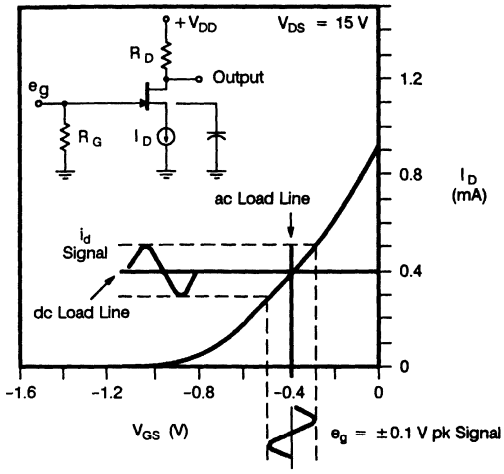

Figure 3. Constant-current bias fixes the output voltage for any R_D. Hence, input signals cannot affect the output unless the current source is bypassed.

The constant-current bias approach (Figure 3) for establishing the Q-point of Figure 1 requires a 0.39-mA current source. For an ideal constant-current generator, input signal excursions merely shift the bias line horizontally and produce no gate-source voltage excursion. This bias technique is therefore limited to source followers, source coupled differential amplifiers, and ac amplifiers where the source terminal is bypassed to ground at the signal frequency.

If an ac ground is provided by a bypass capacitor across the current source, a vertical ac bias line will be established. Input signal variations will then translate the ac bias line horizontally, and signal development will proceed as with constant-voltage biasing (Figure 3).

Should the bypass capacitor not provide a sufficiently low reactance at the signal frequency, the ac bias line will not be be vertical. It will still intersect the transfer curve at the Q-point but with a slope equal to $-(1/X_C) = -\omega C$ (Figure 4).

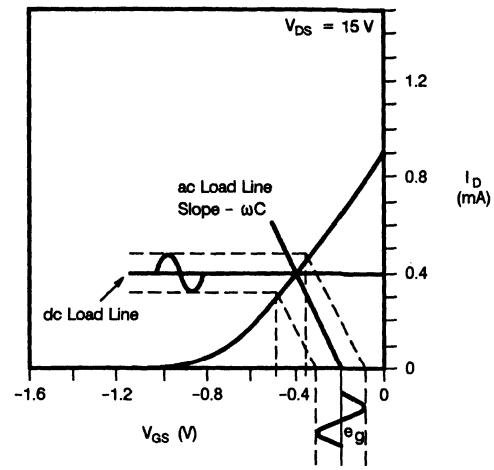

Figure 4. Partial bypassing of the current source (Figure 3) lowers the circuit gain by tilting the ac load line from the vertical. The capacitor drop subtracts from e_g.

This will lower the gain of the amplifier because of signal degeneration at the source. The input signal, e_g, is reduced by the drop across the capacitor:

$$V_{GS} = e_g - V_S = e_g - i_S X_C \qquad (1)$$

It is clear from Figure 4 that the input signal shifts the operating point only by an amount equal to V_{GS}, the effective input signal. As the signal frequency is decreased, the slope of the ac bias line decreases, causing the effective input signal to approach zero.

Self-Bias Needs No Extra Supply

The self-bias circuit (Figure 5) establishes the Q-point by applying the voltage dropped across the source resistor, R_S, to the gate. Since no voltage is dropped across R_S when I_D = 0, the self-bias load line passes through the origin. Its slope is given by $-1/R_S = I_{DQ}/V_{GSQ}$.

Signal development is the same as in the case of the partially bypassed constant-current scheme except that the load line is a dc bias line. Signal degeneration is described by Equation 1 with X_C replaced by R_S. The ac gain of the circuit can be increased by shunting R_S with a bypass capacitor, as in the constant-current case. The ac load line then passes through the Q-point with a slope $-(1/Z_S = -(\omega C + 1/R_S)$.

The circuit is biased automatically at the desired Q-point, requiring no extra power supply, and providing a degree of current stabilization not possible with constant-voltage biasing.

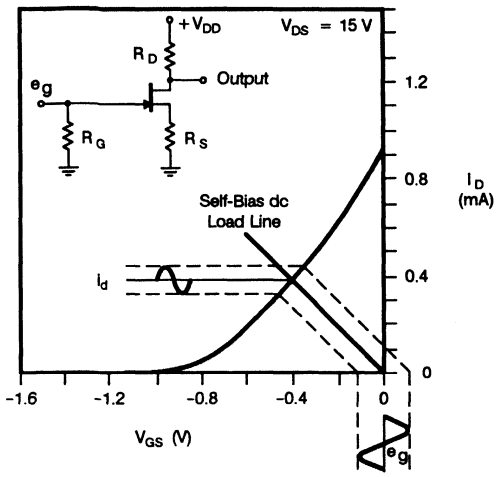

Figure 5. The self-bias load line passes through the origin with a slope $-1/R_S$. Bypassing R_S will steepen the slope and increase the gain of the circuit.

A fourth biasing method, combining the advantages of constant-current biasing and self biasing, is obtained by combining the constant-voltage circuit with the self-bias circuit (Figure 6). A principal advantage of this configuration is that an approximation may be made to constant-current bias without any additional power supply. The bias load line may be drawn through the selected Q-point and given any desired slope by properly choosing V_{GG}. (The bias line intercepts the V_{GS} axis at V_{GG}.) The larger V_{GG} is made, the larger R_S will be and the better will be the approximation to constant-current biasing.

All three circuits in Figure 6 are equivalent. Circuit 6a requires an extra power supply. The need for an additional supply is avoided in 6b by deriving V_{GG} from the drain supply. R_1 and R_2 are simply a voltage divider. To maintain the high input impedance of the FET, R_1 and R_2 must both be very large.

Very large resistors cannot always be found in the exact ratio needed to derive the desired V_{GG} in every circuit application. Circuit 6c overcomes this problem by placing a large R_G between the center point of the divider and the gate. This allows R_1 and R_2 to be small, without lowering the input impedance.

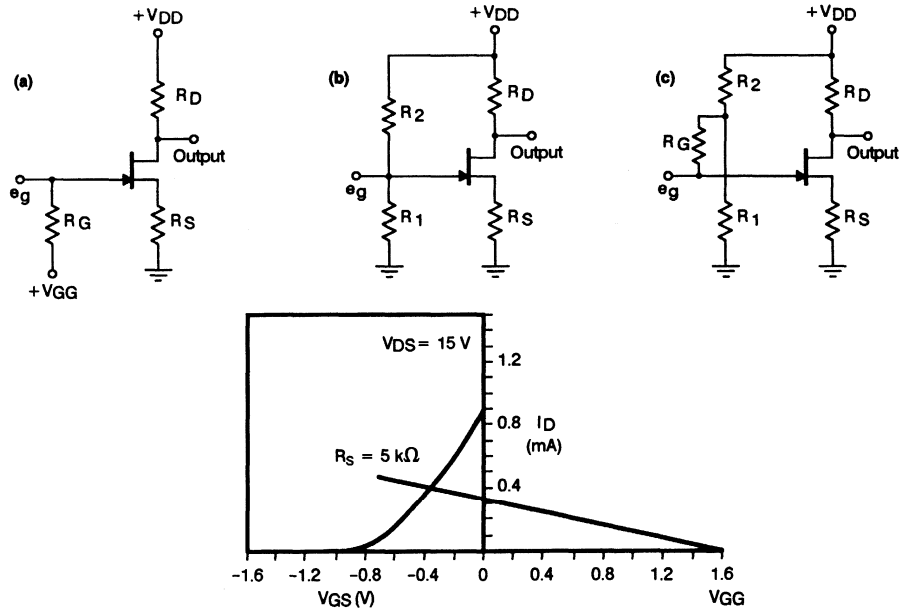

Figure 6. All three combination-bias circuits are equivalent. They add constant-voltage biasing to the self-bias circuit to establish a reasonably flat load line without sacrificing dynamic range.

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One point of caution is that as V_{GG} is increased, V_S increases, and V_{DS} decreases. Therefore, with low V_{DD}, there may be a significant decrease in the allowable output voltage swing.

Biasing for Device Variations

The value of the combination-bias technique becomes apparent when one considers the normal production spread of device characteristics. The problem is illustrated in Figure 7 where two limiting sets of output characteristics are presented. Limiting characteristics like these are not normally available. Even if they were, however, they'd be of little help in establishing operating points suitable for all devices with output characteristics lying between the two extremes. The problem is much more easily approached by using the set of limiting transfer characteristics of Figure 8.

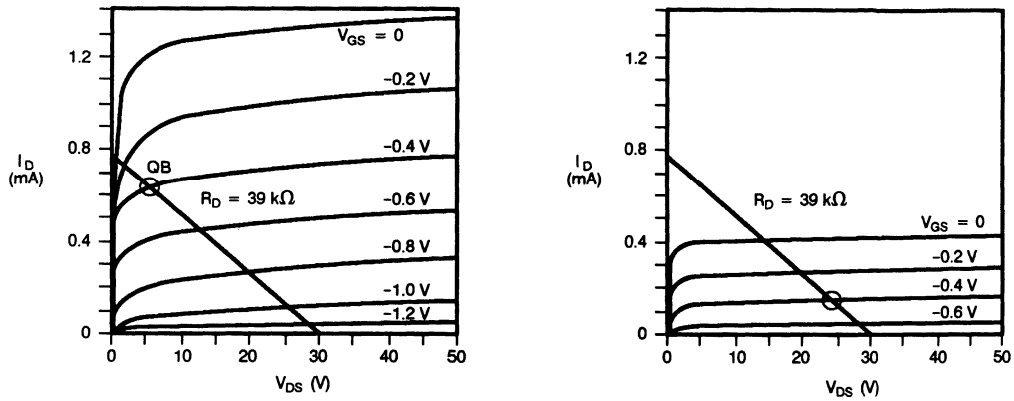

Figure 7. The wide variations in device performance shown by this pair of output characteristics make clear the disadvantages of constant-voltage biasing.

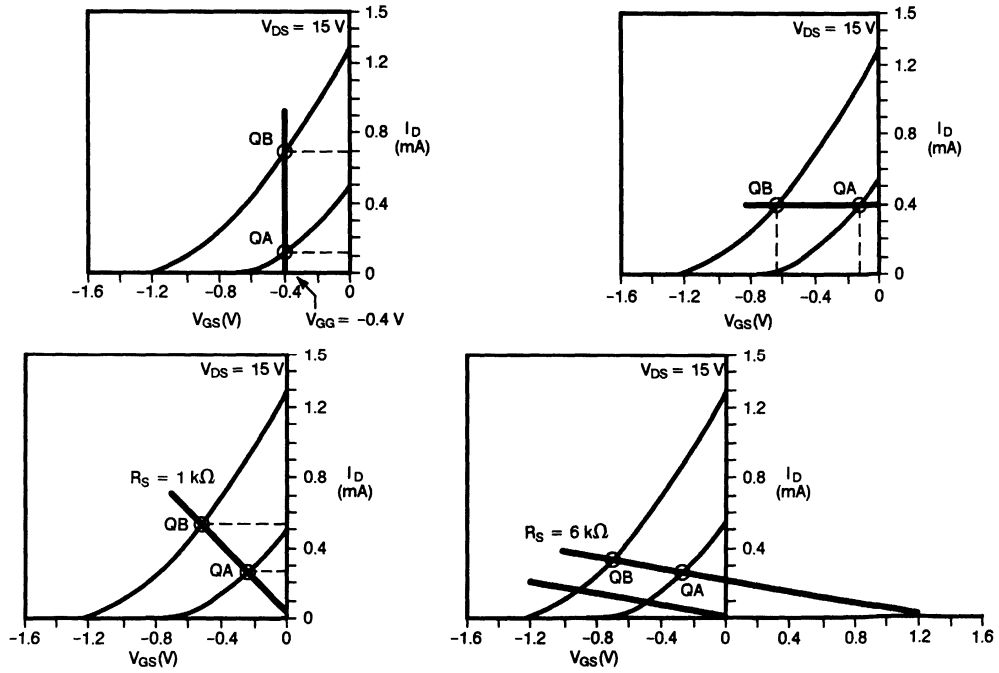

Figure 8. The advantages of combination biasing, when one is working with a spread of device characteristics, are made obvious by plotting the load lines for the various types of biasing on a pair of limiting transfer curves.

Attempting to establish suitable constant-voltage bias conditions for a production spread of devices is practical only for circuits with very small values of dc drain resistance - for example, circuits with inductive loads. As the constant-voltage bias plot of Figure 8 reveals, constant gate bias causes a significant difference in operating I_{DQ} for the extreme limit devices. At V_{GS} = -0.4 V, the range of I_{DQ} is 0.13 to 0.69 mA, and V_{GSQ} for a given R_D will vary greatly for most resistance-loaded circuits. For the example of Figure 1, with R_D = 39 kΩ and V_{DD} = 30 V, V_{GSQ} varies from near saturation (5 V) to 25 V.

An excellent method of biasing is the constant-current method of Figure 3. Biasing in this manner fixes the operating drain current for all devices and sets V_{DSQ} to $V_{DD} - I_{DQ}R_L$ for any device in the production spread. V_{GS} automatically finds a value to set the appropriate I_{DQ} = constant for all devices. For the constant-current bias plot of Figure 8, with I_{DQ} = 0.39 mA, V_{GS} would range from -0.11 to -0.67 V.

Output characteristics are not needed as long as I_{DQ} is chosen to be below the minimum I_{DSS}. With R_D = 39 kΩ and V_{DD} = 30 V, V_{DSQ} is 14.8 V for all devices.

The disadvantages of the constant-current method are that it allows no signal to be developed unless the current source is bypassed and, as we shall see, it lacks the flexibility to provide constant gain despite variations in the forward transconductance, g_{fs}, of the devices.

The self-bias scheme is a reasonable choice for single-ended dc amplifiers and for ac amplifiers. In unbypassed or dc circuits, some compromise must be made between the gain loss due to current feedback degeneration and the advantage of current stabilization achieved with high R_S.

An appropriate choice of I_{DQ} limits can be made by using the pair of limiting transfer curves. For example, for R_S = 1 kΩ, the load line shown on the self-bias curve of Figure 8 is established. The maximum I_D is 0.52 mA, and the minimum I_D is 0.24 mA. The operating range of V_{DSQ} may be calculated for any value of V_{DD} and R_D. Clearly, for R_D = 39 kΩ, the maximum-limit device (device B) would operate with V_{DSQ} = 9.8 V and the minimum-limit device (device A) would operate with V_{DSQ} = 20.6 V. This results in satisfactory operation for all devices. However, such a variation in I_{DQ} imposes severe limitations on the circuit design.

A better approach is illustrated by the combination-bias curve of Figure 8 with V_{GG} = 1.2 V. The range of I_{DQ} for the bias condition is 0.25 mA to 0.32 mA. A similar minimum difference in I_{DQ} could be achieved with R_S = 6 kΩ and V_{GG} = 0, (a self-bias condition) but the operating points would be pushed toward the toe of the transfer characteristics and allowable signal input would be reduced.

The upper load line allows g_{fs} = +1.8 V (limited by I_{DSSA}), while the lower line allows a V_{GS} of only +0.7 V (limited by $V_{GS(off)}$ A). (The subscript letters A and B refer to the minimum and maximum devices, respectively.) The combination circuit allows almost ideal operation over the full production spread of devices. Even with R_D = 6 kΩ, the V_{DSQ} would range only between 10 and 15 V.

For this circuit, R_D should be chosen to allow the largest output signal swing for I_{DQ} midway between the two extremes of 0.25 and 0.32 mA; namely 0.285 mA. Setting the voltage drop across R_D at one-half of (V_{DD} - 2 $V_{GS(off)typ}$) or 14 V, yields R_D = (14 V/0.285 mA) = 49 kΩ .

It is helpful, in any design, to know the effect of temperature variations on the transfer curves and transconductance characteristics. Ideally, minimum and maximum transfer characteristics would be plotted at three temperatures: above, below, and at room temperature. Then the design would take all types of variation into account.

Minimize The Gain Variations

Leaving R_S unbypassed helps reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

A better approach is to use the combination-bias technique with the bias point selected from the transfer and transconductance curves (Figure 9).

As Figure 9 shows, it is possible to find an R_S and a V_{GG} that will set I_{DQA} and I_{DQB} to values such that g_{fsQ} will be the same for both devices. The g_{fsQ} of all intermediate devices will be approximately equal to the limiting values. Thus, a constant, or nearly constant, stage gain is obtained even with a bypass capacitor.

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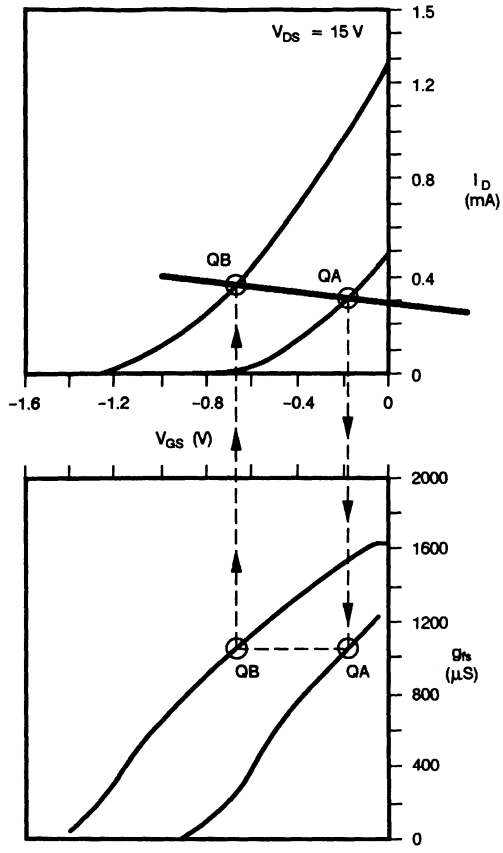

Figure 9. Gain variations are minimized when the load line is designed to intersect the pair of limiting transfer curves (top) at points of equal g_{fs} (bottom).

The design procedure is as follows:

Step 1. Select a desired I_{DQA} below I_{DSSA}. A good value, allowing for temperature variations, is 60% of I_{DSSA}. This will allow for decreasing I_{DSS} due to temperature variation and for reasonable signal excursions in load current.

Step 2. Enter the transfer curves at $I_{DQA} \sim 0.6\ I_{DSSA}$ (0.3 mA) to find V_{GSQA}. Thus $V_{GSQA} \sim -0.2$.

Step 3. Drop vertically at V_{GSQA} to the minimum limit transconductance curve to find g_{fsQA}. The value as read from the plot is approximately 1000 µS.

Step 4. Travel across the g_{fs} plot to the maximum curve to find V_{GSQB} at the same value of g_{fs}. This is $V_{GSQB} \sim -0.7$ V.

Step 5. Travel vertically up to the maximum limit transfer curve to find I_{DQB} at V_{GSQB}. This is $I_{DQB} \sim$ 0.36 mA.

Step 6. Construct an R_S bias line through points QA and QB on the transfer curves. The slope of the line is $1/R_S$, and the intercept with the V_{GS} axis is the required V_{GG}.

As Figure 9 demonstrates, it may be somewhat inconvenient to perform Step 6 graphically. An algebraic solution can be employed instead. The source resistance is given by

$$R_S = (V_{GSQA} - V_{GSQB}) / (I_{DQB} - I_{DQQA}) \quad (2)$$

and the bias voltage is

$$V_{GG} = R_S I_{DQB} + V_{GSQB} \quad (3)$$

Care should be taken to maintain the proper algebraic signs in Equations 2 and 3. For n-channel FETs, V_{GS} is negative and I_D is positive. For p-channel units, the signs are reversed.

If the transconductance curves of Figure 9 are not available, g_{fs} can be determined by simply measuring the slope of the transfer curve at the desired operating point. Just place a straight-edge tangent to the curve at the Q-point and note the points at which it intercepts the I_D and V_{GS} axes. The slope and g_{fs} are given by:

$$\text{slope} = g_{fs} = I_{D(\text{intercept})} / -V_{GS(\text{intercept})} \quad (4)$$

In designing a constant-gain circuit, simply set the straight-edge tangent to the transfer curve of device A at point QA and slide it, without changing its slope, until it is tangent to the curve of device B. The tangency point is QB.

Designing Without Output Curves

Although the transfer characteristic has been shown to be extremely valuable in designing a bias circuit, it cannot be used to graphically establish V_{DSQ}. However, if a set of output curves is not available, V_{DSQ} can be determined or selected from the transfer curve by using the following procedure:

Step 1. Establish R_S and limiting values of I_{DQ}, V_{GSQ} and g_{fsQ} from the transfer curve.

Step 2. Establish V_{DD} as available, but in no case greater than $V_{(BR)GSS}$ nor less than several times $V_{GS(off)}$. There are special cases where V_{DD} will be below this limit, but in no case should instantaneous V_{DG} be allowed to fall below $2 \times V_{GS(off)}$ if minimum distortion is to be achieved.

Step 3. Set V_{DSQ} approximately midway between V_{DD} and $2 \times V_{GS(off)}$; lower if large output signals will not be handled.

Step 4. Select R_D to give the appropriate V_{DSQ}. The formula is:

$$R_D = [(V_{DD} - V_{DSQ}) / 0.5 (I_{DQA} + I_{DQB})] - R_S \quad (5)$$

In the example of Figure 8, this procedure would have yielded $V_{DSQ} = (30 - 3)/2 = 13.5$ V and $R_D = (30 - 13.5)/0.5\ (0.52 + 0.24)$ mA $- 1\ k\Omega = 42.5\ k\Omega$.

Step 5. Check to ensure that with this R_D, device B is not in a saturated condition, i.e. $V_{DQB} = V_{DD} - I_{DQB}R_D > 2\,V_{GS(off)} + R_S I_{DQB}$.

An alternate method, that selects R_D to provide a specified voltage gain, follows Steps 1 and 2 above and then proceeds as follows:

Step 3 Determine required stage gain, A_V, and set $R_D = A_V/g_{fsQ}$.

Step 4. Calculate V_{DSQ} to ensure that the criteria of Step 2 are not violated:

$$V_{DSQ} = V_{DD} - (R_D + R_S)\, I_{DQ} \quad (6)$$

Step 5. If necessary, change I_{DQ}, V_{DD}, A_V and/or R_D to obtain an optimum compromise.

FET SOURCE-FOLLOWER CIRCUITS

The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors. By considering ten circuits (Figure 10), which represent virtually every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations (Figure 10). Circuits 10a through 10e have no gate feedback; their input impedances, therefore, are equal to R_G. Circuits 10f through 10k employ feedback to their gates to increase the input impedance above R_G.

Before getting into the details of bias-circuit design, note several general observations that can be made about the circuits of Figure 10:

- Circuits a, c, d, f, h, and j can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals limited only by the available supply voltages and device breakdown voltage.

- Circuits c, d, e, h, j, and k employ current sources to improve drain-current (I_D) stability and increase gain.

- Circuits d, e, and k employ FETs as current sources. In circuit d, Q_2 must have a lower cutoff voltage, $V_{GS(off)}$, and a lower zero gate-voltage drain current, I_{DSS}, than Q_1.

- Circuits e, g, and k employ a source resistor, R_S, which may be selected to set the quiescent output voltage equal to zero.

- Circuits e and k use matched FETs. R_S is selected to set I_D near the specified low-drift operating current. The input-output offset is zero.

Biasing Without Feedback Is Simple

The no-feedback circuits of Figure 10 (circuits 10a through 10e use simple biasing techniques (see the earlier article). Circuit 10a is a self-bias configuration; the voltage drop across R_S biases the gate (which draws essentially zero current) through resistor R_G. Since no gate-to-source voltage, V_{GS}, can be developed when $I_D = 0$, the self-bias load line passes through the origin (Figure 11). The quiescent drain current is seen to lie between about 0.25 and 0.55 mA when a 1 kΩ source resistor is used. The quiescent output voltage lies between 0.25 and 0.55 V.

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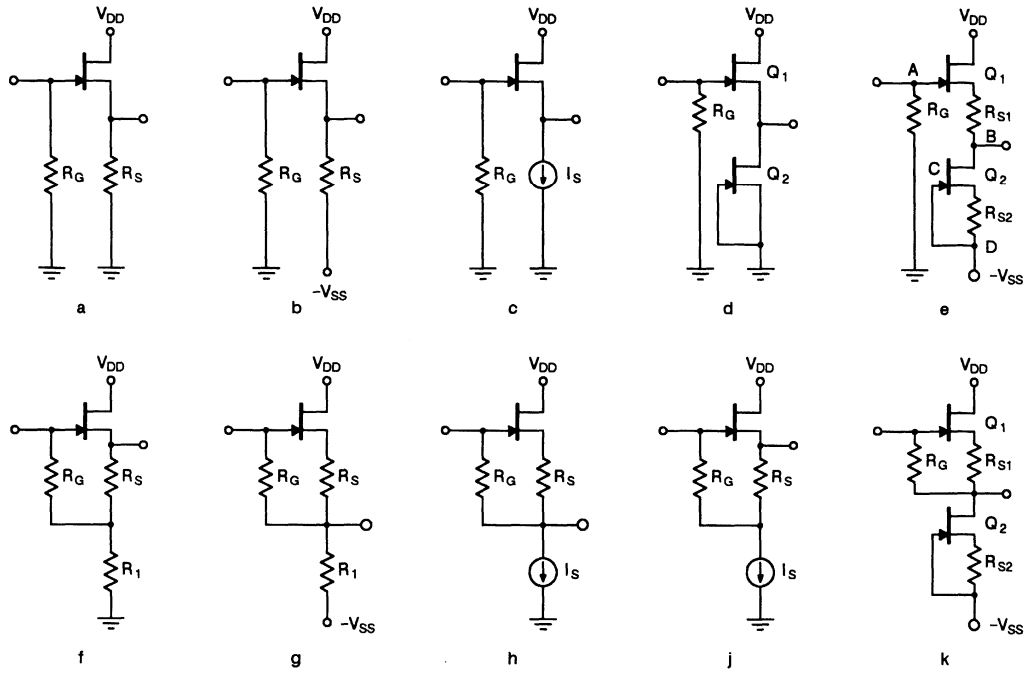

Figure 10. Virtually every practical source-follower configuration is represented in this collection of ten circuits. The configurations in the top row do not employ gate feedback; the corresponding ones in the bottom row do.

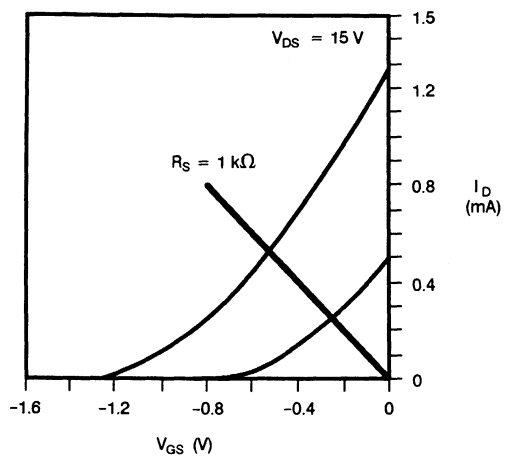

Figure 11. Self-biasing (Figure 10a) uses the voltage dropped across the source resistor, R_S to bias the gate. The load line passes through the origin and has a slope of $-1/R_S$.

Circuit 10b is another example of source-resistor biasing with a $-V_{SS}$ supply added. The advantage over circuit 10a is that the signal voltage can swing negative to approximately $-V_{SS}$. Two bias lines are shown in Figure 12, one for V_{SS} = −15 V and the other V_{SS} = −1.6 V. For the first case, the quiescent output voltage lies between 0.18 and 0.74 V. For the second, it lies between 0.3 and 0.82 V.

The bias load line for circuit 10c is just a horizontal line (I_D = constant). The quiescent output voltage is between 0.15 and 0.7 for I_D = 0.3 mA.

Circuit 10d is similar to 10c except that the V_{GS} = 0 output characteristic of FET Q_2 is used as a current source. As seen in Figure 13, Q_2 does not supply constant current when its V_{DS} gets very small. This technique should therefore be used only to bias FETs whose $V_{GS(off)}$ is significantly higher than the equivalent $V_{GS(off)}$ of the current-source FET diode.

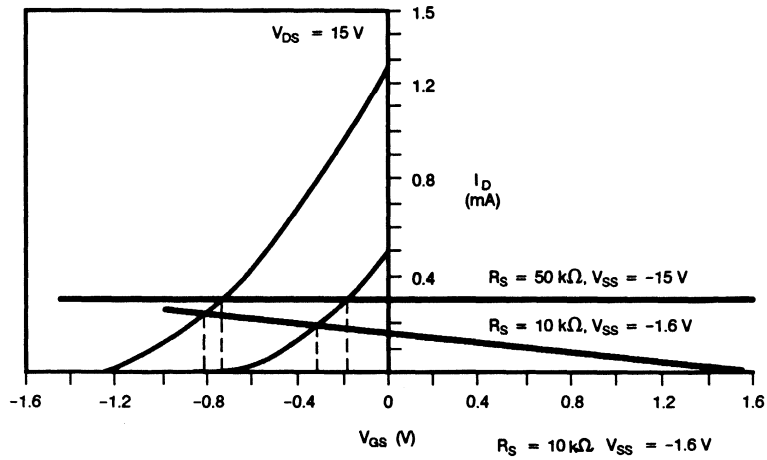

Figure 12. Adding a V_{SS} supply to the self-bias circuit (Figure 10b) allows it to handle large negative signals. The load line's intercept with the V_{GS} axis is at $V_{GS} = V_{SS}$. Bias lines are shown for V_{SS} = −15 V and V_{SS} = −1.6 V.

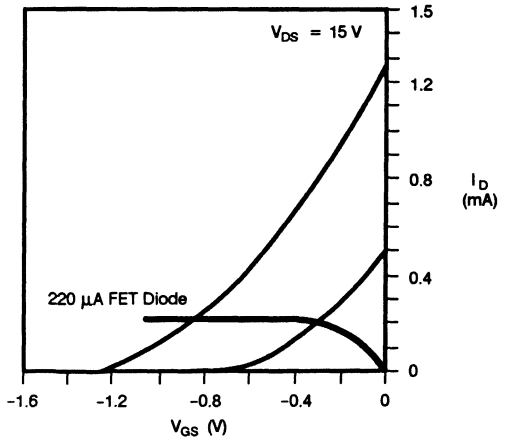

Figure 13. FET Q_2 doesn't behave like an ideal current source when its V_{DS} gets very small (Figure 10d). Therefore, Q_1 should have a significantly larger $V_{GS(off)}$ than the Q_2 does.

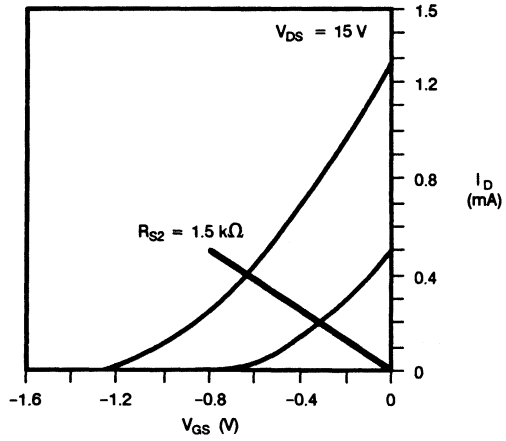

Figure 14. This load line is set by R_{S2} and Q_2 which acts as a current source (Figure 10e). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are temperature-matched at the operating I_D, the source follower will exhibit zero or near-zero temperature drift.

8

A pair of matched FETs is used in the circuit of Figure 10e, one as a source follower and the other as a current source. The operating drain current (I_{DQ}) is set by R_{S2}, as indicated by the load line of Figure 14. The drain current may be anywhere from 0.2 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however, $V_{GS1} = V_{GS2}$ because the FETs are matched.

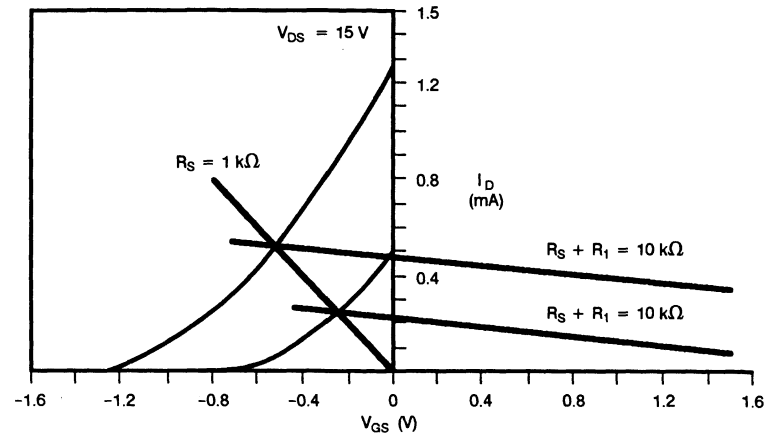

Figure 15. The bias load line is set by R_S but the output load line is determined by $R_S + R_1$ when gate feedback is employed (Figure 10f). The feedback V_{FB} is determined by the intercept of the $R_S + R_1$ load line and the V_{GS} axis.

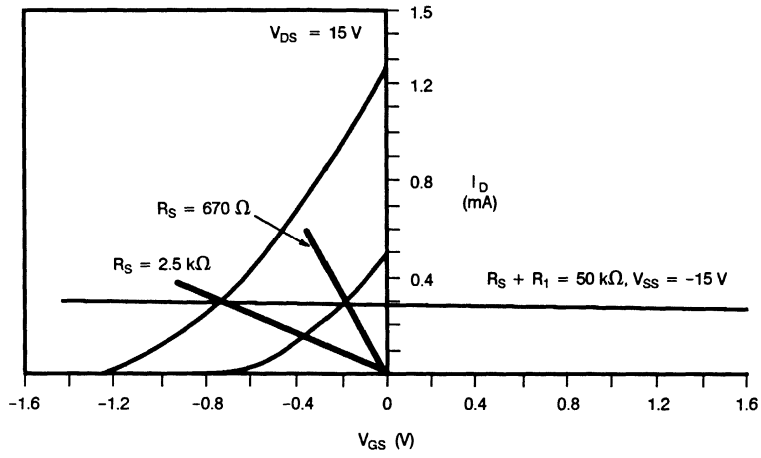

Figure 16. R_S can be trimmed to provide zero offset at some point between 670 Ω and 2.5 kΩ (Figure 10g). The source load line intercepts the V_{GS} axis at $V_{SS} = V_{GG} = -15$ V. Note that this load line is not perfectly flat. It has a slope of -1/50 kΩ, because the current source is not perfect; it has a finite impedance.

Biasing With Feedback Increases Z_{IN}

Each of the feedback-type source followers (Figure 10f through 10k) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case, R_G is returned to a point in the source circuit that provides almost unity feedback to the lower end of R_G. If R_S is chosen so that R_G is returned to zero dc volts (except in circuit 10f, then the input/output offset is zero. R_1 is usually much larger than R_S.

Circuit 10f is useful principally for ac-coupled circuits. R_S is usually much less than R_1 to provide near-unity feedback. The bias load line is set by R_S (Figure 15). The output load line, however is determined by the sum of $R_S + R_1$. The feedback voltage V_{FB}, measured at the junction of R_S and R_1, is determined by the intercept of the $R_S + R_1$ load line with the V_{GS} axis. The quiescent output voltage is $V_{FB} - V_{GS}$.

In the circuit of Figure 10g, R_S can be trimmed to provide zero offset. As the curves show (Figure 16), R_S will be between 670 Ω and 2.5 kΩ. R_S is much less than R_1. The source load line intercepts the V_{GS} axis at $V_{SS} = -V_{GG} = -15$ V.

Circuit 10h is almost the same as 10g; the difference is that resistor R_S is replaced by a current source. Since an ideal current source has infinite impedance, the bias curve of circuit 1h differs from that of Figure 10g (Figure 16) in that the load line is perfectly flat. In Figure 16 the load line is almost, but not quite, flat; it has a slope of −1/50 kΩ.

Circuit 10j is similar to 10h except that the output is taken from the top of R_S to reduce the output impedance. R_S must be trimmed if the circuit is to work properly.

In Figure 17, the constant-current load line represents a 0.3 mA current source, and the effect of a 1 kΩ source resistor is shown. The offset voltage is seen to lie between 0.2 and 0.75 V. The intercept of the R_S load line and the V_{GS} axis sets the voltage at the junction of R_S and the current source (V_{FB}). For R_S = 1 kΩ, V_{FB} will be between −0.1 V and 0.45 V. Since V_{FB} appears at the gate, it must be zero if the dc input impedance of the circuit is to be preserved.

This can be done by trimming R_S, as shown dashed in Figure 17. The biasing then becomes the same as for circuit 10h.

Biasing for circuit 10k is identical to that for circuit 10e (Figure 14) except that feedback is added to raises the input impedance.

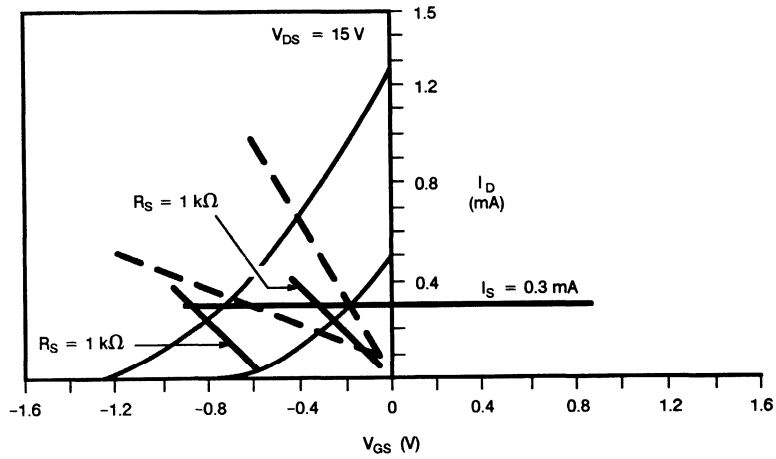

Figure 17. If R_S is not trimmed so that the load line passes through the origin, a voltage will appear at the gate causing a reduction in dc input impedance. The incremental input impedance will not be affected.

8

THE FET CONSTANT-CURRENT SOURCE

INTRODUCTION

The combination of low associated operating voltage and high output impedance make the FET attractive as a constant-current source. An adjustable-current source (Figure 1) may be built with a FET, a variable resistor, and a small battery. For good thermal stability, the FET should be biased near the zero temperature coefficient point.

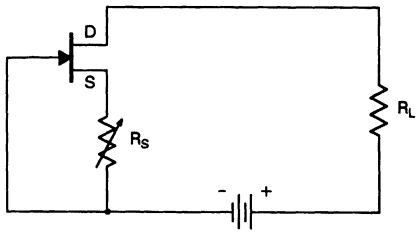

Figure 1. Field-Effect Transistor Current Source

Whenever the FET is operated in the saturated region, its output conductance is very low. This occurs whenever the drain-source voltage V_{DS} is significantly greater than the cut-off voltage $V_{GS(off)}$. The FET may be biased to operate as a constant-current source at any current below its saturation current I_{DSS}.

For a given device where I_{DSS} and $V_{GS(off)}$ are known, the approximate V_{GS} required for a given I_D is

$$V_{GS} = V_{GS(off)}\left[1 - \left(\frac{I_D}{I_{DSS}}\right)^{1/k}\right] \quad (1)$$

where k can vary from 1.7 to 2.0, depending on device geometry. The series resistor R_S required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \quad (2)$$

A change in supply voltage or a change in load impedance, will change I_D by only a small factor because of the low output conductance g_{oss}.

$$\Delta I_D = (\Delta V_{DS})(g_{oss}) \quad (3)$$

The value of g_{oss} is an important consideration in the accuracy of a constant-current source. As g_{oss} may range from less than 1 µS to more than 50 µS according to the FET type, the dynamic impedance can be greater than 1 MΩ to less than 20 kΩ. This corresponds to a current stability range of 1 µA to 50 µA per volt. The value of g_{oss} also depends on the operating point. Output conductance g_{oss} decrease approximately linearly with I_D. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}} \quad (4)$$

where

$$g_{oss} = g'_{oss} \quad (5)$$

when

$$V_{GS} = 0 \quad (6)$$

So as $V_{GS} \longrightarrow V_{GS(off)}$, $g_{oss} \longrightarrow$ Zero. For best regulation, I_D must be considerably less than I_{DSS}.

It is possible to achieve much lower g_{oss} per unit I_D by cascading two FETs, as shown in Figure 2.

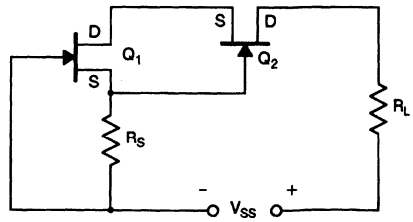

Figure 2. cascade FET Current Source

Now, I_D is regulated by Q_1 and $V_{DS1} = -V_{GS2}$. The dc value of I_D is controlled by R_S and Q_1. However, Q_1 and Q_2 both affect current stability. The circuit output conductance is derived as follows:

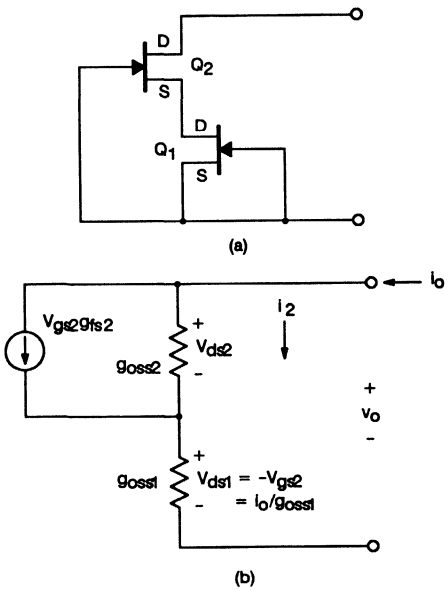

Figure 3. Cascade FET $V_{GS1} = 0$

$$i_o = i_2 + v_{GS2} g_{fs2} = v_{ds2} g_{oss2} - i_o \frac{g_{fs2}}{g_{oss1}} \quad (7)$$

$$i_o = \frac{v_{ds2} g_{oss2} g_{oss1}}{g_{oss1} + g_{fs2}} \quad (8)$$

$$v_o = v_{ds1} + v_{ds2} = v_{ds2} + \frac{i_o}{g_{oss1}} \quad (9)$$

$$v_o = v_{ds2} \frac{g_{oss1} + g_{oss2} + g_{fs2}}{g_{oss1} + g_{fs2}} \quad (10)$$

$$g_o = \frac{i_o}{v_o} = \frac{g_{oss1} g_{oss2}}{g_{oss1} + g_{oss2} + g_{fs2}} \quad (11)$$

If $g_{oss1} = g_{oss2}$ (12)

$$g_o = \frac{g_{oss}}{2 + g_{fs} / g_{oss}} \quad (13)$$

when $R_S \neq 0$ as in Figure 2

$$g_o = \frac{g_{oss}^2}{2g_{oss} + g_{fs} + R_S (g_{fs}^2 + g_{oss} g_{fs} + g_{oss}^2)} \quad (14)$$

$$\approx \frac{g_{oss}^2}{g_{fs} (1 + R_S g_{fs})} \quad (15)$$

In either case ($R_S = 0$ or $R_S \neq 0$), the circuit output conductance is considerably less than the g_{oss} of a single FET.

In designing any cascaded FET current source, both FETs must be operated with adequate drain-gate voltage, V_{DG}. That is,

$$V_{DG} > V_{GS(off)}, \text{ preferably } V_{DG} > 2 V_{GS(off)} \quad (16)$$

If $V_{DG} < 2V_{GS(off)}$, the g_{oss} will be significantly increased, and circuit g_o will deteriorate. For example: A JFET may have a typical $g_{oss} = 4\ \mu S$ at $V_{DS} = -20$ V and $V_{GS} = 0$. At $V_{DS} \sim -V_{GS(off)} = 2$ V, $g_{oss} \sim 100\ \mu S$.

The best FETs for current sources are those having long gates and consequently very low g_{oss}. The Siliconix 2N4869 exhibits typical $g_{oss} = 1\ \mu S$ at $V_{DS} = 20$ V. A single 2N4869 in the circuit of Figure 4 will yield a current source adjustable from 5 μA to 1 mA with internal impedance greater than 2 MΩ.

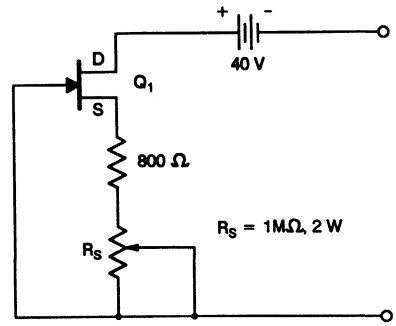

Figure 4. Adjustable Current Source $R_S = 1$ MΩ, 2 W

The cascade circuit of Figure 5 provides a current adjustable from 2 μA to 1 mA with internal resistance greater than 10 MΩ.

Siliconix also offers a line of JFETs with a resistor fabricated on the device, thus creating a 10% current range. The series is called the CR022 (0.22 mA range) through the CR530 (5.3 mA range). See the data sheet section for specific part types. The devices allow precision designs using a single device versus the typical approach using several components.

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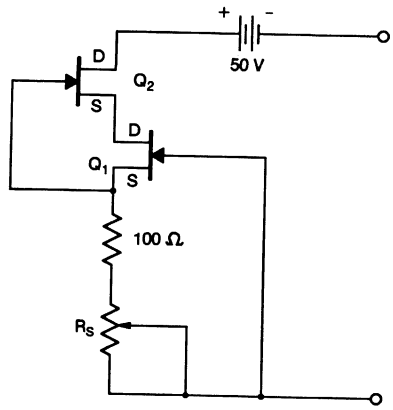

Q_1 = 2N4340
Q_2 = 2N4341
R_S = 1MΩ, 2 W

Figure 5. Cascade FET Current Source

P-CHANNEL MOSFETS THE BEST CHOICE FOR HIGH-SIDE SWITCHING

Ed Oxner

Historically, p-channel FETs were not considered as useful as their n-channel counterparts. The higher resistivity of p-type silicon, resulting from its lower carrier mobility, put it at a disadvantage compared to n-type silicon.

Getting n-type performance out of p-type FETs has meant larger area geometries with correspondingly higher inter-electrode capacitances. Consequently, a truly complementary pair – a p-channel and an n-channel device that match in *all* parameters – is impossible.

Yet, despite its shortcomings, the p-channel MOSFET performs a vital "high-side" switch task that the n-channel simply cannot equal.

Used as a high-side switch, a p-channel MOSFET in a totem-pole arrangement with an n-channel MOSFET will simulate a high-current, high-power CMOS (complementary MOS) arrangement. Although the p-channel MOSFET cannot complement the n-channel in both on-resistance and capacitance simultaneously, such combinations as the low-threshold p-channel TP0610 and the n-channel 2N7000 together offer outstanding performance as a complementary pair.

CIRCUIT APPLICATIONS

Switching Ground-Return Loads

The principal application of the p-channel, enhancement-mode MOSPOWER FET is in switching power (or voltage) to grounded (ground return) loads.

To drive the FET properly, the gate voltage must be referenced to its source. For enhancement-mode MOSFETs, this gate potential is of the same polarity as the MOSFET's drain voltage. To turn on, the n-channel MOSFET requires a positive gate-source voltage, whereas the p-channel MOSFET requires a negative gate-source potential.

During switching, a MOSFET's source voltage must remain fixed, as any variation will modulate the gate and thus adversely affect performance. Figure 1 shows this degradation by comparing n-channel and p-channel MOSFET high-side switching.

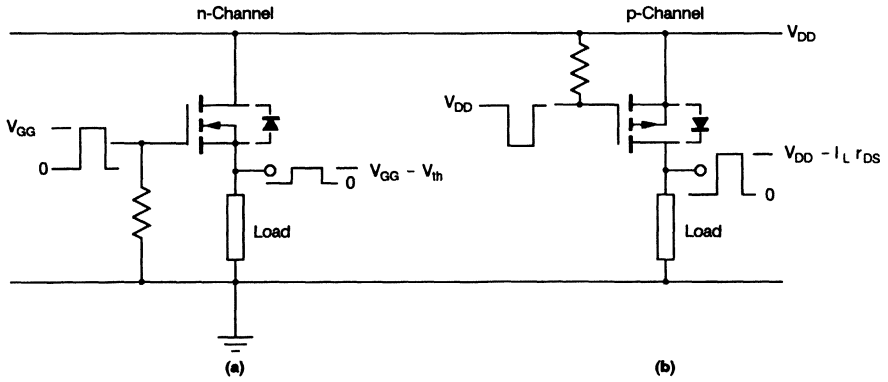

Figure 1. Comparing the Performance Between n-Channel and p-Channel Grounded-Load Switching

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If an n-channel, enhancement-mode MOSFET were switching a positive-polarity voltage to a grounded load, the output would be limited to $V_{GG} - V_{th}$.

The equations describing performance of the n-channel ground-switching MOSFET with a ground-reference gate drive are based on the relationship between V_{DD} and V_{GG}:

If $V_{DD} \geq V_{GG}$, then $V_O = V_{GG} - V_{th}$;

If $V_{DD} < V_{GG}$, then $V_O = V_{DD} - I_L r_{DS(on)}$.

Sustaining a more acceptable gain with an output in direct relation to V_{DD} would require an isolated gate drive referenced to the source, as shown in Figure 2.

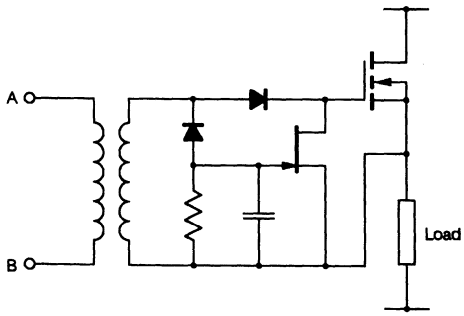

Figure 2. Floating Gate Drive

Bootstrapping the n-channel MOSFET (Figure 3) is satisfactory for short turn-on times of a few milliseconds. In this arrangement, both MOSFETs must have breakdown voltage specifications that match or exceed the rail voltage.

Using a p-channel MOSFET in the configuration shown in Figure 1b may place some severe restraints on the gate drive, since the gate must be close to V_{DD}. To return gate control to a more acceptable logic format, add an n-channel MOSFET as shown in Figure 4.

Using an n-channel MOSFET in this way simplifies the gate drive for a high-voltage, high-side, p-channel MOSFET. Placing a Zener diode between the gate and rail ensures that $V_{(BR)GSS}$ will not be exceeded. Again, both MOSFETs must withstand the full rail voltage.

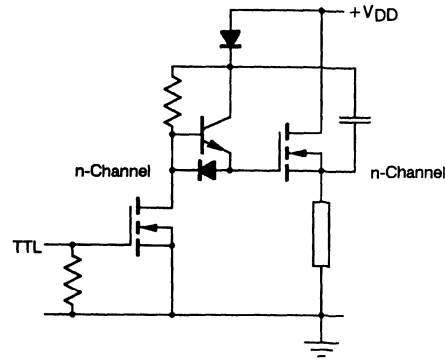

Figure 3. Bootstrapping for n-Channel Ground-Loaded Switching

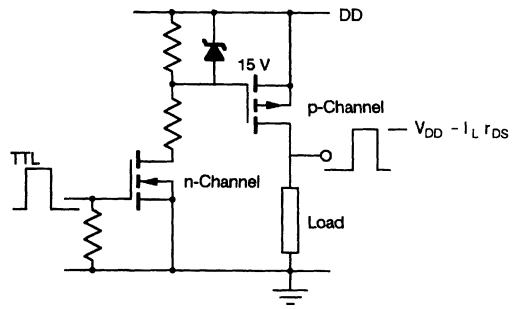

Figure 4. Using an n-Channel Level-Shifter Simplifies Driving from Logic

Half-Bridge (Totem Pole)

A high-side p-channel MOSFET and a low-side n-channel MOSFET tied with common drains (Figure 5) make a superb high-current "CMOS equivalent" switch. One fault common to such circuits has been the excessive crossover current during switching that may occur if the gate drive allows both MOSFETs to be on simultaneously.

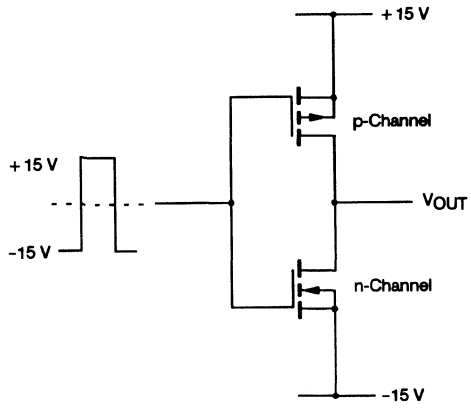

Figure 5. Low-Voltage Complementary MOSPOWER Array

At high rail voltages (both $+V_{DD}$ and $-V_{DD}$), properly driving the MOSFET gates can minimize unwanted crossover current, as Figure 6 shows. When the output stage uses high-power MOSFETs, a resistively-coupled lower-power complementary pair offers extremely low crossover current. The Zener, Z1, and resistors, R1 and R3, act as a level shifter, properly driving the low-power MOSFETs. The Zener may be selected according to the equation

$$V_{ZENER} = 2V_{DD} - |V_{th}|$$

where $+V_{DD} = -V_{DD}$

Whatever crossover current that might occur in the low-power drivers is dramatically reduced by the series resistor, R4. Additionally, driving the high-power complementary pair using this resistor divider scheme all but eliminates crossover current in this critical output driver. This increases both the driver's efficiency and its reliability.

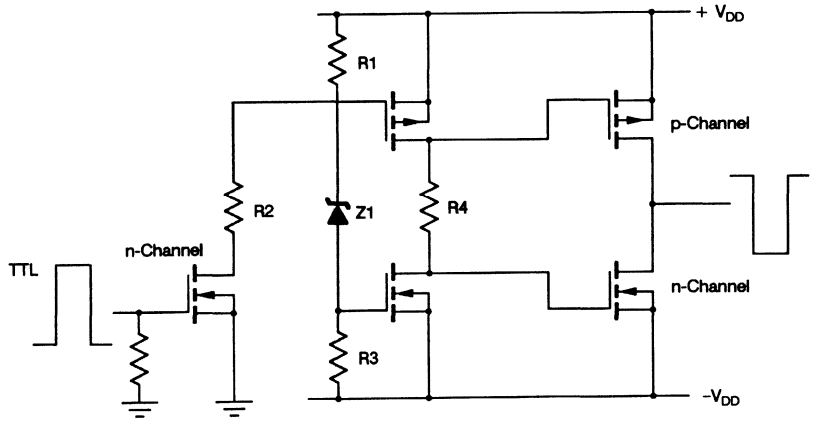

Figure 6. High-Voltage Complementary Pair Driven by Logic-Compatible MOSFET

8

DEPLETION-MODE MOSFETS EXPAND CIRCUIT OPPORTUNITIES

Ed Oxner & Richard Bonkowski

INTRODUCTION

A principal advantage of the depletion-mode MOSFET is its ability to perform at higher operating voltages than its JFET counterpart. As a depletion-mode structure, the MOSFET permits the added flexibility of allowing the gate potential not only to be higher but to be of either polarity. Earlier, small-signal MOSFETs were classed as being quite sensitive to ESD. With the introduction of the ND2020 and ND2410 series, sensitivity to ESD has been greatly reduced.

Perhaps the only short coming for the depletion-mode MOSFET is its higher-than-JFET noise performance. Where the JFET has been perceived as a "noiseless" transistor, the MOSFET does not share that renown.

Depletion-Mode vs. Enhancement-Mode

Three Classes of FETs

There are three classes of FETs, both n- and p-channel, that are identified by the Class A, B and C. Class A encompasses the whole field of junction FETs (JFETs). Class B includes those that are identified as depletion-mode MOSFETs, and Class C includes those recognized as enhancement-mode MOSFETs. Figure 1 illustrates the basic differences that distinguish the various classes and also demonstrates how these classes differ with respect to biasing.

In the symbols used in Figure 1, the solid bar identifies a depletion-mode FET (current conduction at zero bias); the broken bar identifies an enhancement-mode MOSFET (zero conduction at zero bias).

Note that although Class A and B are both classified as depletion-mode, Class B radically differs in that depletion-mode MOSFETs are also capable of performance in the enhancement-mode region. This distinction is only achievable for Class B. Although neither Class A (JFETs) nor Class C (MOSFETs) can perform beyond their respective mode, Class B – the depletion-mode MOSFET – is capable of operation in both modes!

Perhaps the simplest definition of depletion-mode operation is shown by the transfer characteristic (biasing) curves shown in Figure 1b. Drain current is reduced to zero when the gate voltage reaches a critical cutoff voltage, opposite in polarity to that of the drain voltage. The n-channel JFET (or Class B MOSFET) has a positive-polarity drain voltage and is controlled by a negative-polarity gate voltage. Why the Class B MOSFET may also perform in the enhancement-mode is made clear by study of the structure.

The Structure of MOSFETs

All MOSFETs are classified as either depletion-mode or enhancement-mode. Although they can be fabricated as n- or p-channel, generally we find n-channel MOSFETs in either mode and p-channel MOSFETs available only as enhancement-mode devices.

There are, however, three fundamental styles of MOSFETs regardless of mode. The classic planar MOSFET, shown in cross-section in Figure 2, the short-channel double-diffused MOSFET (DMOS FET), shown in Figure 3, and the vertical power MOSFET, shown in Figure 4. The features of each style are distinguished by performance.

When viewing the cross section, the distinguishing feature that quickly identifies the mode is whether a diffused channel spans the gap from source to drain. The absence of a visible channel (Figure 2a, 3a, and 4a) identifies the enhancement-mode MOSFET.

The Performance of a Depletion-Mode MOSFET

Regardless of whether or not a MOSFET is an n- or p-channel device, there are fundamental performance differences between depletion-mode and enhancement-mode MOSFETs. There are also important, though secondary, differences between styles of MOSFET: planar, DMOS, or vertical. The principle differences will be clarified by studying the transfer characteristics (biasing) shown in Figure 1.

Revised (02/11/91)

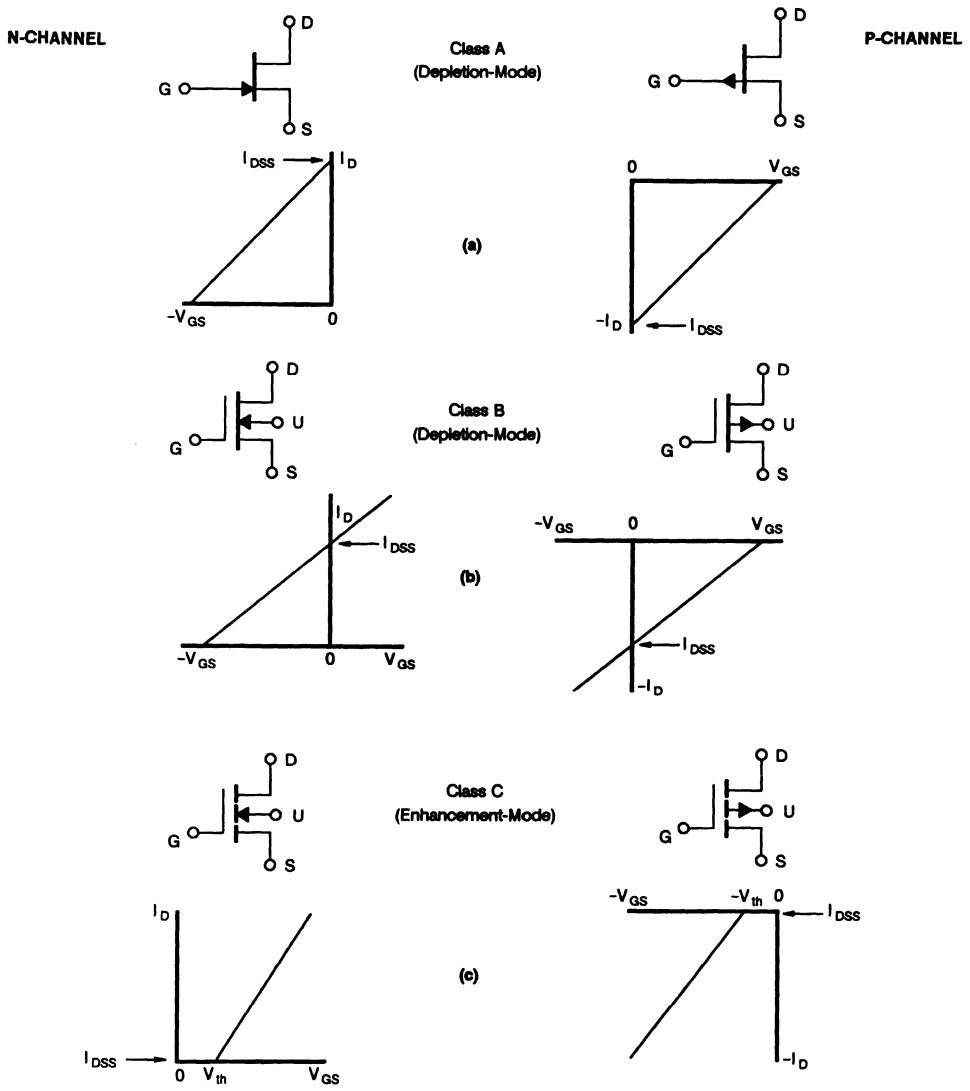

Figure 1. Classification of FETs

The transfer characteristics of the n-channel, depletion-mode MOSFET are shown in Figure 1b. Because the gate is isolated (see Figure 2b), V_{GS} can be reversed without creating a gate current. The gate may be made either positive or negative with respect to the source. By allowing the gate-to-source potential to go positive and increasing the magnitude of gate voltage, additional free electrons will be attracted beneath the gate oxide further enhancing the diffused channel and allowing I_D to become greater than I_{DSS}!

8

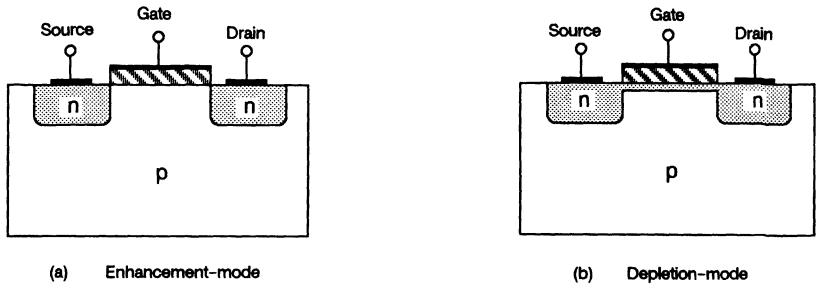

Figure 2. Classic Planar MOSFETs

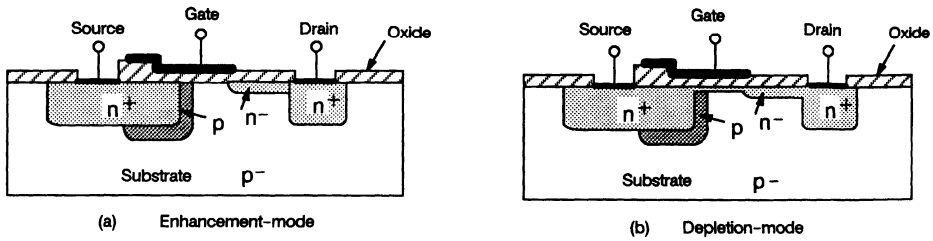

Figure 3. Short-Channel Double-Diffused MOSFET

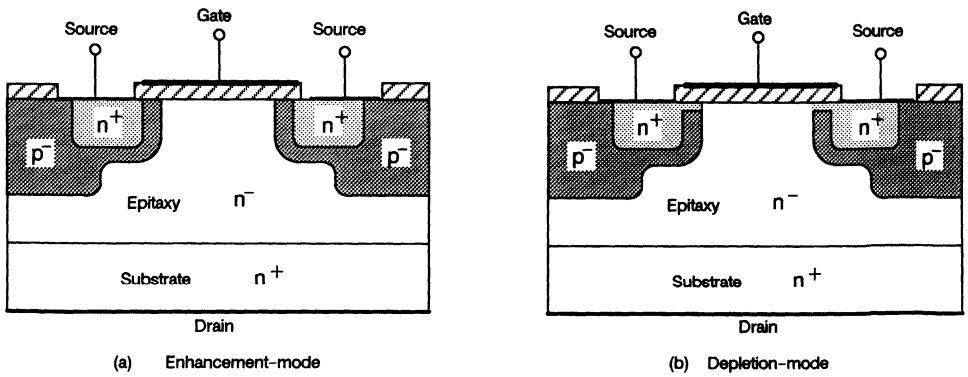

Figure 4. Vertical Power MOSFET

This mode of operation results in a unique series of output characteristics where, for the n-channel depletion-mode MOSFET, we see near-linear performance in what appears as the enhancement region. This performance is shown in Figure 5. The foregoing establishes that the depletion-mode MOSFET is a "normally-on" device; that is, when $V_{GS} = 0$, $I_D = I_{DSS}$. When a normally-off device is needed, the enhancement-mode MOSFET is selected.

Applications For Depletion-Mode MOSFETs

As a Current Regulator

An ideal current source supplies a fixed current to a load independent of the impressed voltage. Such a source would exhibit zero output conductance. Aside from the fact that depletion-mode MOSFETs can handle higher voltages and greater currents than most JFETs, they exhibit two characteristics which make them near-ideal current regulators. First, when the impressed voltage exceeds pinch-off, V_P , the saturation characteristics exhibit near-constant current (low output conductance) over a wide voltage range (see Figure 5). Second, performance as a depletion-mode transistor allows for simplified biasing to achieve the desired results.

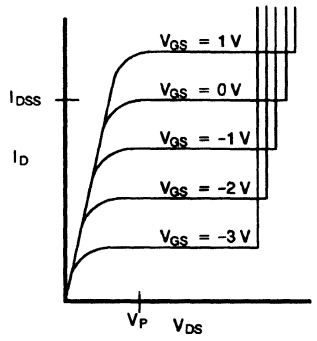

Figure 5. Output Characterictics n-Channel Depletion-Mode MOSFET

Basic Regulator Circuit

For a given device where I_{DSS} and $V_{GS(off)}$ are both known, the value of bias required to establish the regulating current may be approximated by

$$V_{GS} = V_{GS(off)} \left(1 - \frac{I_D}{I_{DSS}}\right)^{1/2} \quad (1)$$

The biasing resistor, R_S, required in the source of the MOSFET is

$$R_S = \frac{V_{GS}}{I_D} \quad (2)$$

A change in either supply voltage or load impedance will change the regulating current in proportion to the magnitude of the output conductance of the MOSFET.

$$dI_D = dV_{DS}\, g_{os} \quad (3)$$

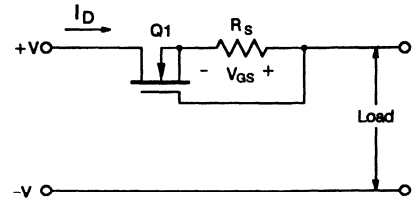

Figure 6. Basic Regulator Circuit

A typical constant-current regulator circuit that employs a depletion-mode MOSFET is shown in Figure 6. As with any depletion-mode FET, the lower the ratio between I_D and I_{DSS} the better the regulation, as shown in Figure 7 and Table 1.

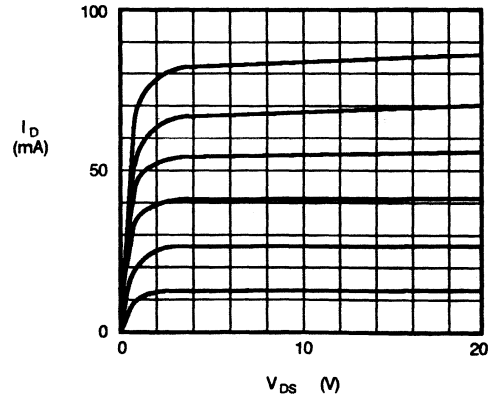

Figure 7. Output Characterictics of a Depletion-Mode MOSFET

Table 1

$\frac{I_D}{I_{DSS}}$	% Regulation
0.02	0.5
0.05	1.0
0.10	1.5
0.20	2.5
0.30	3.5

8

Extending Power Level Using MOSPOWER

The n-channel, depletion-mode MOSFET can be used in conjunction with an enhancement-mode power device to give an appreciable boost to the power handling capability of a current regulator. Such a power regulator circuit is shown in Figure 8, where both the operating voltage and regulating current are set by the selection of the MOSPOWER FET, Q2. Regulation may suffer somewhat when using large MOSPOWER FETs due to the higher g_{os} typical of large power FETs. Q2, operating in the linear mode, will, in all likelihood, require a heatsink. The basic regulator circuit, Q1 and R_S, is used to establish a small bias current that, in conjunction with R1, sets the bias level for the enhancement-mode MOSPOWER FET.

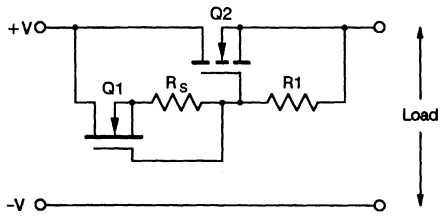

Figure 8. Extended-Range Current Limiter

A Simple Regulator for Telecom

Modern telephone handsets are steadily increasing their electronic content. Useful features, such as a memory to retain the last number dialed, require constant voltage to retain the information in memory. Typically, small memory ICs require only a few microamperes at 3 to 4 V to perform. This sustaining voltage must be available at all times, even when the phone is inactive or "on hook." Some handsets use a small battery cell to fill this need, while other designs use the −48 V which are available from the telephone line.

To utilize the incoming line, one needs to reduce the voltage and loosely regulate it, without consuming much power. In most systems, current drain in excess of 10 to 15 μA will alert the central office to an "off hook" condition and the subscriber's phone is presumed "busy." A simple depletion-mode regulator using the ND2410 can satisfy these requirements very economically. As shown in Figure 9, the depletion-mode MOSFET is used in a current-regulator mode to supply 10 μA to a 500-kΩ load. This establishes a voltage of 5-V to power the memory circuit. If the memory requires 2 microamperes, only 8 μA will flow through the resistor, and the voltage drops to 4 V, which is sufficient to sustain the memory. Should the telecom line rise to 60 volts, the current regulator continues to supply a fixed 10 μA to the load; the surplus voltage is dropped by the MOSFET. The regulation is not precise, but more than sufficient to provide a simple and reliable solution. Alternatives such as 3-terminal bipolar regulators require high bias currents (over 1 mA) and are not readily available to sustain the high voltages necessary for use on telephone lines.

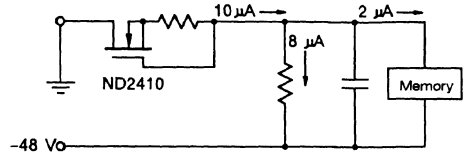

Figure 9. Telecom Voltage Regulator for Memory – Resident Redialing

As a Switch

When considering a switch, we usually select one whose natural, quiescent state is either normally-on or normally-off. With no applied power (or voltage), the depletion-mode MOSFET is normally-on.

Improving the dV/dt of Thyristors

The ND2410 can be used very effectively in power SCR circuits to improve the critical dV/dt rating. Spurious turn-on of an SCR caused by dV/dt can result in permanent damage to an SCR or an out-of-sequence turn-on that can have disastrous effects in high-powered phase-control equipment.

Traditionally, SCRs fired by pulse transformers have used a resistor from gate to cathode to shunt false gate signals caused by dV/dt as shown in Figure 10. This method requires a large wattage resistor, since the normal gate trigger signal is also applied across the resistor. The resistor, therefore, shunts part of the normal gate current, thus reducing the signal available for adequate turn-on of the SCR. The ideal solution would be a shunting resistor that seems to disappear when a normal gate signal is applied.

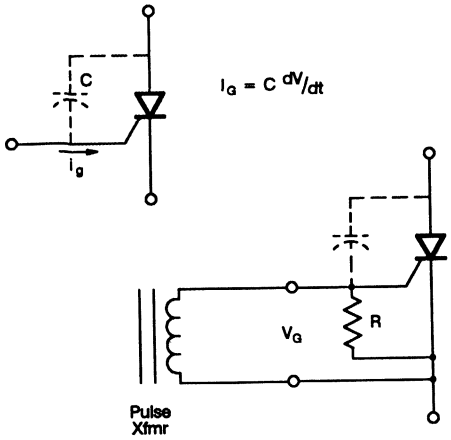

Figure 10. dV/dt Triggering of SCRs

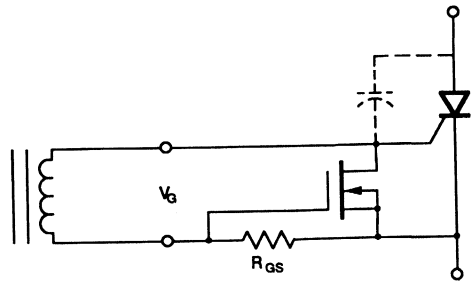

Figure 11. Depletion-Mode Active Shunt

Just such an effect can be achieved using the normally on feature of the ND2410 as shown in Figure 11. With no gate pulse applied, the depletion-mode transistor is "on" with an equivalent resistance of about 10 Ω. When the gate current is applied, the voltage drop across R_{GS} turns the transistor off, allowing all of the gate current to flow through the SCR gate.

Since the MOSFET turns off in a few nanoseconds, it has very little effect on normal SCR operation. In an actual experiment, the dV/dt of a 25-A SCR (similar to a 2N692) was improved from 300 V/μs (with no gate shunt network) to 2000 V/μs with the depletion-mode shunt.

Some suggestions for effective operation:

1. Use a fast-rising gate pulse: $I_G > 3 \times I_{gt}$
2. The shunt should be located as physically close to the SCR gate terminal as possible to reduce the winding inductance and noise pick-up from long gate wires.
3. $R_{GS} \geq \frac{V_{GS(off)}}{I_G}$
4. Do not use with non-isolated gate drive circuits; a pulse transformer should be used.

8

SPICE PARAMETERS FOR SELECT JFETS

Ed Oxner

INTRODUCTION

SPICE is the de facto standard for simulating circuit performance. Abundant libraries are available, but many of them were derived from data sheets. Data sheets seldom define the product—at best they offer minimum performance guarantees. Furthermore, often the programs used to develop these faulty library models default parameters that rightfully need to be extracted.

The following table of SPICE parameters have been extracted from measurements—none have been derived from data sheets. Additionally, the parameters for each geometry have been verified by modeling, both as a sine-wave and pulse amplifier, with excellent precision.

The following table of parameters will input directly into the PSPice®[1] circuit file. To users familiar with PSPice, where CDS or ALPHA is offered, the MODEL statement is the GASFET; otherwise it is the JFET.

Be aware that SPICE parameters for any semiconductor—JFETs included—are valid only for that manufacturer. Because of the vagaries in design, the product of one manufacturer seldom matches that of another. This is especially true for the critically-important parameters, RS and RD.

The following represents typical models of Siliconix FETs. However, we make no warranty, implied, expressed or otherwise, for their accuracy. These models are offered only as a guide for use in circuit analysis.

We encourage interested users to contact Analog Applications Engineering (408-970-5321) for additional data that may not have been available at the time of this publication.

SPICE PARAMETERS

Geometry/ Part Number	VTO	BETA	LAMBDA	RS	RD[a]	CGS	CGD	CDS[a]	ALPHA
NCB/2N4391	-5	4.9 M	35 M	13	13	14 P	9.5 P	1.1 P	1.5
NH/2N4416	-3	1.7 M	4.7 M	55	-	2.48 P	1.72 P	-	0.8
NPA/2N4339	-0.88	0.85 M	5 M	50	-	3.7 P	3.5 P	-	
NNT/½U401	-1.15	3.33 M	15 M	314	-	0.71 P	0.64 P	-	
NZB/U310	-1.22	10.8 M	10 M	10	-	5.37 P	3.5 P	-	
NZF/J211	-3.15	2.25 M	4.3 M	23	-	3 P	3 P	-	0.8
PSCIA/2N5116	-1.78[b]	4.7 M	5 M	20	35	14 P	13 P	1.1 P	1.5

Notes:

a. These parameters are only important when modeling the JFET as a switch.

b. SPICE identifies depletion-mode FETs (all JFETs, regardless of polarity) by a negative VTO.

When ALPHA and CDS are offered, the PSPice model used is the GASFET, not the JFET model.

For the parameter I_S, refer to the Gate Operating Current for the particular geometry, which may be found among the typical characteristic curves in the Data Book.

[1] PSPice is the registered trade mark of MicroSim Corporation.

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Publications Index 9
Worldwide Sales Offices and Distributors 10

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Publications Index
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(615) 475-9012/3
FAX: 615-475-6340

TEXAS

Austin (78759)
Ion Associates, Inc.
4412 Spicewood Springs Road
Ste 1008
(512) 794-9008/9007
FAX: 512-794-9008

Grand Prairie (75050)
Ion Associates, Inc.
1504 109th Street
(214) 647-8225
Easylink: 62956328
FAX: 214-641-9839

Houston (77014-1696)
Ion Associates, Inc.
14300 Cornerstone Village Drive
Suite 228
(713) 537-7717
FAX: 713-537-5612

TEXAS (El Paso Area)

See New Mexico

UTAH

See Idaho

VERMONT

See Massachusetts

VIRGINIA

Charlottesville (22901)
Third Wave Solutions
2100 Wisteria Drive
(804) 974-7575
FAX: 804-974-7480

WASHINGTON

Bellevue (98005)
QR/Crown, Inc.
375 118th Ave., S.E.
(206) 453-5100
FAX: 206-646-6775

WEST VIRGINIA

See Ohio

WEST WISCONSIN

See Minnesota

WISCONSIN

Wauwatosa (53226)
Larsen Associates, Inc.
10855 West Potter Road
(414) 258-0529
FAX: 414-258-9655

WYOMING

See Colorado

DISTRICT OF COLUMBIA

See Maryland

Canadian Sales Representatives

Islington, Ontario (M9B6E3)
Pipe Thompson, Ltd.
5468 Dundas Street W.
Suite 208
(416) 236-2355
FAX: 416-236-3387

Chip Distributor

FLORIDA

Orlando (32810)
Chip Supply, Inc.
7725 N. Orange Blossom Trail
(407) 298-7100
TWX: 810-850-0103
FAX: 407-290-0164

U.S. Distributors

ALABAMA

Huntsville (35805-6229)
Future Electronics Corp.
4950 Corporate Drive NW, Suite 145
(205) 830-2322
FAX: 205-830-6664

Huntsville (35805)
Hamilton/Avnet, #23
4960 Corporation Drive Ste 135
(205) 837-7210
FAX: 205-721-0356

Huntsville (35801)
Marshall Industries
3313 Memorial Parkway South Ste 150
(205) 881-9235
FAX: 205-881-1490

Huntsville (35805)
Pioneer Tech.
4835 University Square Ste 5
(205) 837-9300
FAX: 205-837-9358

ARIZONA

Chandler (85226)
Hamilton/Avnet, #04
30 S. Mc Kemy Ave.
(602) 961-6400
FAX: 602-961-1331

Phoenix (85044)
Marshall Industries
9830 S. 51st St., Ste. B121
(602) 496-0290
FAX: 602-893-9029

Phoenix (85040)
Wyle Laboratories-EMG
4141 E. Raymond St., Suite 1
(602) 437-2088
FAX: (602) 437-2124

CALIFORNIA

Agoura Hills (91301)
Zeus Components
5236 Colodny Drive
(818) 889-3838
FAX: 818-889-2464

Calabasas (91302)
Wyle Laboratories
26677 W. Agoura Rd
(818) 880-9000
FAX: 818-880-5510

Chatsworth (91311)
Future Electronics Corp.
9301 Oakdale Ave., Suite #210
(818) 772-8240
FAX: 818-772-6247

Chatsworth (91311)
Marshall Industries
9710 DeSoto Avenue
(818) 407-0101
FAX: 818-709-5334

Costa Mesa (92626)
Hamilton/Avnet, #29
3170 Pullman Street
(714) 641-4100
FAX: 714-641-4122

Culver City (90230)
Hamilton Corporate
10950 W. Washington Blvd.
(213) 558-2000
FAX: 213-558-2076

El Monte (91731)
Marshall Corporate
9320 Telstar Avenue
(818) 307-6000
FAX: 818-307-6297

Gardena (90248)
Hamilton Electro Sales, #01
1361 "B" W. 190th Street
(213) 217-6850
FAX: 213-217-6873

Irvine (92714)
Future Electronics Corp.
1692 Browning Ave.
(714) 250-4141
FAX: (714) 250-4185

Irvine (92718)
Marshall Industries
1 Morgan
(714) 859-5050
FAX: 714-581-5255

Irvine (92714)
Wyle Laboratories-EMG
17872 Cowan Avenue
(714) 863-9953
TWX: 910-595-1572
FAX: 714-863-0473

Milpitas (95035)
Marshall Industries
336 Los Coches St.
(408) 942-4600
FAX: 408-262-1224

Rancho Cordova (95670)
Marshall Industries
3039 Kilgore Ave. #140
(916) 635-9700
FAX: 916-635-8044

Rancho Cordova (95742)
Wyle Distribution Group
Sacramento Division
2951 Sunrise Blvd., Ste. 175
(916) 638-5282
FAX: 916-638-1491

Reseda (91335)
JAN Devices
8925 Canby, Bldg. 109
(818) 708-1100
FAX: 818-708-7436

Rocklin (95677)
Bell Industries
4311 Anthony Ct., #100
(916) 652-0414
FAX: 916-652-0403

Siliconix incorporated

U.S. Distributors (Cont'd)

CALIFORNIA (Cont'd)

Roseville (95661)
Hamilton/Avnet, #35
755 Sunrise Avenue Sre 150
(916) 781-6614
FAX: 916-781-3819

San Diego (92123)
Future Electronics Corp.
3940 Ruffin Road, Unit E
(619) 278-5020
FAX: (619) 576-8564

San Diego (92123)
Hamilton/Avnet, #02
4545 Viewridge Avenue
(619) 571-7540
FAX: 619-277-6136

San Diego (92131)
Marshall Industries
10105 Carroll Canyon Road
(619) 578-9600
FAX: 619-586-0469

San Diego (92123)
Wyle Laboratories-EMG
9525 Chesapeake Drive
FAX: 619-565-6512

San Jose (95131)
Future Electronics Corp.
2220 O'Toole Avenue.
(408) 434-1122
FAX: (408) 433-0822

San Jose (95119)
Zeus Components
6276 San Ignacio Ave., Ste. E
(408) 629-4789
FAX: 408-629-4792

Santa Clara (95052)
Wyle Distribution Group
3000 Bowers Avenue
(408) 727-2500
TWX: 910-379-6480
FAX: 408-727-5896

Sunnyvale (94089)
Bell Industries
1161 No. Fairoaks Avenue
(408) 734-8570
Fax: 408-734-8875

Sunnyvale (94089)
Hamilton/Avnet, #03
1175 Bordeaux Drive
(408) 743-3300
FAX: 408-745-6679

Woodland Hills (91367)
Hamilton /Avnet, #48
21150 Califa St.
(818) 594-0404
FAX: 818-594-8234

Yorba Linda (92686)
Zeus Components
22700 Savi Ranch Pkwy.
(714) 921-9000
FAX: 714 -921-2715

COLORADO

Broomfield (80021)
Future Electronics Corp.
9030 Yukon St., Suite 2700
(303) 421-0123
FAX: 303-421-7696

Englewood (80112)
Hamilton/Avnet, #06
9605 Marcon Clr. #200
(303) 799-7800
FAX: 303-799-7801

Thornton (80241)
Marshall Industries
12351 N. Grant St. Ste A
(303) 451-8444
FAX: 303-457-2899

Thornton (80241)
Wyle Distribution Group
451 E. 124th Avenue
(303) 457-9953
FAX: 303-457-4831

Wheatridge (80033)
Bell Industries
12421 W. 49th Avenue
(303) 424-1985
FAX: 303-424-0932

CONNECTICUT

Bethel (06801)
Future Electronics Corp.
24 Stony Hill Road
(203) 743-9594
FAX: 203-798-9745

Danbury (06810)
Hamilton/Avnet, #21
55 Federal Road
(203) 797-2800
FAX: 203-791-0373

Milford (06460)
Falcon Electronics
5 Higgins Drive
(203) 878-5272
FAX: 203-877-2010

Norwalk (06851)
Pioneer Std.
112 Main Street
(203) 853-1515
FAX: 203-838-9901

Waltingford (06492)
Marshall Industries
20 Sterling Drive
Barnes Industrial Park
(203) 265-3822
FAX: 203-284-9285

FLORIDA

Altamonte Springs (32701)
Marshall Industries
380 S. Northlake Blvd.,Ste.1024
(407) 767- 8585
FAX: 407-767-8676

Altamonte Springs (32701)
Pioneer Tech.
337 South Northlake Blvd. #1000
(407) 834-9090
FAX: 407-834-0865

Deerfield Beach (33441)
Pioneer Tech.
674 S. Military Trail
(305) 428-8877
FAX: 305-481-2950

Fort Lauderdale (33309)
Hamilton/Avnet, #17
5371 N.W. 33rd Avenue
(305) 484-5016
FAX: 305-484-8369

Fort Lauderdale (33309)
Marshall Industries
2700 W. Cypress Creek Rd.
Suite D114
(305) 977-4880
FAX: 305-977-4887

Oveida (32765)
Zeus Components
1750 W. Broadway, Ste. 114
(407) 365-3000
FAX: 407-365-2358

St. Petersburg (33716)
Hamilton/Avnet, #25
3247 Tech Drive No.
(813) 572-4346
FAX: 813-572-0633

Winter Park (32792)
Hamilton/Avnet, #76
7079 University Blvd.
(407) 628-3888
FAX: 407-678-4414

GEORGIA

Norcross (30071)
Future Electronics Corp.
3000 Northwoods Pkwy., Suite 295
(404) 441-7676
FAX: 404-441-7580

Norcross (30092)
Hamilton/Avnet, #15
5825 Peachtree Corners E-D
(404) 447-7500
FAX: 404-825-5490

Norcross (30093)
Marshall Industries
5300 Oakbrook Pkwy.,Ste.140
(404) 923-5750
FAX: 404-923-2743

Duluth (30136)
Pioneer Tech.
4250C Rivergreen Parkway
(404) 623-1003
FAX: 404-623-0865

ILLINOIS

Addison (60101)
Pioneer Std.
2171 Executive Drive
Suite 200
(708) 495-9680
FAX: 708-495-9831

Bensenville (60106)
Hamilton/Avnet, #10
1130 Thorndale Avenue
(708) 860-7780
FAX: 708-860-8530

Schaumburg (60195)
Future Electronics Corp.
1000 East State Pkwy., Suite B
(708) 882-1255
FAX: 708-490-9290

Schaumburg (60173)
Marshall Industries
50 E. Commerce Dr., Unit I
(708) 490-0755
FAX: 708-490-0569

INDIANA

Carmel (46032)
Hamilton/Avnet, #28
485 Gradle Drive
(317) 844-9533
FAX: 317-844-5921

Indianapolis (46278)
Marshall Industries
6990 Corporate Drive
(317) 297-0483
FAX: 317-297-2787

Indianapolis (46240)
Pioneer Std.
9350 N. Priority Way West Dr.
(317) 573-0880
(800) 332-5503 (IN)
(800) 428-9128 (IL, KY)
FAX: 317-573-0979

IOWA

Cedar Rapids (52402)
Hamilton/Avnet, #44
2335-A Blairsferry N.E.
(319) 393-0033
(800) 332-4757
FAX: 319-393-7050

KANSAS

Lenexa (66214)
Marshall Industries
10413 W. 84th Terrace
(913) 492-3121
FAX: 913-492-6205

Lenexa (66219)
Hamilton/Avnet, #58
15313 W. 95th
(913) 888-1055
FAX: 913-541-7951

KENTUCKY

Lexington (40511)
Hamilton/Avnet
805A Newtown Circle
(606) 259-1475
FAX: 606-252-3238

MARYLAND

Columbia (21046)
Future Electronics Corp.
7195 Columbia Gateway, Suite G
(301) 290-0600
FAX: 301-290-0328

Columbia (21045)
Hamilton/Avnet, #12
6822 Oak Hall Lane
(301) 995-3500 (MD)
(301) 621-5410 (DC)
FAX: 301-995-3553

Columbia (21045)
Zeus Components
8930-A Route 108
(301) 997-1118
FAX: 301-964-9784

Gaithersburg (20760)
Pioneer Tech.
9100 Gaither Road
(301) 921-0660
FAX: 301-921-4255

Silver Springs (20904)
Marshall Industries
2221 Broad Birch Dr., Ste. G
(301) 622-1118
FAX: 301-622-0451

MASSACHUSETTS

Lexington (02173)
Pioneer Std.
44 Hartwell Ave.
(617) 861-9200
FAX: 617-863-1547

Wakefield (01880)
Zeus Components
607 North Avenue
11 Lakeside Office Park
(617) 246-8200
FAX: 617-246-8293

Peabody (01960)
Hamilton/Avnet, #18
10 D Centennial Drive
(508) 531-7430
FAX: 508-532-9802

Bolton (01740)
Future Electronics Corp.
41 East Main Street
(508) 366-4200
FAX: (508) 366-1195

Wilmington (01887)
Marshall Industries
33 Upton Dr.
(508) 658-0810
FAX: 508-657-5931

U.S. Distributors (Cont'd)

MICHIGAN

Grandville (49418)
Hamilton/Avnet, #67
2676 28th St, S. W. Ste. 5
(616) 531-0345
(800) 632-9370
FAX: 616-531-0059

Grand Rapids (49512)
Pioneer Std.
4505 Broadmoor Ave. SE
(616) 698-1800
FAX: 616-698-1831

Livonia (48150)
Future Electronics Corp.
35200 Schoolcraft Rd., Suite 106
(313) 261-5270
FAX: 313-261-8175

Livonia (48150)
Marshall Industries
31067 Schoolcraft Rd.
(313) 525-5850
FAX: 313-525-5855

Livonia (48150)
Pioneer Std.
13485 Stamford Ct.
(313) 525-1800
FAX: 313-427-3720

Novi (48050)
Hamilton/Avnet, #66
41650 Gardenbrook, #100
(313) 347-4271
(800) 632-9370
FAX: 313-347-4021

MINNESOTA

Eden Prairie (55344)
Future Electronics Corp.
10025 Valley View Rd., Suite 196
(612) 944-2200
FAX: 612-944-2520

Eden Prairie (55344)
Pioneer Std.
7625 Golden Triangle Dr.
(612) 944-3355
FAX: 612-944-3794

Minnetonka (55343)
Hamilton/Avnet, #63
12400 Whitewater Dr.
(612) 932-0606
(800) 662-3948
FAX: 612-932-0613

Plymouth (55447)
Marshall Industries
3955 Annapolis Lane
(612) 559-2211
FAX: 612-559-8321

MISSOURI

Bridgeton (63044)
Marshall Industries
3377 Hollenberg Drive
(314) 291-4650
FAX: 314-291-5391

Chesterfield (63005)
Hamilton/Avnet, #05
739 Goddard Avenue
(314) 537-4265
(800) 325-6854
FAX: 314-537-4248

St. Louis (63141)
Future Electronics Corp.
11067 North Mason Road
(314) 469-6805
FAX: 314-469-7226

NEW HAMPSHIRE

See Machusetts

NEW JERSEY

Cherry Hill (08003)
Hamilton/Avnet, #14
One Keystone Avenue
(609) 424-0100
FAX: 609-751-2509

Fairfield (07006)
Hamilton/Avnet, #19
10 Industrial Road
(201) 575-3390
FAX: 609-751-2552

Fairfield (07006)
Marshall Industries
101 Fairfield Road
(201) 882-0320
FAX: 201-882-0095

Fairfield (07006)
Pioneer Std.
14 "A" Madison Rd.
(201) 575-3510
FAX: 201-575-3454

Marlton (08053)
Future Electronics Corp.
12 E. Stow Road, Ste. 200, Bldg. 12
(609) 778-7600
FAX: 609-596-4266

Mt. Laurel (08054)
Marshall Industries
158 Gaither Dr., Unit 100
(609) 234-9100 (NJ)
(215) 627-1920 (PA)
FAX: 609-778-1819

Parsippany (07054)
Future Electronics Corp.
1259 Route 46 East
(201) 299-0400
FAX: 201-299-1377

NEW MEXICO

Albuquerque (87123)
Bell Industries
11728 Linn N.E.
(505) 292-2700
FAX: 505-275-2619

Albuquerque (87106)
Hamilton/Avnet, #22
5659 Jefferson St. N.E.
Ste. A & B
(505) 345-0001
TWX: 910-989-0614
FAX: 505-345-2024

NEW YORK

Binghamton (13904)
Pioneer Std.
68 Corporate Dr.
(607) 722-9300
FAX: 607-722-9562

Buffalo (14202)
Summit, Inc.
916 Main Street
(716) 887-2800
FAX: 716-887-2866

East Syracuse (13206)
Hamilton/Avnet, #08
103 Twin Oaks Drive
(315) 437-2642
TWX: 710-541-1560
FAX: 315-432-0740

Fairport (14450)
Pioneer Std.
840 Fairport Park
(716) 381-7070
FAX: 716-381-5955

Hauppauge (11788)
Future Electronics Corp.
801 Motor Parkway
(516) 234-4000
FAX: 516-234-6183

Hauppauge (11788)
Hamilton/Avnet, #20
933 Motor Parkway
(516) 434-7420
FAX: 516-434-7426

Johnson City (13790)
Marshall Industries
129 Brown Street
(607) 798-1611
FAX: 607-797-7031

Liverpool (13088)
Future Electronics Corp.
7453 Morgan Rd.
(315) 451-2371
FAX: 315-451-7258

Port Chester (10573)
Zeus Components
100 Midland Avenue
(914) 937-7400
FAX: 914-937-2553

Rochester (14620)
Future Electronics Corp.
333 Metro Park
(716) 272-1120
FAX: 716-272-7182

Rochester (14623)
Hamilton/Avnet, #61
2060 Town Line Road
(716) 475-9130
FAX: 716-475-9119

Rochester (14624)
Marshall Industries
1250 Scottsville Road
(716) 235-7620
TWX: 510-253-5526
FAX: 716-235-0052

Ronkonkoma (11779)
Zeus Components
2110 Smithtown Ave.
(516) 737-4500
FAX: 516-737-4520

Westbury (11590)
Hamilton/Avnet, #39
1065 Old Country Road, Ste. 211A
(516) 997-6868
FAX: 516-886-6375

Woodbury (11797)
Pioneer Std.
60 Crossways Park W.
(516) 921-8700
FAX: 516-921-2143

NORTH CAROLINA

Charlotte (28209)
Future Electronics
4701 Hedgemore Dr., Suite 812
(704) 542-2256
FAX: 704-527-2222

Charlotte (28273)
Pioneer Tech.
9401-A Southern Pine Blvd.
(704) 527-8188
FAX: 704-522-8564

Raleigh (27604)
Future Electronics Corp.
5225 Capitol Blvd.
(919) 790-7111
FAX: 919-790-9022

Raleigh (27604)
Hamilton/Avnet, #24
3510 Spring Forrest Road
(919) 878-0819, X210
FAX: 919-954-0940

Raleigh (27604)
Marshall Industries
5224 Greens Dairy Rd.
(919) 878-9882
FAX: 919-872-2431

OHIO

Cleveland (44105)
Pioneer Std.
4800 E. 131st Street
(216) 587-3600
FAX: 216-587-3906

Dayton (45459-3953)
Hamilton/Avnet, #64
7760 Washington Village Dr.
(513) 439-6721
(800) 888-4714
FAX: 513-439-6711

Dayton (45414)
Marshall Industries
3520 Park Center Dr.
(513) 898-4480
FAX: 513-898-9835

Dayton (45424)
Pioneer Std.
4433 Interpoint Blvd.
(513) 236-9900
FAX: 513-236-8133

Dayton (45439)
Zeus Components
2912 Springboro West, Ste. 106
(513) 293-8162
FAX: 513-293-1781

Solon (44139)
Hamilton/Avnet, #62
30325 Bainbridge Rd., Bldg. A
(216) 349-4910
(800) 888-4714
FAX: 216-349-1894

Solon (44139)
Marshall Industries
30700 Bainbridge Rd. Unit A
(216) 248-1788
FAX: 216-248-2312

Columbia (43231)
Hamilton/Avnet, #79
2600 Corporate Exchange Dr.
Suite 180
(614) 882-7389
(800) 888-4714
FAX: 614-882-8650

OKLAHOMA

Tulsa (74146)
Hamilton/Avnet #46
12121 E. 51st St., Suite 102
(918) 252-7297
FAX: 918-250-8763

OREGON

Beaverton (97006)
Future Electronics Corp.
Cornell Oaks Corp. Center
15236 N.W. Greenbrier
Pkwy. Phase IIIA, Bld. A
(503) 645-9454
FAX: 503-645-1559

Siliconix incorporated

U.S. Distributors (Cont'd)

OREGON (Cont'd)

Beaverton (97005)
Hamilton/Avnet, #27
9409 SW Nimbus Ave.
(503) 627-0201
FAX: 503-641-4104 or
FAX: 503-641-5939

Beaverton (97005)
Marshall Industries
9705 S.W. Gemini
(503) 644-5050
FAX: 503-646-8256

Beaverton (97005)
Wyle Laboratories-EMG
9640 Sunshine Ct.
Bldg. G-200
(503) 643-7900
FAX: 503-646-5466

PENNSYLVANIA

Horsham (19044)
Pioneer Tech.
500 Enterprise Rd.
Keith Valley Business Center
(215) 674-4000
TWX: 510-665-6778
FAX: 215-674-3107

Mars (16046)
Hamilton/Avnet, #43
213 Executive Dr., Ste 320
(412) 281-4150
(800) 258-3848
FAX: 412-772-1890

Pittsburgh (15205)
Marshall Electronics
401 Parkwayview Drive
(412) 788-0441
FAX: 412-788-0447

Pittsburgh(15238)
Pioneer Std.
259 Kappa Drive
(412) 782-2300
FAX: 412-963-8255

TEXAS

Addison (75244)
Jaco Electronics
4251 Kellway Circle
(214) 733-4300
FAX: 214-250-0216

Austin (78758)
Hamilton/Avnet, #26
1826 F Kramer Lane
(512) 832-4306
(800) 525-9631
FAX: 512-832-4315

Austin (78758)
Pioneer Std.
1826 D Kramer Lane
(512) 835-4000
FAX: 512-835-8929

Austin (78758)
Jaco Electronics
2120-M Braker Lane
(512) 835-0220
FAX: 512-339-9252

Austin (78759)
Wyle Distribution
4030 W. Braker Lane
Ste. 330
(512) 345-8853
FAX: 512-345-9330

Carrollton (75006)
Marshall Industries
2045 Chenault St.
(214) 233-5200
FAX: 214-770-0675

Dallas (75244)
Hamilton/Avnet, #16
4004 Beltline Rd., Ste. 200
(214) 404-9906
FAX: 214-308-8109

Dallas (75244)
Pioneer Std.
13765 Beta Road
(214) 386-7300
FAX: 214-490-6419

Houston (77082)
Future Electronics Corp.
11271 Richmond Ave., Suite 106
(713) 556-8696
FAX: 713-589-7069

Houston (77040)
Marshall Industries
7250 Langtry
(713) 895-9200
FAX: 713-462-6714

Houston (77099)
Pioneer Std.
10530 Rockley Rd., Ste. 100
(713) 495-4700
FAX: 713-495-5642

Houston (77099)
Wyle Distribution
11001 S. Willcrest, #100
(713) 879-9953
FAX: 713-879-6540

Richardson (75081)
Future Electronics Corp.
185 N. Greenville Avenue, Suite 148
(214) 437-2437
FAX: 214-669-2347

Richardson (75081)
Wyle Distribution
1810 N. Greenville Avenue
(214) 235-9953
FAX: 214-644-5064

Richardson (75081)
Zeus Components
1800 N. Glenville Drive
Suite 120
(214) 783-7010
FAX: 214-234-4385

Houston (77008)
Hamilton/Avnet, #11
1235 North Loop West, Ste. 521
(713) 861-8517
FAX: 713-861-6541

Sugarland (77478)
Jaco Electronics
1005 Industrial Rd.
(713) 240-2255
FAX: 713-240-6988

UTAH

Salt Lake City (84119)
Future Electronics Corp.
2250 S. Redwood Rd. Ste. 8
(801) 972-8489
FAX: 801-972-3602

Salt Lake City (84121)
Hamilton/Avnet, #09
1100 E. 6600 S., Ste. 120
(801) 266-2022
FAX: 801-263-0104

Salt Lake City (84115)
Marshall Industries
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